Loop Enhanced Passive Source- and Load-Pull Technique for High Reflection Factor Synthesis

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Abstract—An original source- and load-pull topology based on a passive technique is presented in this paper. The proposed system consists of passive tuners and loop structures. The use of a passive loop structure in cascade with a passive tuner allows for synthesis of reflection coefficients in the order of 0.97 magnitudes at the device under test’s access plane. The measurement and characterization results of a 1W GaAs MESFET device show an improvement of 0.9 dB in the gain and 6% in the power-added efficiency when the proposed impedance synthesis techniques are used.

Index Terms—Load-pull, passive loop, reflection coefficient, source-pull, tuner.

I. INTRODUCTION

Ower amplifier characterization is essential in order to optimize its performance, in terms of output power, efficiency and linearity, on one hand, and extraction or validation of its large signal model, on the other hand. One of the most used measurement technique for power amplifier optimization is the well-known source- and load-pull measurement procedure, which consists of varying the impedances presented at the device input and output ports to optimize the amplifier’s performance. The variation of the impedances at the access planes of a device under test (DUT) can be performed using passive or active impedance synthesis or a combination thereof [1]–[10].

In a passive technique, the desired impedance is synthesized by varying the reflection coefficient of the impedance controlling element, as depicted in Fig. 1. The reflection coefficient is varied by tuning the phase and/or amplitude of the transmitted signal, b, with the help of a passive tuner. The main advantages of the passive technique are i) rapid impedance synthesis, ii) relatively higher power handling capability and measurements of high power devices with no nonlinear effects, iii) ease of usage, iv) low maintenance cost, v) relatively low implementation cost, and vi) the absence of any oscillation. However, due to the intrinsically passive nature of such systems, the synthesized reflection coefficients are typically limited in magnitude by the inherent losses in the tuner as well as the associated cablings. If the losses in the tuner are considered, then, depending on the operating frequency, the synthesized magnitude may range from 0.9 (few hundred MHz) down to 0.6 (approaching tens of GHz).

This major limitation implies that passive techniques cannot synthesize reflection coefficients whose values lie nearest to the Smith chart border. As a result, some Smith chart regions (those closer to the Smith chart border, i.e., low impedances) that are critical for high power devices are precluded. To overcome this issue, solutions have been proposed on the use of pre-matching networks [10], [11] at the device level or the use of pre-matched tuners [12], [13] at the measurement system level. In both these cases, the idea is based on the quarter-wave based pre-matching network transforming the tuner impedance to lower values.

The pre-matching network [10], [11] is capable of matching the microwave devices with sub-1 Ω output impedance; however, this requires additional hardware and calibration steps, increasing the size and cost of the system and the calibration time. State-of-the-art pre-matched passive structures [12], [13] are able to synthesize reflection coefficients in the order of 0.90–0.92 magnitudes in the practical applications, but the prices of such systems are relatively high. Passive source-/load-pull structure that are reasonably priced can typically synthesize reflection coefficient of magnitude 0.85.

Many source-/load-pull systems based on active structures have also been proposed in the literature [3]–[6], [14]–[18], in order to overcome the limitations encountered in the passive systems. Active load-pull systems consist of either active loop [4] or active branch [5] architectures. In both techniques, the reflection coefficient is synthesized at a DUT access plane by controlling the amplitude and phase of the injected signal. Active techniques of load synthesis suffers either from slow nature of load convergence in active branch structure or oscillation in the active loop architecture, thereby limiting the usefulness of active source-/load- pull systems.

Fig. 1. A basic representation of a passive load-pull technique.
To lessen the ultra high gain and high power requirements of the loop amplifier, a recent publication [7] has shown a load-pull system composed of an active structure and a passive structure combined together. The main claimed benefit reported in this publication is the replacement of ultra high gain loop amplifier with a reasonable high gain loop amplifier.

In this paper, a cost and calibration time effective passive structure for the synthesis of a high reflection coefficient is proposed. The passive structure is composed of a passive loop followed by a passive loop. The passive loop is composed of a low loss circulator, a low loss coupler and a variable length transmission line. Two separate configurations are proposed for source- and load-pull measurement purposes. The proposed system, based on the fully passive elements, allows synthesis of reflection coefficients with magnitudes in the order of 0.97 at the DUT access planes. Only three transmission line lengths are required to cover the entire Smith chart, which reduces the calibration time compared to conventional pre-matching techniques.

This paper presents a comprehensive description and analysis along with an experimental evaluation and validation of the proposed source- and load-pull setups. Finally, measurement and characterization of a gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET) device is presented that validates the performances of the proposed source- and load-pull architectures.

II. PROPOSED SOURCE- AND LOAD-PULL TOPOLOGY

A. Source Impedance Synthesis

The proposed source-pull topology is depicted in Fig. 2. It is apparent that the source impedance presented to the DUT input access plane, Plane—2, of the DUT is synthesized by the tuner, Tuner1, and the passive loop, which is composed of the circulator, \( C_\text{ir} = 1 \), and the directional coupler, \( C_1 \).

The following relationships among the traveling waves \( b_2, b_3 \) and \( b_4 \) can be expressed as

\[
\begin{align*}
  b_2 &= k_3 b_1 \\
  b_3 &= k_2 b_2 \\
  b_4 &= a_1 = k_3 b_3
\end{align*}
\]

where \( k_1, k_2 \) and \( k_3 \) are complex constants that depend on the scattering parameters of the directional coupler, \( C_1 \), and the circulator, \( C_\text{ir} = 1 \). The signal flow model for this architecture can be defined as given in Fig. 3.

The reflection coefficient presented by the passive loop structure, at Plane-1, is given by

\[
\Gamma_{\text{SOURCESCIRC}} = K_S = \frac{a_1}{b_1} = |K_S|e^{-2j\beta L_1}
\]

where factor \( K_S \) represents the combined effect of the circulator, \( C_\text{ir} = 1 \), and the coupler, \( C_1 \), and is defined by \( K_S = k_3k_2k_3 \). This factor depends on the length of the loop, \( L_1 \), and the phase velocity, \( \beta \), of the travelling waves.

The error model from Fig. 3 can now be solved to obtain the total reflection coefficient of the synthesized source impedance at the DUT input access plane, Plane — 2, as given by

\[
\Gamma_S = \frac{a}{b} = \frac{S_{1\text{Tuner1}} + S_{2\text{Tuner1}}S_{2\text{Tuner1}}K_S}{1 - S_{2\text{Tuner1}}K_S}
\]

It is apparent from (5) that the incorporation of a passive-loop between the RF source and the Tuner1 enhances the \( \Gamma_S \) by the additional second term. In principle the cascade of the RF source and the passive-loop structure can be considered as a generator with non-50 \( \Omega \) output impedance. This is the result of intentionally mismatching the source impedance of Tuner1.

In other words, this can also be considered as the superposition of two waves \( a_g \) and \( b_4 \) travelling towards Tuner1 contributing in the enhancement of the \( \Gamma_S \), where \( a_g \) is the wave generated by the RF source and \( b_4 \) is the wave caused by the reflected wave \( b_3 \) passing through the passive-loop and redirected toward Tuner1 by the passive-loop. The other parameter affecting the \( \Gamma_S \) is the length of the passive loop, \( L_1 \). It can be altered by utilizing cables of appropriate lengths.

B. Load Impedance Synthesis

The topology for the proposed load-pull setup is given in Fig. 4. The architecture combines a passive tuner and a passive loop at the DUT output access plane, Plane — 3. The coupling port of the directional coupler, \( C_2 \), is connected to a power meter, in order to monitor and measure the DUT performances in term of output power or linearity during source- and/or load-pull characterization.

From Fig. 4, the following expressions can be derived that relate the travelling waves

\[
\begin{align*}
  a_4 &= k_5a_3 \\
  a_5 &= k_5a_4 \quad (6) \\
  b_3 &= k_5a_5 \quad (8)
\end{align*}
\]
where \( k_4, k_5 \) and \( k_6 \) are the complex factors dependent on the scattering parameters of the circulator, \( C_\text{ir} \rightarrow 2 \), and the directional coupler, \( C_2 \).

Thus, between \( \text{Tuner2} \) and the passive loop plane, \( \text{Plane} = 4 \), the following expression for the mismatch reflection coefficient can be derived

\[
\Gamma_{\text{LOADLOOP}} = K_L = \frac{b_3}{a_3} = |K_L| \cdot e^{-2j\beta L_2}. \quad (9)
\]

The parameter \( K_L(=k_4k_5k_6) \) is a complex factor that depends on the passive loop structure characteristics, i.e., the transmission factors of coupler \( C_2 \) and circulator \( C_\text{ir} \rightarrow 2 \). It is evident from (9) that it is also dependent on the phase velocity, \( \beta \), of the travelling waves and the length of passive loop, \( L_2 \). The topology in Fig. 4 can be represented by the error model given in Fig. 5, which can then be analyzed to obtain the expression for the total reflection coefficient at the DUT output access plane, \( \text{Plane} = 3 \), given in

\[
\Gamma_L = \frac{b_2}{a_2} = S_{12\text{Tuner2}} + \frac{S_{12\text{Tuner2}}S_{22\text{Tuner2}}K_L}{1 - S_{22\text{Tuner2}}K_L}. \quad (10)
\]

Thus, it can be seen from (10) that the total load reflection coefficient, \( \Gamma_L \), is the reflection coefficient synthesized by \( \text{Tuner2} \), plus the additional contribution from the passive loop. As the parameter \( K_L \) is dependent on the length of the cable, \( L_2 \), in the passive loop, it can be altered by employing cables of appropriate lengths.

From the mathematical explanation it is clear that the new source- and load-pull topologies are able to synthesize higher reflection coefficients. Although similar to the popular pre-matching techniques [10], [11], these new architectures have two main benefits over the pre-matching approach: i) there is no need to consider the architecture as two different blocks of the pre-match tuner and the main tuner—the whole tuner and passive loop can be considered as a single impedance controlling element; and, ii) it is substantially more economical.

The next section provides the experimental evaluation of the proposed topologies.

III. EXPERIMENTAL EVALUATION OF THE NEW SETUP

For evaluation purposes, the source- and load-pull topologies were integrated into a nonlinear measurement system [19], while replacing the DUT with a ‘Thru’ standard. First, the measurement for validation of the performance of the source-pull topology is performed. The reflected and transmitted waves at the input port of the DUT are measured by employing a tuner alone and then again by deploying the proposed source-pull architecture. The synthesized source impedances using the tuner alone and the new source-pull architecture is shown in Fig. 6.

The maximum synthesized reflection coefficient in terms of magnitude, using \( \text{Tuner1} \) alone, is around 0.85, which is equivalent to a minimum real impedance of 4.05 \( \Omega \). The proposed source-pull architecture can synthesize a reflection coefficient of around 0.95, which is equivalent to 1.28 \( \Omega \). This is a significant improvement in the performance of the passive tuner and, hence, allows source-pull measurements of highly mismatched devices.

It is also evident that the synthesized impedances are concentrated in a certain region of the Smith chart. By varying the length of the loop, \( L_1 \) (i.e., changing the cables connecting \( C_\text{ir} \rightarrow 1 \) and \( C_1 \)), the location of the synthesized reflection coefficients can be changed.

To evaluate the new load-pull architecture, measurements were carried out to obtain the transmitted and reflected travelling waves at the output access plane, \( \text{Plane} = 3 \), of the
DUT by successively employing the passive tuner and then by employing the proposed architecture. The obtained results are depicted in Fig. 7. It demonstrates that the increase in the achievable load reflection coefficient is relatively significant. While the passive tuner was able to synthesize maximum load reflection coefficients of 0.75, equivalent to 7.14 Ω, the proposed architecture was able to synthesize a load reflection coefficient of 0.97, equivalent to 0.76 Ω.

It is also apparent from (9) that the orientation and location of the load reflection coefficient can be altered by changing the length of cable $L_2$. To demonstrate this, an experiment was performed with a different setup and employing a different length, $L_2$. The obtained result is displayed in Fig. 8.

It was, therefore, experimentally proven that the theoretical formulation in (9) is correct. The new load-pull architecture requires just three different sets of loop lengths, $L_2$, to cover the whole Smith chart and, hence, provides speedy and precise calibration of the setup as compared to the conventional pre-matching approach, which requires time-consuming calibration of a considerably higher number of positions for the pre-match tuner [11]. Moreover, in the conventional state-of-the-art pre-matching technique, the points’ density increases around one region, as shown in Fig. 8, close to the edge of the Smith chart, which covers just a small portion [11], thereby, affecting the accuracy of the interpolation algorithms [20]. The proposed approach, however, relocates the impedance points in a larger region on the edge of the Smith chart, which results in a less condensed constellation, hence higher coverage range and more accurate interpolation algorithms. Thus, the proposed architectures also improve the calibration time and the precision in setting the desired reflection coefficients.

It is also important to note that the proposed source- and load-pull structures utilize low loss circulators to close the respective loops. This helps in achieving the maximum source and load reflection coefficients, $\Gamma_S$ and $\Gamma_L$, respectively, for all settings of the passive tuners, as shown in Figs. 6–8.

The data presented in Table I compare the performance of the various types of passive source- and load-pull architectures at a carrier frequency of 2.425 GHz. It is evident that the proposed architectures perform better than the commercial pre-matched tuners. In addition to improved performance the proposed architecture is cost-effective, compared to commercial pre-matched tuners which are considerably more expensive.

It is also evident from Figs. 2 and 4 that the magnitudes of the source and load reflection coefficients, $\Gamma_S$ and $\Gamma_L$, depend on the magnitudes of the waves, $b_4$ and $a_6$, respectively. The higher the wave values of $b_4$ and $a_6$, the higher are the $\Gamma_S$ and $\Gamma_L$, respectively. The source-pull architecture contains a coupled path of the directional coupler (Fig. 2), which is not the case in the load-pull architecture (Fig. 4). Therefore, $a_6$ is higher in terms of magnitude than $b_4$. This leads to a slight higher achievable

<p>| TABLE I |</p>
<table>
<thead>
<tr>
<th>COMPARISON OF THE DIFFERENT TYPES OF EXISTING PASSIVE ARCHITECTURES EMPLOYED FOR SOURCE- AND LOAD-PULL WITH THE DEVELOPED ARCHITECTURES AT CARRIER FREQUENCY OF 2.425 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passive Source-Pull Techniques</td>
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<tr>
<td>Passive Tuner (Without Pre-Match)</td>
</tr>
<tr>
<td>Commercial Passive Tuner (With Pre-Match)</td>
</tr>
<tr>
<td>Proposed Source-Pull Architecture</td>
</tr>
</tbody>
</table>
Fig. 9. Fundamental gain contours for source impedance sweep using the passive tuner (Device: FLL107ME).

Fig. 10. Fundamental gain contours for source impedance sweep using the proposed source-pull topology (Device: FLL107ME).

Fig. 11. Fundamental output power contours for source impedance sweep using the passive tuner (Device: FLL107ME).

Fig. 12. Fundamental output power contours for source impedance sweep using the proposed source-pull topology (Device: FLL107ME).

\( I_L \) compared to the achievable \( I_S \), as shown in Table I, using the proposed architectures.

IV. DEVICE CHARACTERIZATION USING THE NEW SETUP

The proposed impedance synthesis techniques were integrated into a measurement system [19] at the iRadio Lab. Initially, a 1W MESFET from Fujitsu was characterized at a carrier frequency of 2.425 GHz to demonstrate the usefulness of the developed architectures.

As a first step, the optimal load impedance, identified from the device’s data sheet, was set using the load tuner, \( T_{\text{unr}}2 \). Then, the source impedance was swept using the source tuner, \( T_{\text{unr}}1 \), around the anticipated optimal source impedance.

The gain contours plotted and shown in Fig. 9 demonstrate that the gain showed a progressive nature as the source impedance moved towards the edge of the Smith chart. The proposed source-pull topology (Fig. 2) finds immediate application here. As demonstrated earlier, the source-pull architecture is capable of achieving a reflection coefficient of 0.95; therefore, the optimal load was set, and the source impedance was swept using the new source-pull architecture. The obtained result is given in Fig. 10: an optimal gain of 13.5 dB, which is an improvement of 0.9 dB over the result achieved and a gain of 12.6 dB, using a simple source tuner as shown in Fig. 9.

The impact of better source matching is also evident on the achieved output power contours shown in Figs. 11 and 12. The optimal output power obtained using the passive tuner, \( T_{\text{unr}}1 \), as the source-pull architecture was 29.6 dBm, whereas the optimal output power obtained using the proposed source-pull topology was 30.3 dBm.

According to Fig. 6, the setup is able to synthesize the source reflection coefficient of the order of 0.95 therefore a 1W device with very low source impedance was selected on purpose to demonstrate the usefulness of the developed system. The optimal source reflection coefficient was determined using the enhanced source-pull architecture and set at 0.92, as mentioned
For this device at the chosen bias and frequency conditions, the PAE without the optimal source impedance was around 59%, whereas it improved to 65% once the optimal source impedance was set.

The passive loop in the proposed load- and source-pull architecture is essentially a narrow band structure, due to the limited bandwidth of the used circulator, and therefore it re-injects power only at the fundamental frequency and rejects the harmonic components without passing through the loop. Thus, it provides an enhanced reflection coefficient only at the chosen fundamental frequency. The harmonic terminations in both the cases, with or without the passive loop, remains the same since same isolator was used in both configurations and therefore any increase in the achieved gain and PAE is attributed to the improved fundamental matching conditions at the source and load ports provided by the enhanced source- and load-pull architectures reported in this paper. Although this experiment can be performed using the solutions reported in [7], [10], [11] and [15], those solutions might lead to loop oscillation, are not cost effective or may not be able to synthesize the required input or and output reflection coefficients closer to the border of the Smith chart needed to pull the best performance from the device.

The proposed source-pull topology is also scalable to higher power and higher frequency applications without any problems. This was verified by characterizing a 3W MESFET from Fujitsu at the carrier frequency of 2.5 GHz. The measurement was carried out using both the passive tuner, Tuner1, and the proposed topology, respectively. The obtained result gave the optimal gain achievable using the passive tuner, Tuner1, as 11.9 dB. The gain contour, for the 3W device, obtained using the proposed source-pull architecture gave an optimal gain of 12.5 dB, which is an improvement of 0.6 dB. Thus, the measurement and characterization demonstrates that the proposed source-pull setup is easily scalable for higher power devices.

V. SUMMARY & CONCLUSION

This paper gives a comprehensive theoretical and experimental investigation of an innovative loop enhanced source- and load-pull architectures based wholly on using passive components. These passive structures are capable of synthesizing high reflection coefficients and have an advantage over active loop or hybrid active-passive architectures, since they do not suffer from the possibility of oscillations and nonlinearity problems. The implementation cost and calibration time are significantly lower compared to the commercialized systems that provide pre-matching techniques with similar or lower performances.

To the authors’ knowledge, there has been no report in literature of such a cost-effective and full passive solution which can synthesize highly reflective reflection coefficients. The proposed architectures would find immediate application in the characterization of microwave devices, particularly in the characterization of high power devices where the load-pull topology needs to synthesize a reflection coefficient nearer to the edge of the Smith chart.

in the source pull measurement above, then the load impedance was swept around the anticipated optimum location in the Smith chart according to the device datasheet. To prevent the device from instability and oscillation the highest load reflection coefficient presented to the DUT was limited to 0.92 despite that the developed system can achieve a load reflection coefficient of 0.97 as shown in Figs. 7 and 8. Moreover, for this chosen device there was no need to present higher load reflection coefficient since the optimal magnitude of load reflection coefficient is around 0.5. The respective achieved results for the output power and power-added efficiency (PAE) are displayed in Figs. 13 and 14, respectively.

The optimal output power when using the proposed loop enhanced source- and load-pull architecture turns out to be 30.6 dBm, as shown in Fig. 13. For this device, the source impedance lies closer to the edge; hence, this source-pull setup is ideal for synthesizing the required impedance. The result in Fig. 14 displays the overall sensitivity of the varying load impedance on the PAE once the source impedance is set at the optimal value.
Further application of these architectures may be in the design and characterization of switching-mode power amplifiers where ideally the harmonic impedances need to be terminated at the edge of the Smith chart to achieve short and open conditions. The harmonic load-pull system using the proposed architectures could be based on the triplexer/diplexer based setup such as reported in [16]. The higher reflection coefficient synthesis using the proposed architectures will also enable the “all passive harmonic load-pull” to achieve higher reflection coefficients for the harmonic frequencies in comparison with the existing commercial systems [21], [22]. Obviously the magnitude of reflection coefficient will depend on the insertion loss of the used triplexer/diplexer.

ACKNOWLEDGMENT

The authors would like to acknowledge the technical assistance from the iRadio Lab staff at the University of Calgary.

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