Lecture – 13 Date: 29.09.2016

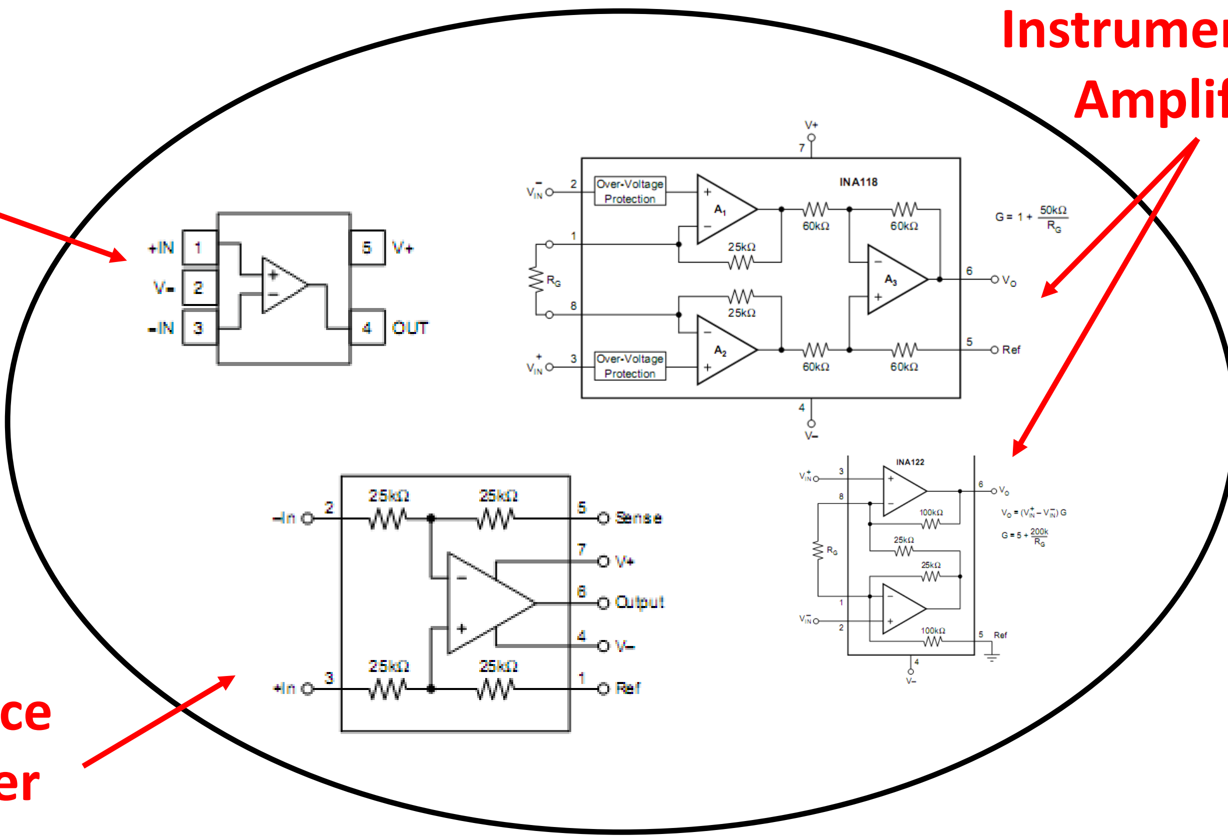
- Common Mode Rejection Ratio
- Non-Idealities in Differential Amplifier

Common Mode Rejection Ratio (CMRR)

- Differential input amplifiers are devices/circuits that can input and amplify differential signals <u>and</u> suppress common-mode signals
  - <u>This includes</u> operational amplifiers, instrumentation amplifiers, and difference amplifiers

Operational Amplifier

Instrumentation Amplifiers

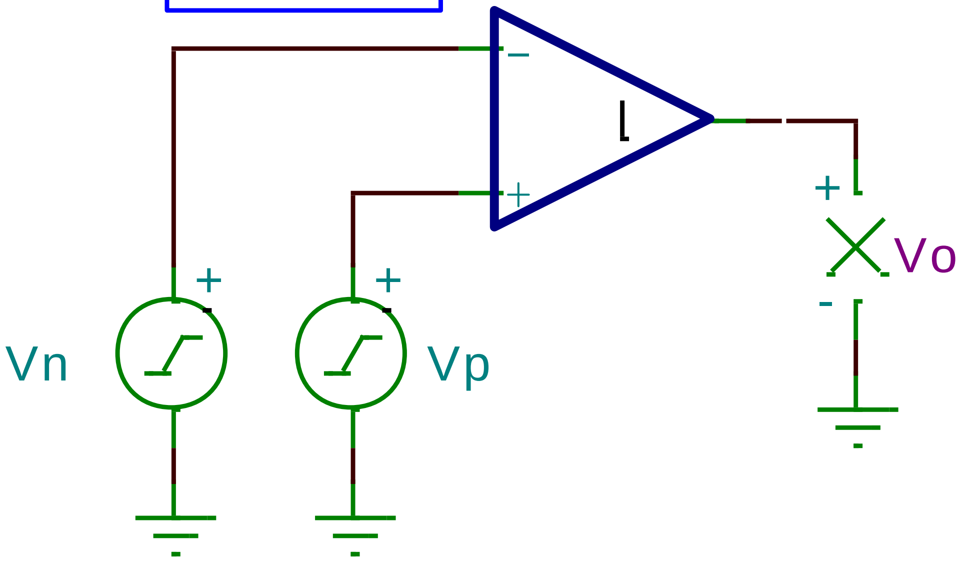


Difference Amplifier

Common Mode Rejection Ratio (CMRR) (contd.)

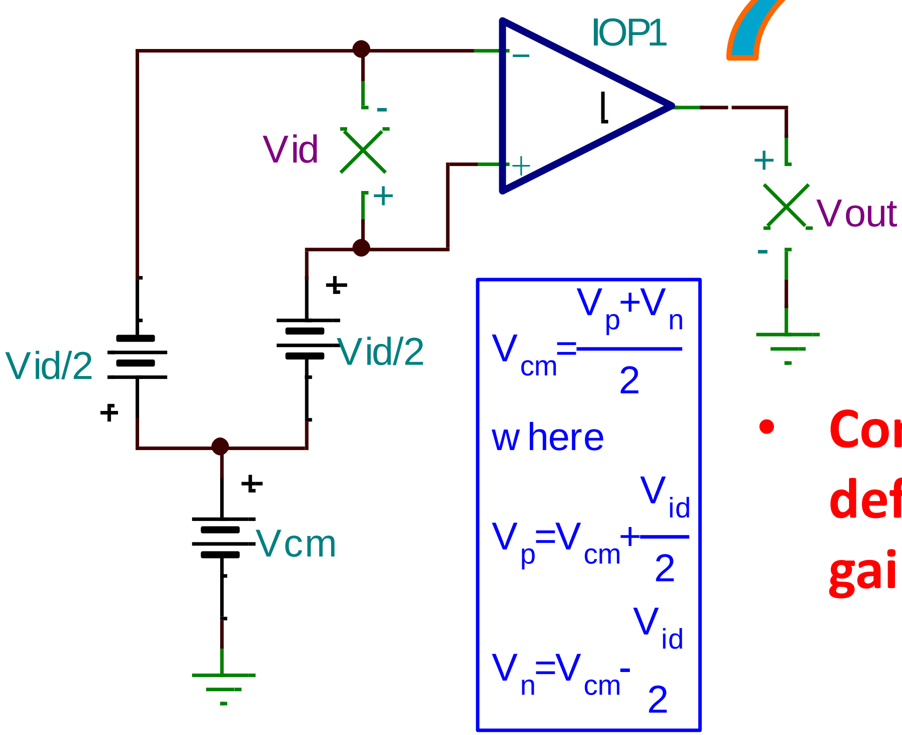
- For a differential input amplifier, common-mode voltage is defined as the average of the two input voltages.

$$\boxed{V_{cm} = \frac{V_p + V_n}{2}}$$



Common Mode Rejection Ratio (CMRR) (contd.)

- **For a differential amplifier, common-mode voltage is defined as the average of the two input voltages.**



$$V_{out} = A_{dm}\left(V_{id}\right) + A_{cm}\left(V_{cm}\right)$$

where

A_{dm} = Differential-mode gain

A_{cm} = Common-mode gain

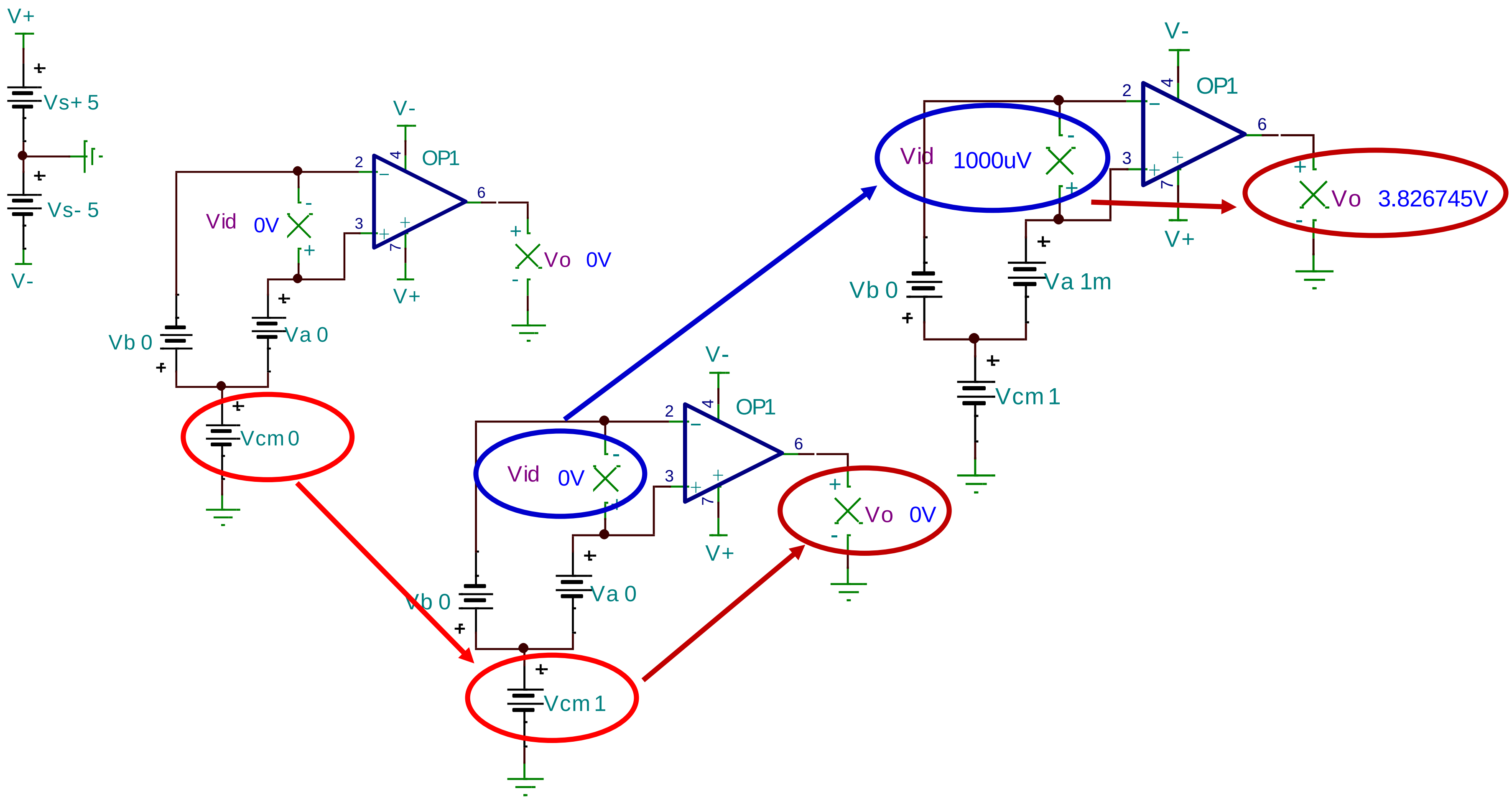
- **Common-Mode Rejection Ratio is defined as the ratio of the differential gain to the common-mode gain.**

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right|$$

- **CMR is defined as:** $CMR(dB) = 20\log_{10}(CMRR)$

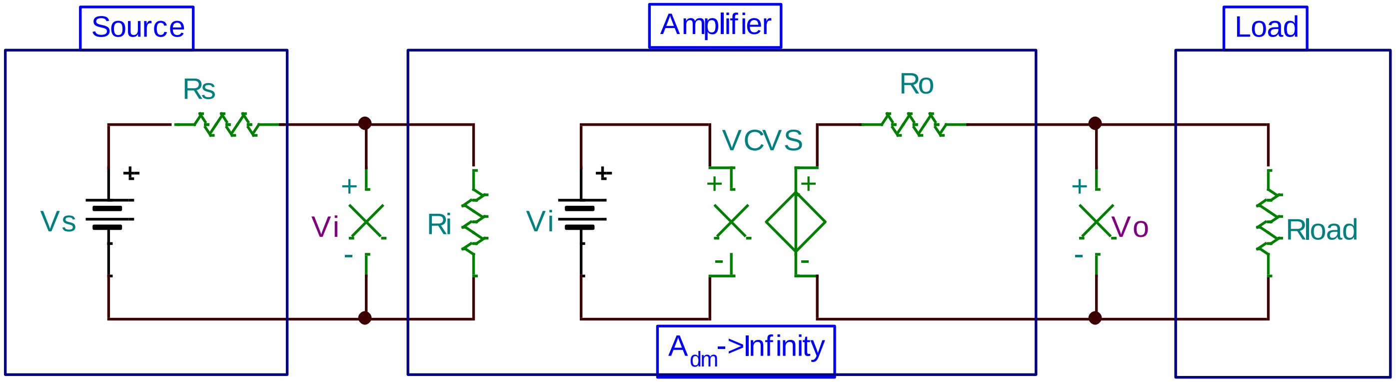
Common Mode Rejection Ratio (CMRR) (contd.)

- Ideally a differential input amplifier only responds to a differential input voltage, not a common-mode voltage.



Common Mode Rejection Ratio (CMRR) (contd.)

- **What is the CMRR of an ideal differential input amplifier (e.g. op-amp)?**
- **Recall that the ideal common-mode gain of a differential input amplifier is ZERO**
- **Voltage Amplifier Model:**



- **Also recall that the differential gain of an ideal op-amp is some high value.**
- **Therefore:**

$$CMRR_{ideal-OA} = \frac{A_{dm}}{A_{cm}} = \frac{A_{dm} \to \infty}{A_{cm} \to 0} \to \infty$$

Common Mode Rejection Ratio (CMRR) (contd.)

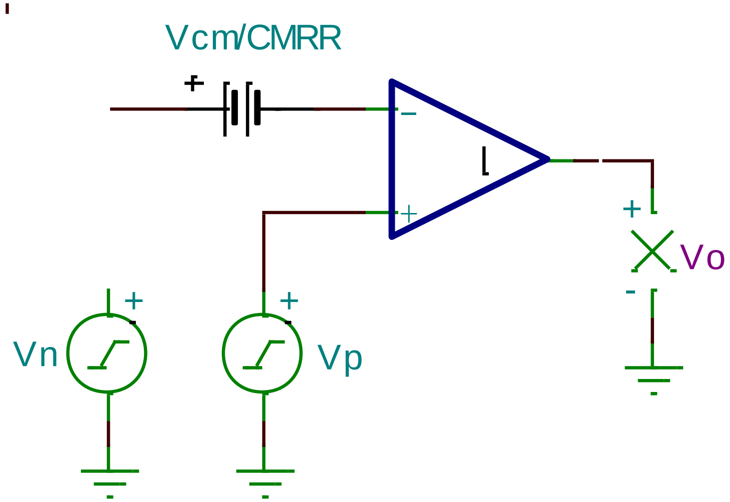
Real Op-Amp CMRR

- There will be a common-mode gain due to the following
  - Asymmetry in the circuit
    - Mismatched source and drain resistors
    - Signal source resistances
    - Gate-drain capacitances
    - transconductances
    - Gate leakage currents
  - Finite output impedance of the tail current source
  - Changes with frequency due to tail current source's shunt capacitance
- These issues will manifest themselves through converting common-mode variations to differential components at the output and variation of the output common-mode level

Common Mode Rejection Ratio (CMRR) (contd.)

Modeling CMRR

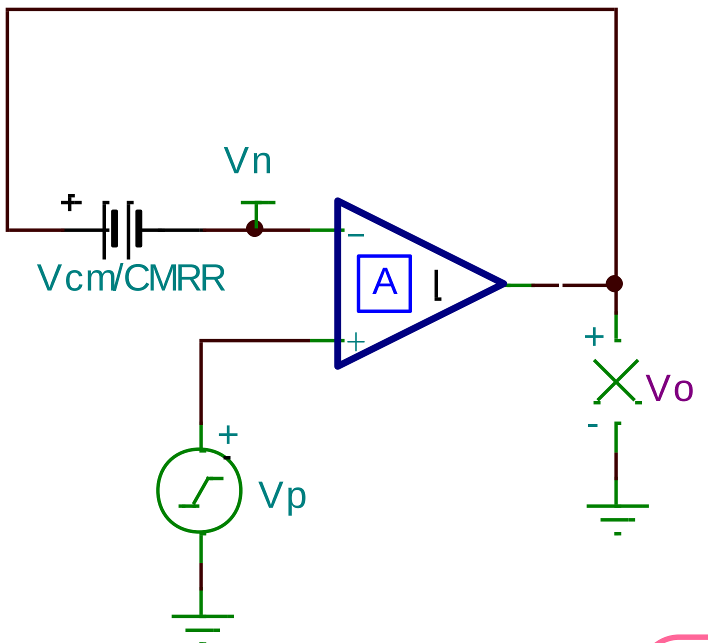
- Now that we understand what CMRR is and what affects it in operational amplifiers, let's see how it can affect a circuit.
- First, however, we need to understand the model
- To be useful, CMRR needs to be referred-to-input (RTI)
- We can then represent it as a voltage source (aka offset voltage) in series with an input. The magnitude (RTI) is V_{cm}/CMRR .



Common Mode Rejection Ratio (CMRR) (contd.)

OA CMRR Error

- **Example: non-inverting buffer**



$$V_O = A\left(V_p - V_n\right)$$

$$V_n = V_O \pm \frac{V_{cm}}{CMRR}$$

Note that $V_{cm} \approx V_p$

$$V_O = A\left(V_p - V_O \pm \frac{V_p}{CMRR}\right)$$

$$\frac{V_O}{V_p} = \frac{A\left(1 \pm \frac{1}{CMRR}\right)}{1 + A}$$

As $A \rightarrow \infty$

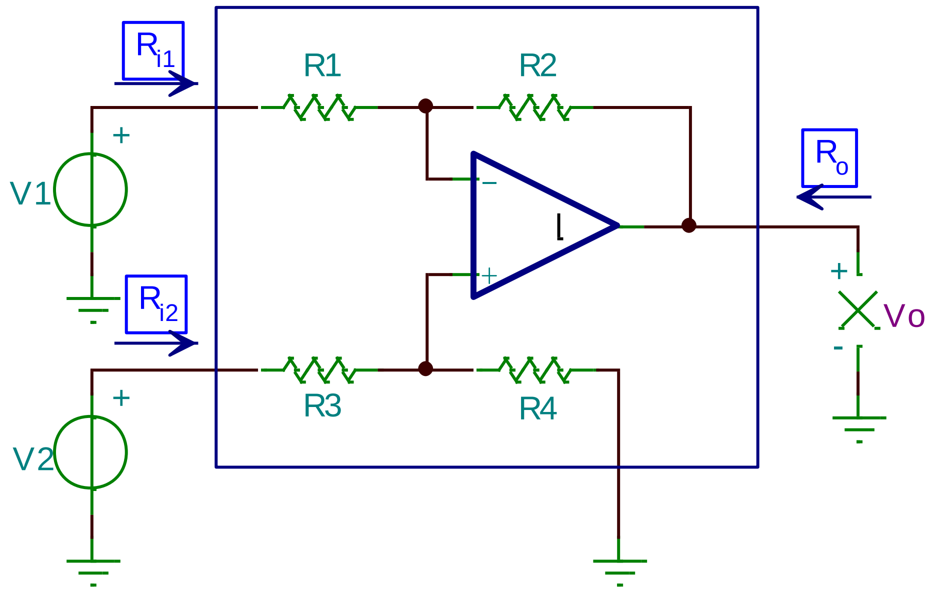
$$\frac{V_O}{V_p} \rightarrow 1 \pm \frac{1}{CMRR}$$

Clearly this factor should be as small as possible

Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

- A difference amplifier is made up of a differential amplifier (operational amplifier) and a resistor network as shown below
- The circuit meets our definition of a differential amplifier
- The output is proportional to the difference between the input signals



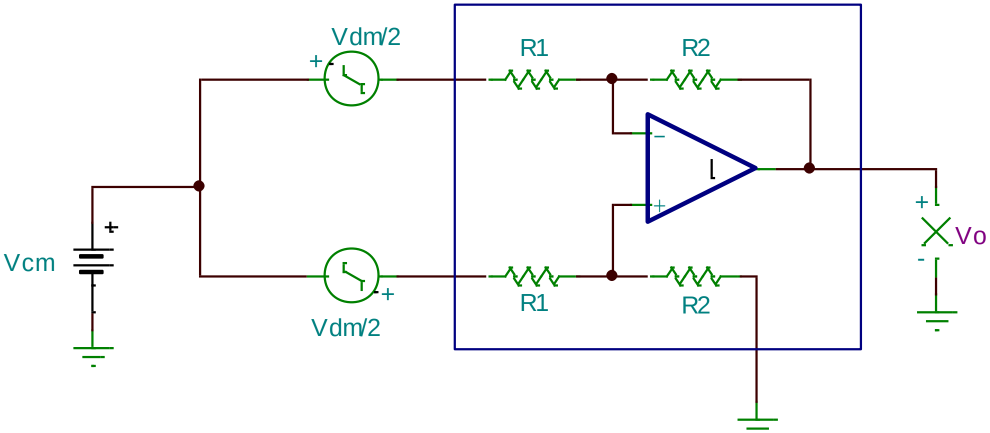
Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

$$V_1 = V_{cm} - \frac{V_{dm}}{2}$$

$$V_2 = V_{cm} + \frac{V_{dm}}{2}$$

- Let's replace V_1 and V_2 with our alternate definition of the inputs (in terms of differential-mode and common-mode signals).



$$V_o = \frac{R_2}{R_1}\left(V_2 - V_1\right)$$

$$V_o = \frac{R_2}{R_1}\left(\left(V_{cm} + \frac{V_{dm}}{2}\right) - \left(V_{cm} - \frac{V_{dm}}{2}\right)\right)$$

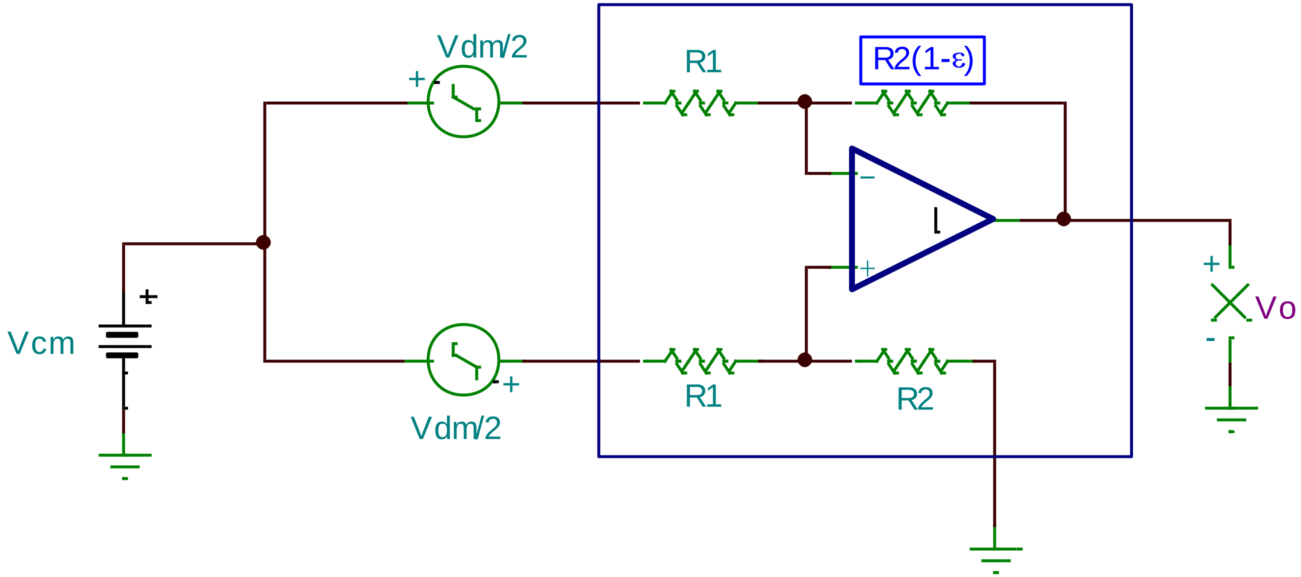
$$V_o = \frac{R_2}{R_1}\left(V_{dm}\right)$$

- It is readily apparent that an ideal difference amplifier's output should only amplify the differential-mode signal…not the common-mode signal.

Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

- The last expression is based on the premise that the operational amplifier is ideal and that the resistors are balanced
- Keeping the assumption that the operational amplifier is ideal, let's see what happens when an imbalance factor (ε) is introduced



Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

- **Using superposition we find that:**

$$V_o = \left(V_{cm} - \frac{V_{dm}}{2}\right)\left(-\frac{R_2(1-\varepsilon)}{R_1}\right) + \left(V_{cm} + \frac{V_{dm}}{2}\right)\left(\frac{R_2}{R_1+R_2}\right)\left(1 + \frac{R_2(1-\varepsilon)}{R_1+R_2(1-\varepsilon)}\right)$$

- **After simplification we find that:**

$$V_o = A_{dm}V_{dm} + A_{cm}V_{cm}$$

where

$$A_{dm} = \frac{R_2}{R_1}\left(1 - \frac{R_1+2R_2}{R_1+R_2} \times \frac{\varepsilon}{2}\right)$$

$$A_{cm} = \frac{R_2}{R_1+R_2} \times \varepsilon$$

As expected, an imbalance affects the differential and common-mode gains, which will affect CMRR!

As the error (ε) → 0, $A_{dm} \rightarrow R_2/R_1$ and $A_{cm} \rightarrow 0$

Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

- **Since we have equations for A_{cm} and A_{dm}, let's look at CMR:**

$$CMR(dB) = 20\log_{10}\left(\frac{A_{dm}}{A_{cm}}\right) = 20\log_{10}\left(\frac{\frac{R_2}{R_1}\left(1-\frac{R_1+2R_2}{R_1+R_2}\times\frac{\varepsilon}{2}\right)}{\frac{R_2}{R_1+R_2}\times\varepsilon}\right)$$

- **If the imbalance is sufficiently small we can neglect its effect on A_{dm}**
- **With that and some algebra we find:**

$$CMR(dB) \cong 20\log_{10}\left(\frac{1+\frac{R_2}{R_1}}{\varepsilon}\right)$$

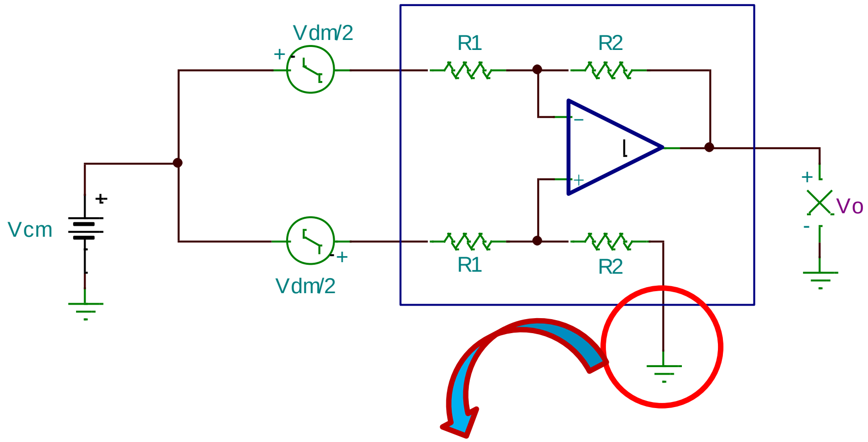
- **This equation shows two very important relationships**
  - **As the gain of a difference amplifier increases (R_2/R_1), CMR increases**
  - **As the mismatch (ε) increases, CMR decreases**

Please remember that this just shows the effects of the resistor network and assumes an ideal amplifier

Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

- **Another possible source for CMRR degradation is the impedance at the reference pin.**
- **So far we have connected this pin to low-impedance ground.**



- **Placing an impedance here will disturb the voltage divider we come across during superposition analysis.**
- **This will negatively affect CMR**

Common Mode Rejection Ratio (CMRR) (contd.)

CMRR of Difference Amplifiers

Pros:

- Difference amplifiers amplify differential signals and reject common-mode signals
- The common-mode rejection is based mainly on resistor matching
- Difference amplifiers can be used to protect against ground disturbances

Cons:

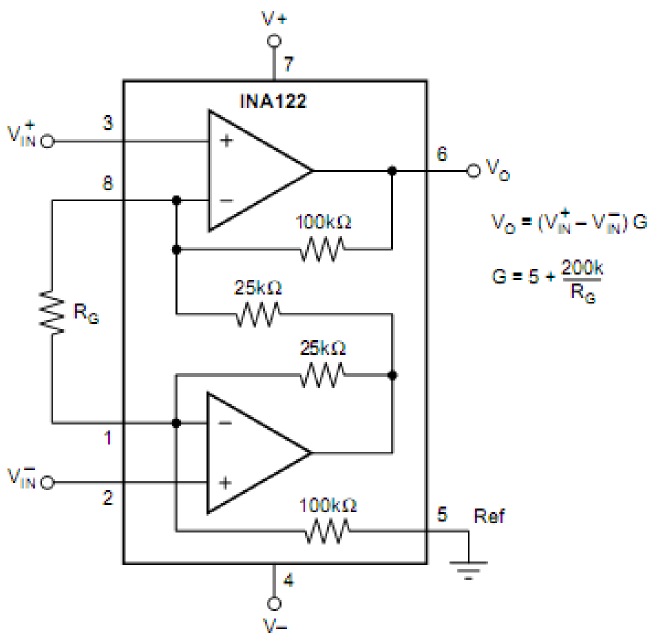
- Externally changing the gain of a difference amplifier is not worthwhile
- The input impedance is finite
  - This means that a difference amplifier will load the input signals
  - If the input signal source's impedances are not balanced, CMR could be degraded
- Is there a way we can amplify differential signals, change the gain, retain high CMR, and not load our source?
- Yes! Buffer the inputs…this creates an Instrumentation Amplifier (IA).

Common Mode Rejection Ratio (CMRR) (contd.)

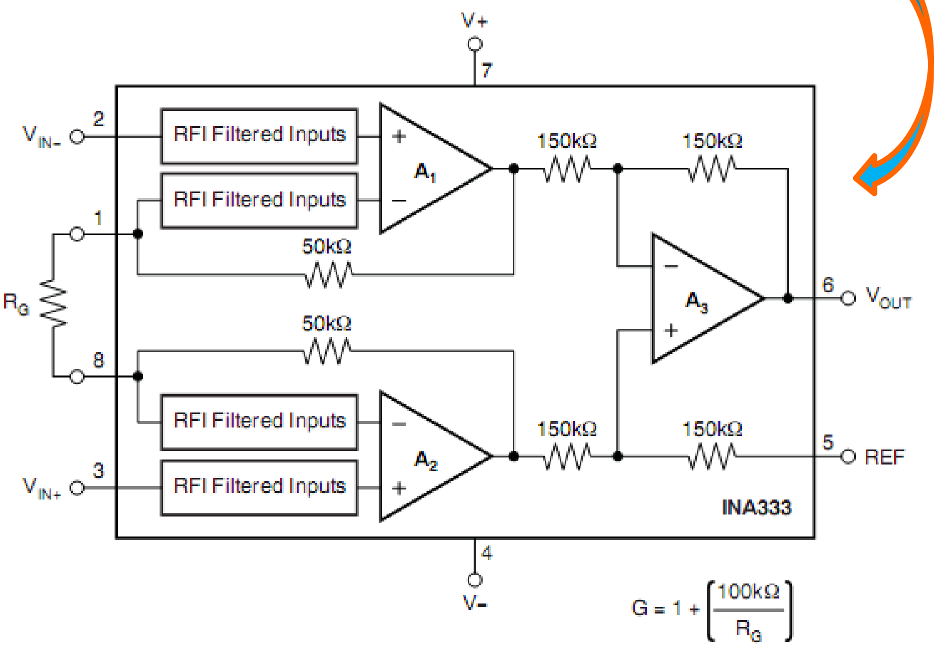
Instrumentation Amplifiers

There are 2 common types of instrumentation amplifiers

2 op-amp (e.g. INA122)



3 op-amp (e.g. INA333)



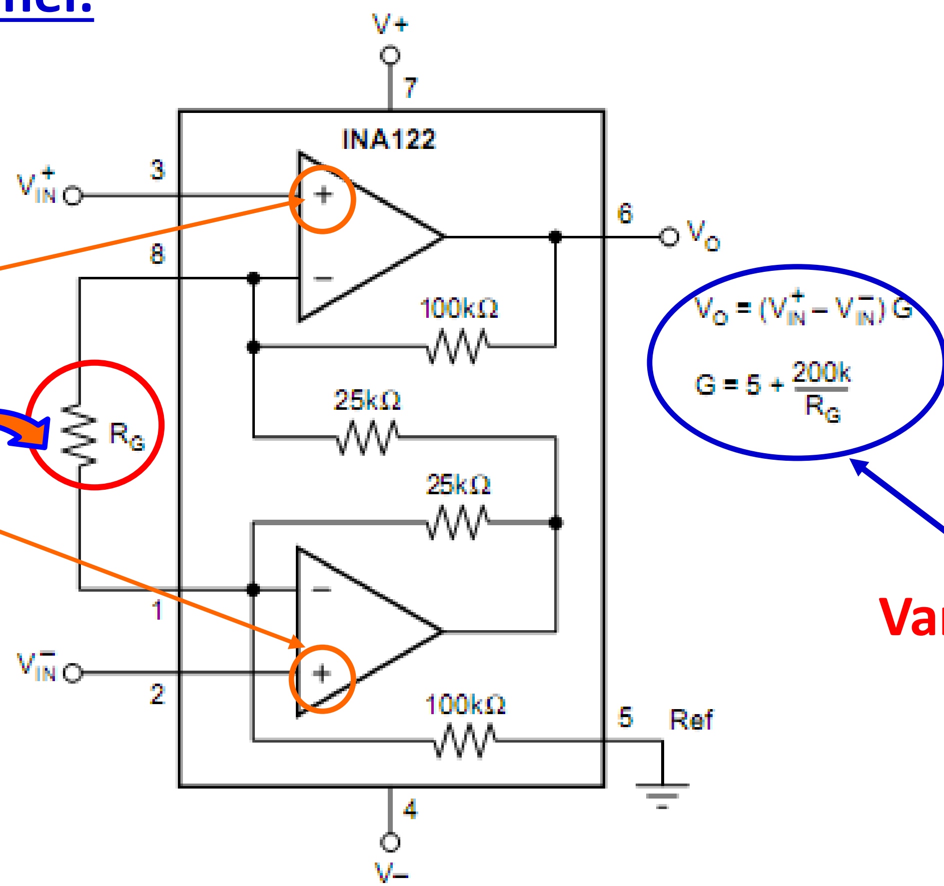
Common Mode Rejection Ratio (CMRR) (contd.)

Instrumentation Amplifiers

- Notice both have gain equations so you can vary the gain.
- Notice the input impedance is that of the non-inverting terminal of a non-inverting amplifier.

High-Z Nodes

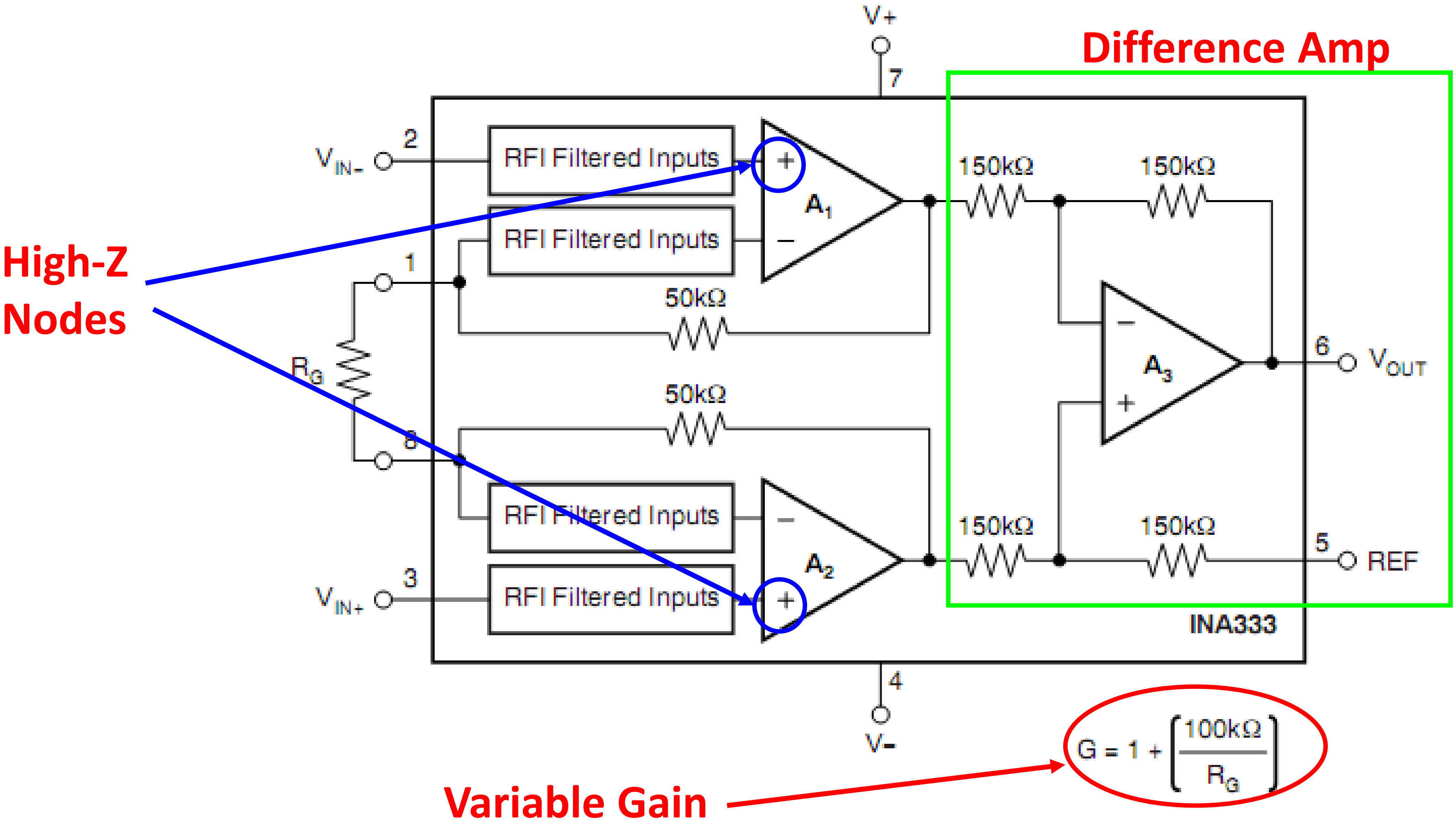
This varies gain



Variable Gain

Common Mode Rejection Ratio (CMRR) (contd.)

Instrumentation Amplifiers



Common Mode Rejection Ratio (CMRR) (contd.)

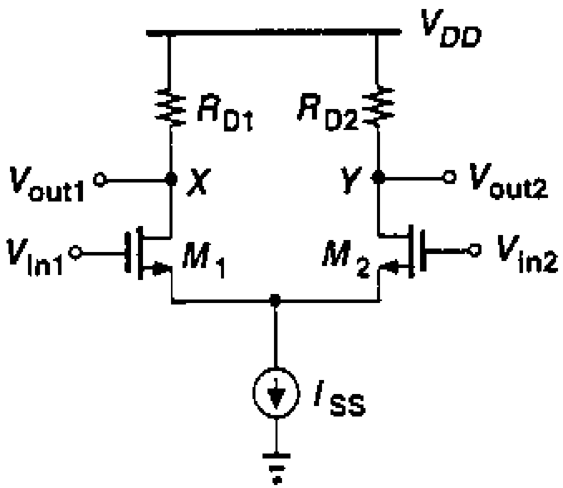
Instrumentation Amplifiers

- So, what is the CMRR of an instrumentation amplifier?
- Instrumentation amplifiers reject common-mode signals ($A_{cm} \rightarrow 0$)
- Recall: $$CMRR = \frac{A_{dm}}{A_{cm}}$$

CMRR is directly related to differential gain. Since we can change the differential gain of an IA, we also change the CMRR.

Non-ideal Characteristics of Differential Amplifier

- DC Offset Problems
- Due to mismatch in load resistances, mismatch in W/L, and mismatch in V_T



- Mismatch in R_D

$$R_{D1} = R_D + \frac{\Delta R_D}{2} \qquad R_{D2} = R_D - \frac{\Delta R_D}{2}$$

$$V_{ou1} = V_{DD} - \frac{I_{SS}}{2}\left(R_D + \frac{\Delta R_D}{2}\right)$$

$$V_{out2} = V_{DD} - \frac{I_{SS}}{2}\left(R_D - \frac{\Delta R_D}{2}\right)$$

- Therefore differential output:

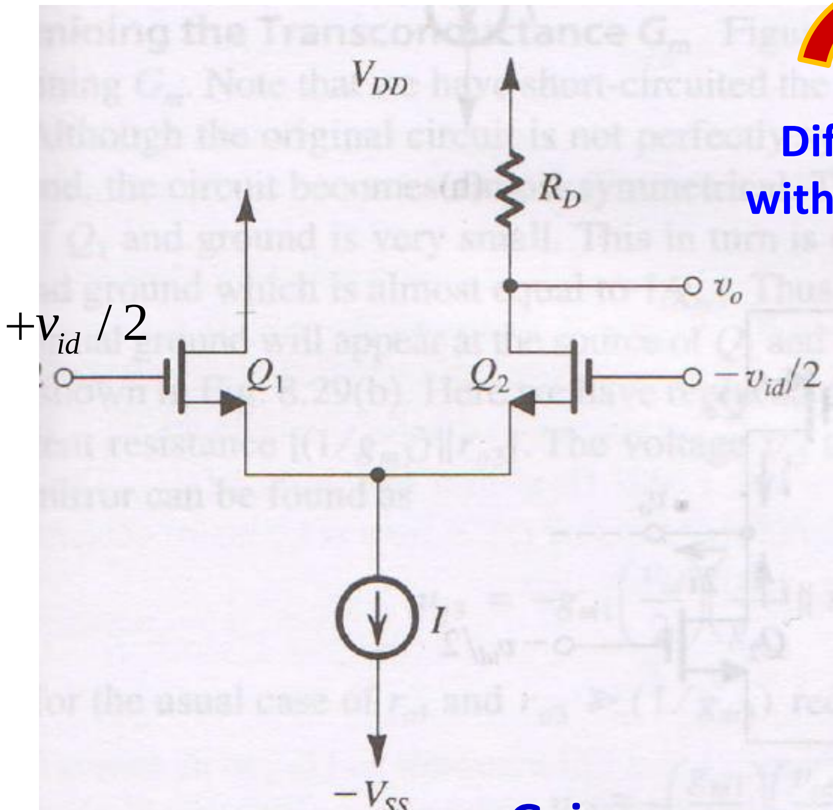
$$V_o = V_{out2} - V_{out1} = \left(\frac{I_{SS}}{2}\right)\Delta R_D$$

Non-zero ← Unwanted ← polarity unknown a priori

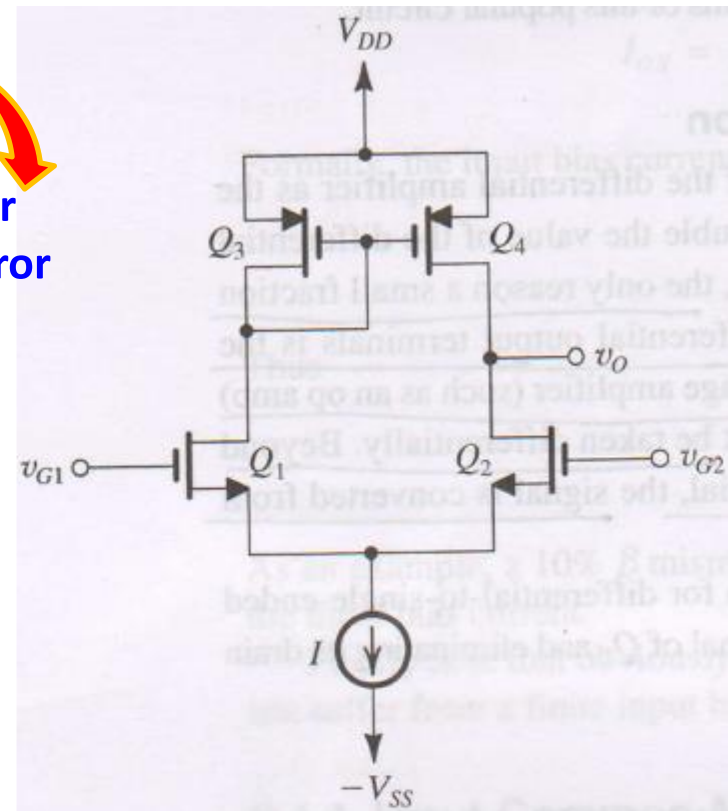
- Offset signal appears due to mismatch → differential can overcome this offset problem

Differential Amplifier with Active Load

- **However most systems are single-ended → require single ended signal → what is the solution?**



Differential pair with current mirror

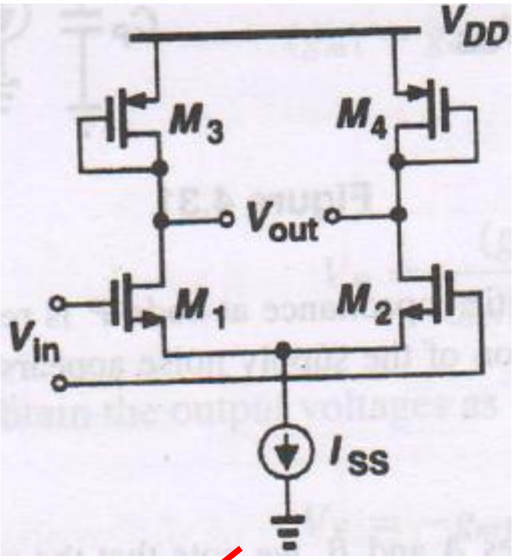


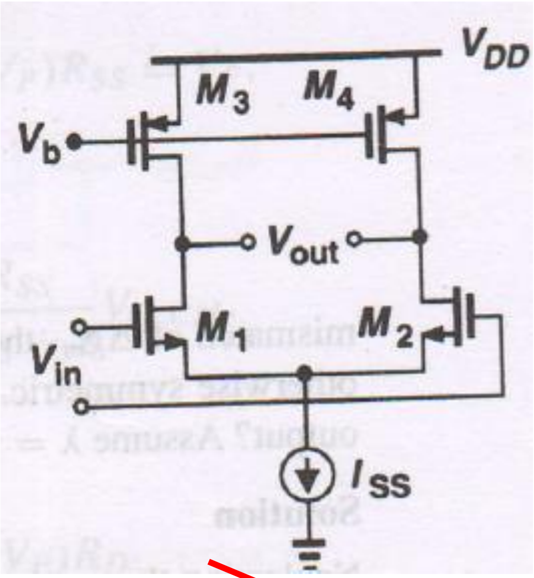
No. Why? → **Gain reduces to half**

Although this solves the problem but any mismatch in Q_3 and Q_4 will cause variations in the eventual output

Differential Pair with Active Loads

- It can help in mitigating the common-mode to differential conversion arising out from R_D mismatch.

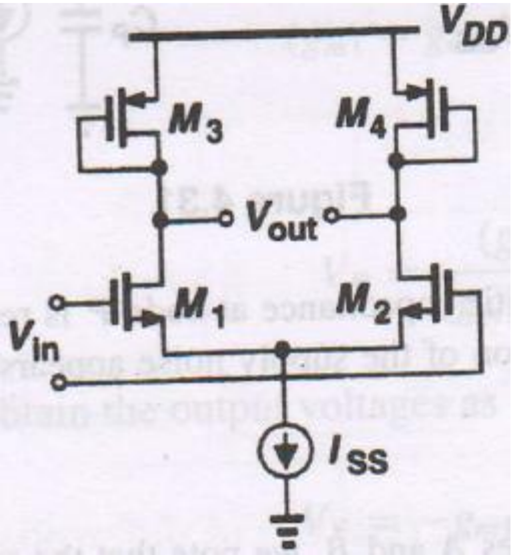




Its easier to define output CM level as M_3/M_4 are in saturation by default

M_3/M_4 are not in saturation by default & therefore output CM level not well defined

Differential Pair with Active Loads (contd.)



- Differential pair with ideal current source:

$$A_v = -\frac{\left(\frac{1}{g_{mP}}\right)}{\left(\frac{1}{g_{mN}}\right)} = -\frac{g_{mN}}{g_{mP}}$$

Dependence on scaling factor and process parameters

- Precision comes but with a price. What is that?

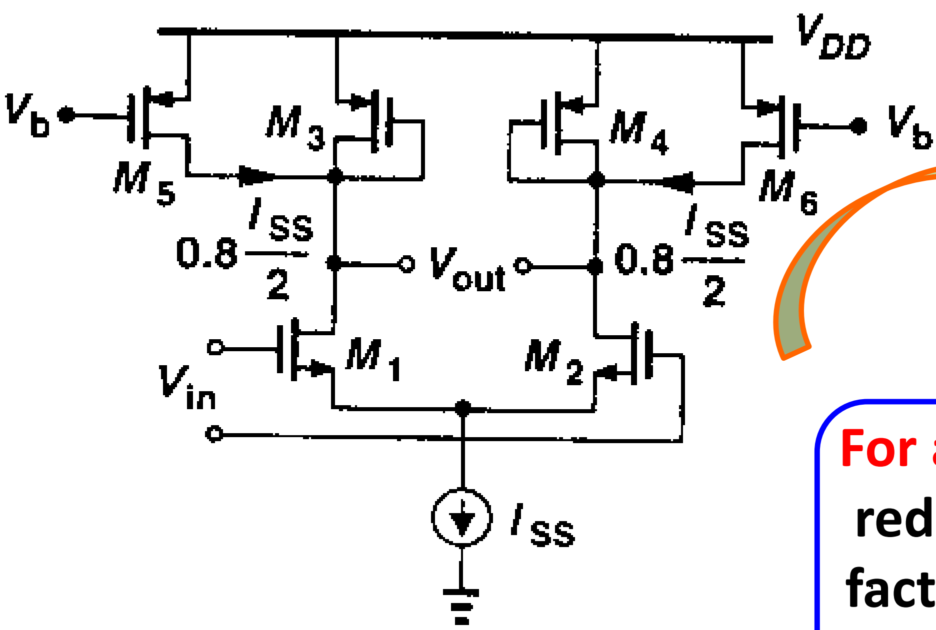
  - Reduced voltage swings

→ to increase gain → reduce $(W/L)_P$ → as a consequence V_{ov} of M_3/M_4 reduces → eventually lowers the CM level at the nodes X and Y → clipping in the negative cycle

Differential Pair with Active Loads (contd.)

Diode-connected Load:

- The output swing can be improved IF part of bias current to M_1 and M_2 can be provided by PMOS current sources
  - The trick here is to reduce the g_m of M_3 and M_4 by lowering their drain currents instead of their aspect ratios



Here, M_5 and M_6 carry 80% of M_1 and M_2 → the current through M_3 and M_4 is reduced by a factor of 5

For a given $|V_{GSP} - V_{TP}|$, this allows reduction in g_m of M_3 and M_4 by a factor of 5 ← potentially enhances the gain by a factor of 5

Differential Pair with Active Loads (contd.)

Constant Current Sources:

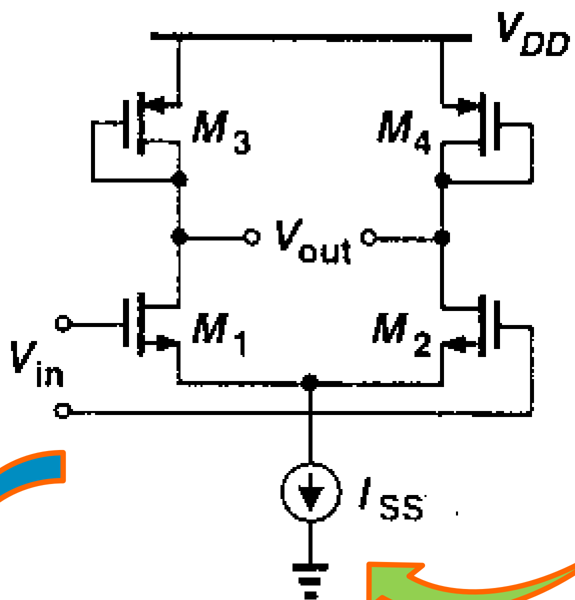
- The small signal gain of differential pair with current source load is usually in the range of 10 – 20.
- How to increase the gain?
- Use Cascode structure both for NFET and PFET

Cascode will definitely enhance the small signal gain BUT at the cost of reduced voltage headroom

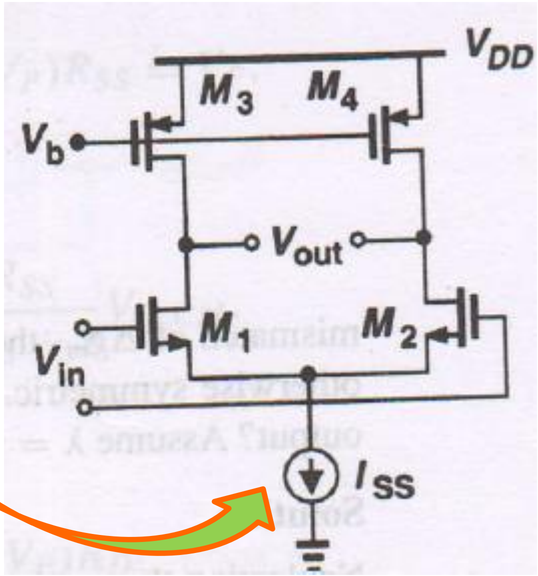
- By now we know, the load resistors in differential pair can be replaced by diode-connected or source-connected loads.
- It can help in mitigating the common-mode to differential conversion arising out from R_D mismatch.

Differential Pair with Active Load

- **Using half-circuit approach:**



Differential pair with ideal current source



$$A_v = -g_{mN}\left(g_{mP}^{-1} \parallel r_{oN} \parallel r_{oP}\right)$$

$$A_v = -g_{mN}\left(r_{oN} \parallel r_{oP}\right)$$

$$\therefore A_v \approx -\frac{g_{mN}}{g_{mP}} = -\sqrt{\frac{\mu_n (W/L)_N}{\mu_P (W/L)_P}}$$