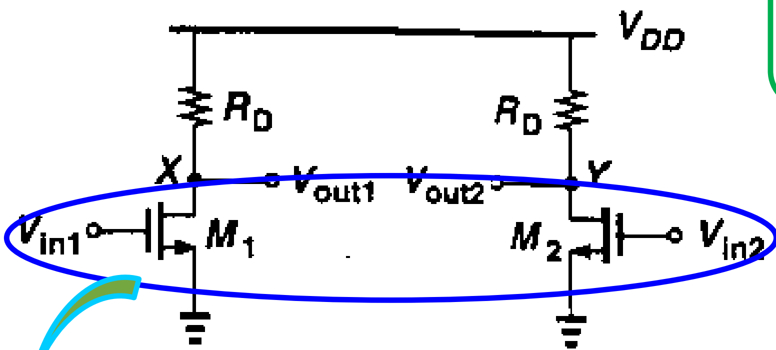
Lecture – 11 **Date: 15.09.2016**

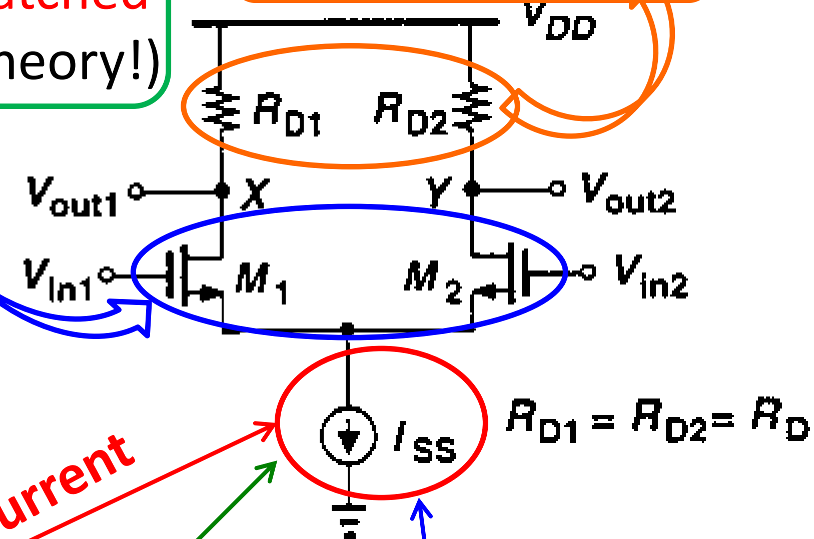
- MOS Differential Pair
- Quantitative Analysis – differential input
- Small Signal Analysis

MOS Differential Pair



M_1 and M_2 are perfectly matched (at least in theory!)

ensures M_1 and M_2 in saturation



Variation of input CM level regulates the bias currents of M_1 and M_2 → Undesired!!!

Solution??

Tail Current

Need?

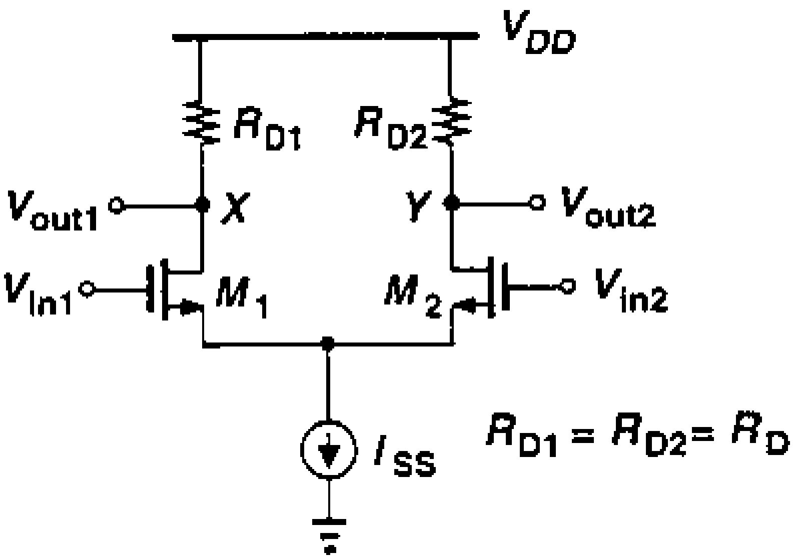
Current source is ideal: constant current, infinite output impedance

To overcome the issues emanating from non-ideal CM level

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from -∞ to ∞

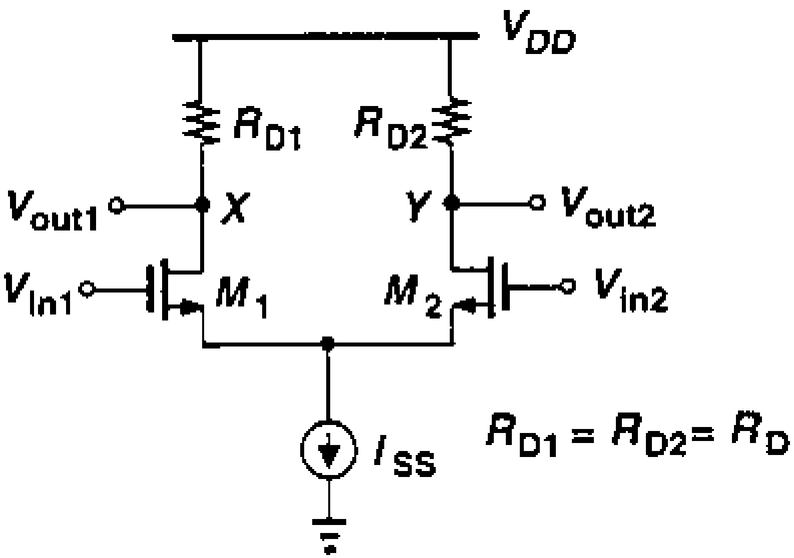


- V_{in1} is much more –ve than V_{in2} then:
    - M_1 if OFF and M_2 is ON
    - $I_{D2} = I_{SS}$
    - $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - I_{SS}R_D$
- V_{in1} is brought closer to V_{in2} then:
    - M_1 gradually turns ON and M_2 is ON
        - Draws a fraction of I_{SS} and lowers V_{out1}
    - I_{D2} decreases and V_{out2} rises
- $V_{in1} = V_{in2}$
    - $V_{out1} = V_{out2} = V_{DD} - I_{SS}R_D/2$

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from $-\infty$ to ∞



- V_{in1} becomes more +ve than V_{in2} then:
  - M_1 if ON and M_2 is ON
  - M_1 carries greater I_{SS} than M_2
- For sufficiently large $V_{in1} - V_{in2}$:
  - All of the I_{SS} goes through M_1 → M_2 is OFF
  - $V_{out1} = V_{DD} - I_{SS}R_D$ and $V_{out2} = V_{DD}$

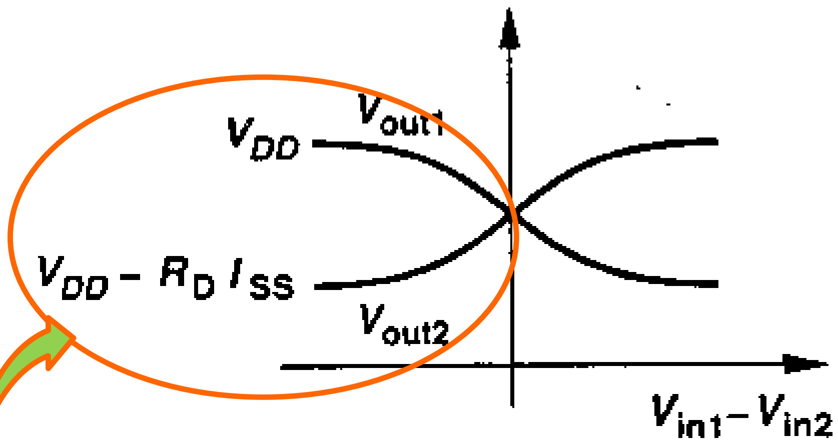
MOS Differential Pair

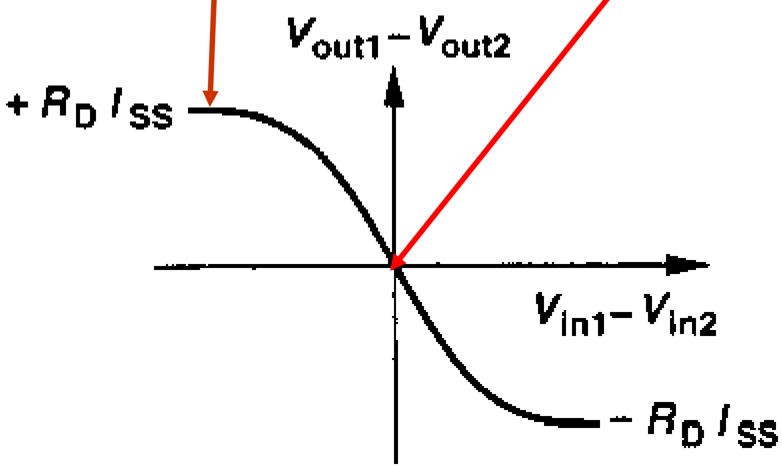
Qualitative Analysis – differential input

- Plotting $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$

Minimum Slope ↔ Minimum Gain

Maximum Slope ↔Maximum Gain





The maximum and minimum levels at the output are well defined and is independent of input CM level ($V_{in,cm}$)

The circuit becomes more nonlinear as the input voltage swing increases (i.e., $V_{in1} - V_{in2}$ increases) ↔ at $V_{in1} = V_{in2}$, the circuit is said to be in equilibrium

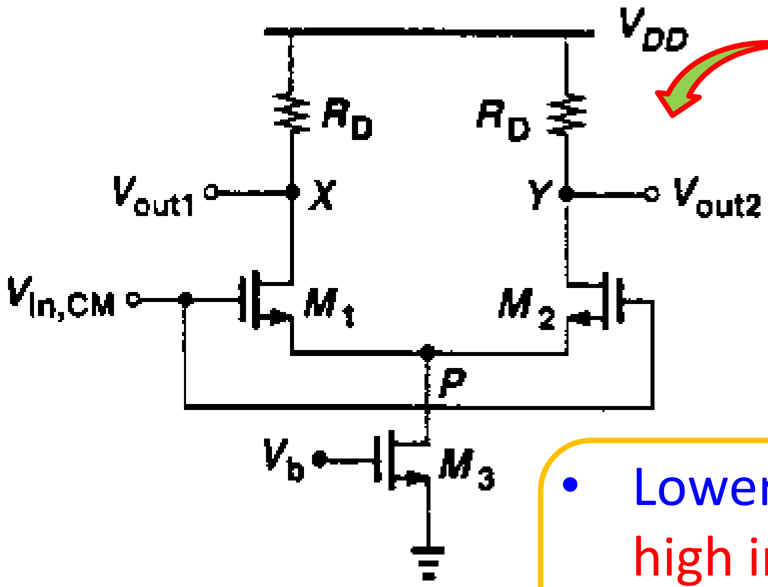
MOS Differential Pair

Qualitative Analysis – common mode input

- Now let us consider the common mode behavior of the circuit

As mentioned, the tail current source is used to suppress the effect of input CM level variation ($V_{in,cm}$)

Does this enable us to set any arbitrary level of input CM ($V_{in,cm}$)



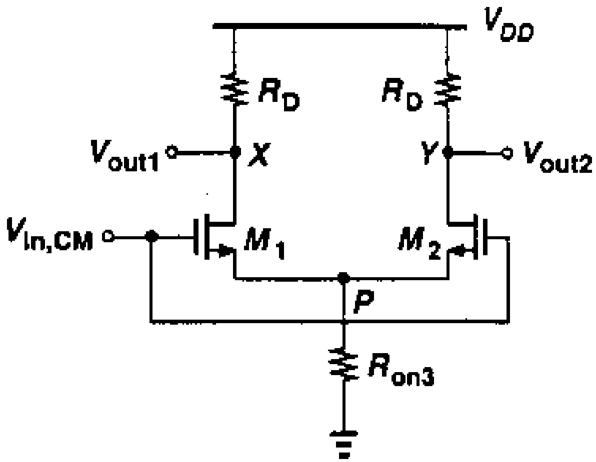
To understand this:

- Set $V_{in1} = V_{in2} = V_{in,CM}$
- Then vary $V_{in,CM}$ from 0 to V_{DD}
- Also implement I_{SS} with an NFET

- Lower bound of $V_{in,cm}$: V_P should be sufficiently high in order for M_3 to act as a current source.
- Upper bound of $V_{in, cm}$: M_1 and M_2 need to remain in saturation.

MOS Differential Pair

Qualitative Analysis – common mode input



- What happens when $V_{in,CM} = 0$?
  - M_1 and M_2 will be OFF and M_3 can be in triode for high enough V_b
  - $I_{D1} = I_{D2} = 0$ ← circuit is incapable of amplification
- Now suppose $V_{in,CM}$ becomes more +ve
  - M_1 and M_2 will turn ON if $V_{in,CM}$ exceeds V_T
  - I_{D1} and I_{D2} will continue to rise with the increase in $V_{in,CM}$
  - V_P will track $V_{in,CM}$ as M_1 and M_2 work like a source follower
  - For high enough $V_{in,CM}$, M_3 will be in saturation as well
- If $V_{in,CM}$ rises further
  - M_1 and M_2 will remain in saturation if:

$$V_{in,CM} - V_T \le V_{out1} \Rightarrow V_{in,CM} \le V_{DD} - \frac{I_{SS}}{2} R_D + V_T$$

MOS Differential Pair

Qualitative Analysis – common mode input

- For M_1 and M_2 to remain in saturation:

$$V_{GS1,2} - V_T \le V_{DS1,2} \quad \Rightarrow V_{in,CM} - V_T \le V_{DD} - \frac{I_{SS}}{2} R_D \quad \Rightarrow V_{in,CM} \le V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

$$\therefore (V_{in,CM})_{\max} = V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

- The lowest value of $V_{in,CM}$ is determined by the need to keep the constant current source operational:

$$V_{in,CM} - V_{GS1,2} \ge V_{GS3} - V_T$$

$$\Rightarrow V_{in,CM} \ge V_{GS1,2} + (V_{GS3} - V_{T3})$$

$$V_{GS1,2} + (V_{GS3} - V_T) \le V_{in,CM} \le \min\left[V_{DD} - \frac{I_{SS}}{2} R_D + V_T, V_{DD} \right]$$

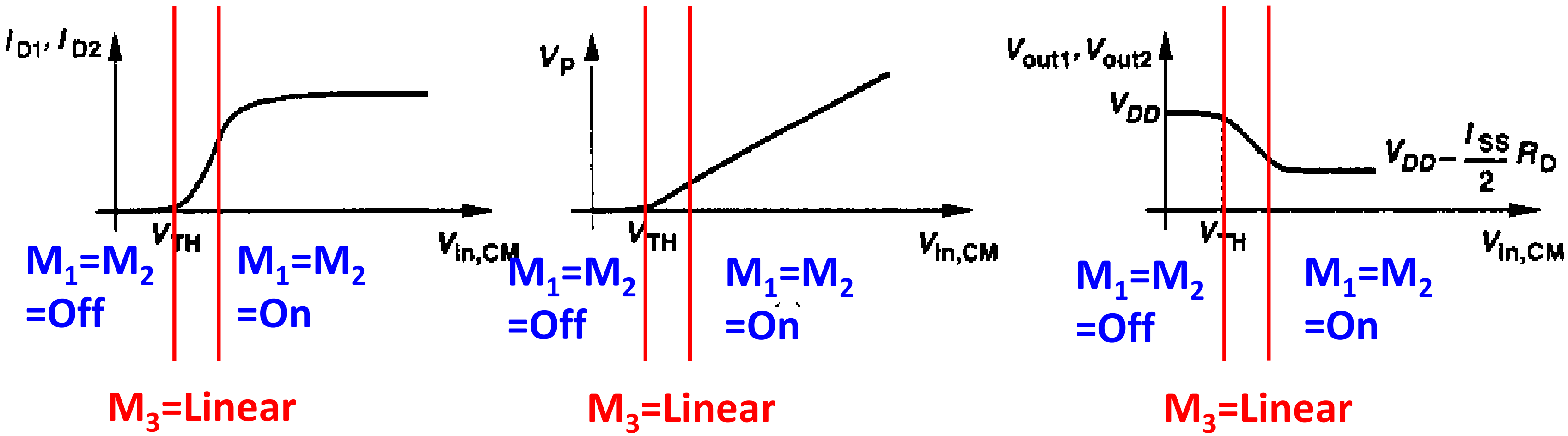
MOS Differential Pair

Qualitative Analysis – common mode input

- Thus, $V_{in,CM}$ is bounded as:

$$V_{GS1,2} + (V_{GS3} - V_T) \le V_{in,CM} \le \min\left[V_{DD} - \frac{I_{SS}}{2}R_D + V_T, V_{DD}\right]$$

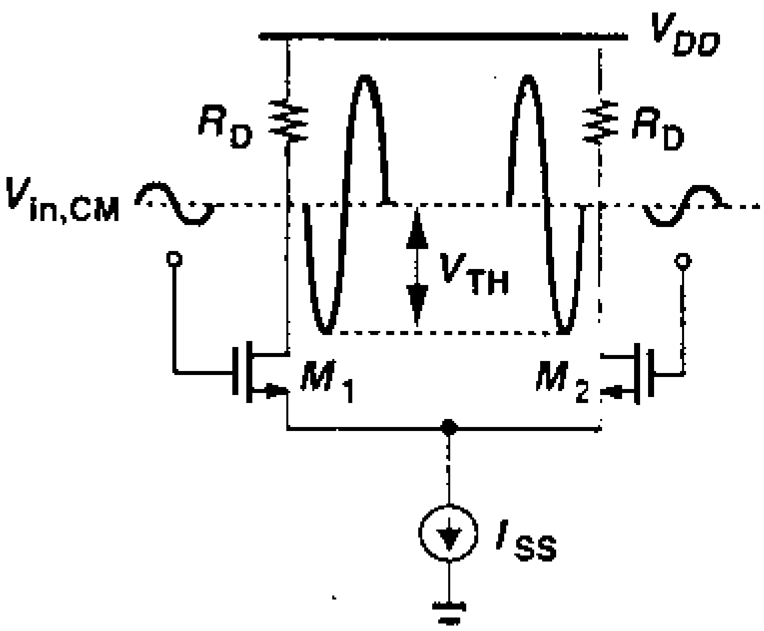
- Summary:



MOS Differential Pair

Qualitative Analysis – common mode input

- How large can the output voltage swings of a differential pair be?



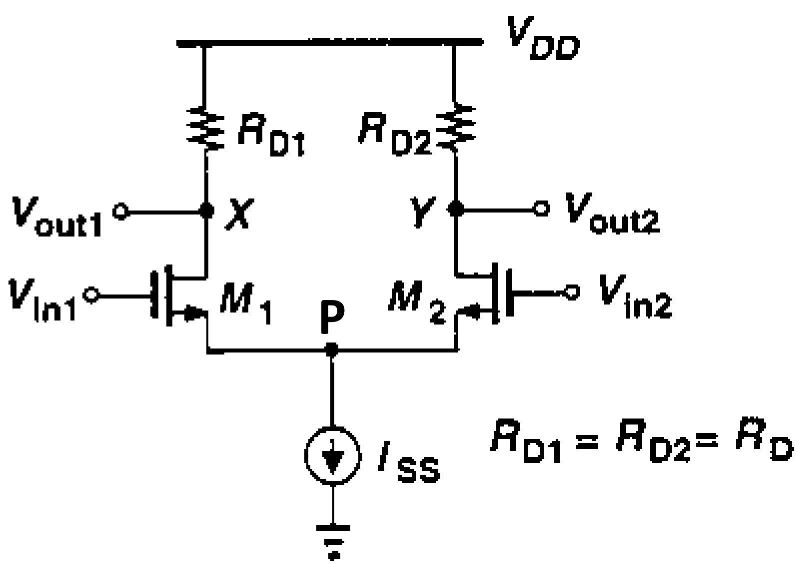
$$V_{out,\max} = V_{DD}$$

$$V_{out,\min} = V_{in,CM} - V_T$$

The higher the input CM level, the smaller the allowable output swings.

MOS Differential Pair

Quantitative Analysis – differential input



For +ve V_{in1} → V_{GS1} is greater than V_{GS2} → I_{D1} will be greater than I_{D2}

$$V_{out2}(=V_{DD} - I_{D2}R_D) > V_{out1}(=V_{DD} - I_{D1}R_D)$$

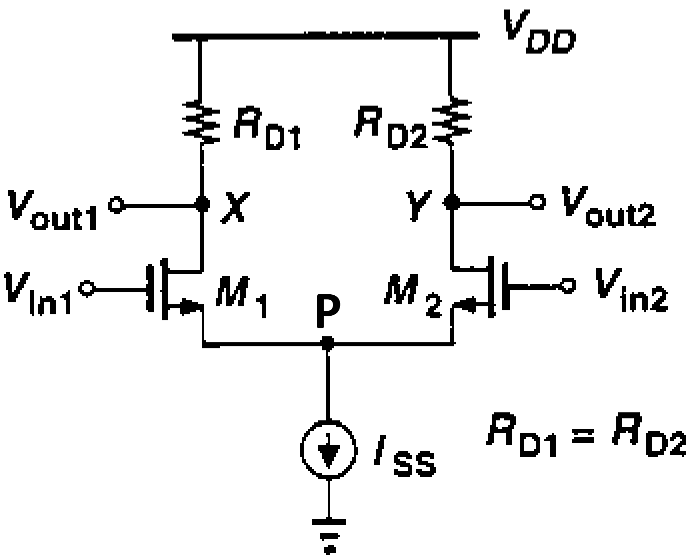
For +ve V_{in2} → V_{GS2} is greater than V_{GS1} → I_{D2} will be greater than I_{D1}

$$V_{out1}(=V_{DD} - I_{D1}R_D) > V_{out2}(=V_{DD} - I_{D2}R_D)$$

It is thus apparent that the differential pair respond to differential-mode signals → by providing differential output signal between the two drains

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input



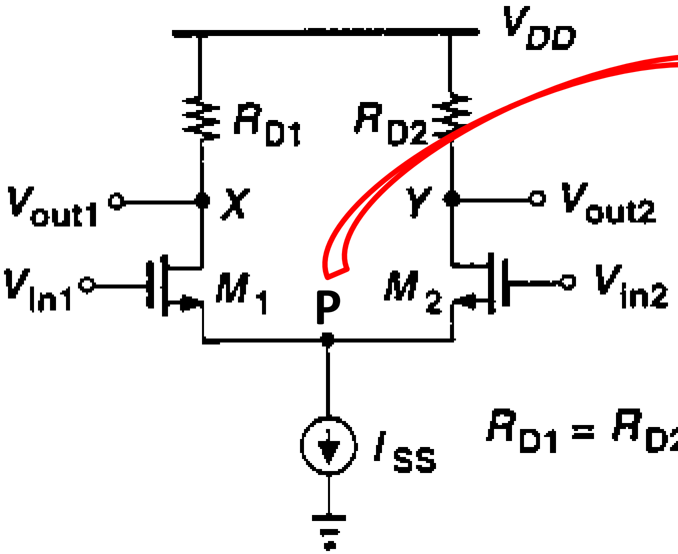
$R_{D1} = R_{D2} = R_D$

- The idea is to define I_{D1} and I_{D2} in terms of input differential signal $V_{in1} - V_{in2}$
- The circuit doesn't include connection details considering that these drain current equations do not depend on the external circuitries

- Assumptions: M_1 and M_2 are always in saturation; differential pair is perfectly matched; channel length modulation is not present

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input



$$V_P = V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

$$\therefore V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

We also know:

$R_{D1} = R_{D2} = R_D$

$$(V_{GS} - V_T)^2 = \frac{2I_D}{\mu_n C_{ox}\frac{W}{L}} \quad \Rightarrow V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} + V_T$$

Therefore:

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}\frac{W}{L}}}$$

Squaring

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{D1} + I_{D2} - 2\sqrt{I_{D1} I_{D2}}\right)$$

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

$$(V_{in1}-V_{in2})^2=\frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{D1}+I_{D2}-2\sqrt{I_{D1}I_{D2}}\right)$$

$I_{D1}+I_{D2}=I_{SS}$

$$\therefore (V_{in1}-V_{in2})^2=\frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{SS}-2\sqrt{I_{D1}I_{D2}}\right)$$

$$\frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)(V_{in1}-V_{in2})^2-I_{SS}=-2\sqrt{I_{D1}I_{D2}}$$

Squaring

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4+I_{SS}^2-I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2=4I_{D1}I_{D2}$$

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4+I_{SS}^2-I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2=(I_{D1}+I_{D2})^2-(I_{D1}-I_{D2})^2$$

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

$$(I_{D1}-I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1}-V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2$$

$$I_{D1}-I_{D2} = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)(V_{in1}-V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}-(V_{in1}-V_{in2})^2}$$

Observations

- $I_{D1} - I_{D2}$ falls to zero for $V_{in1} = V_{in2}$ and $|I_{D1} - I_{D2}|$ increases with increase in $|V_{in1} - V_{in2}|$
- Therefore, $I_{D1} - I_{D2}$ is an odd function of $V_{in1} - V_{in2}$
- Its important to notice that I_{D1} and I_{D2} are even functions of their respective gate-source voltage

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

- **Equivalent G_m of M_1 and M_2 → its effectively the slope of the characteristics**

Lets denote: $I_{D1} - I_{D2} = \Delta I_D$

$V_{in1} - V_{in2} = \Delta V_{in}$

$$\Delta I_D = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\Delta V_{in}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}$$

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\frac{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

For $\Delta V_{in} = 0$: $G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}$

Furthermore: $V_{out1} - V_{out2} = R_D \Delta I = R_D G_m \Delta V_{in}$

$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}\, R_D$$

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

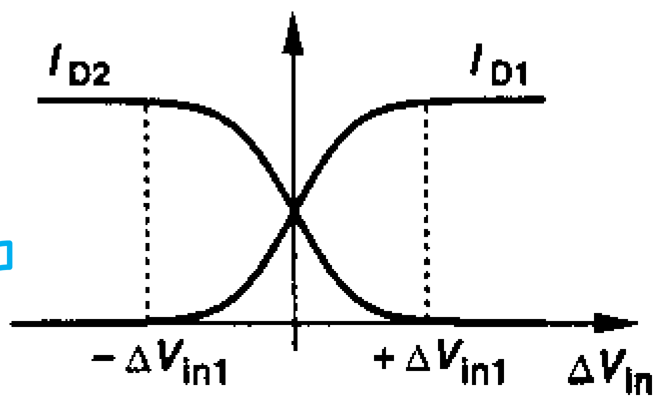
$$G_m = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\frac{\dfrac{\dfrac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{}}{\sqrt{\dfrac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

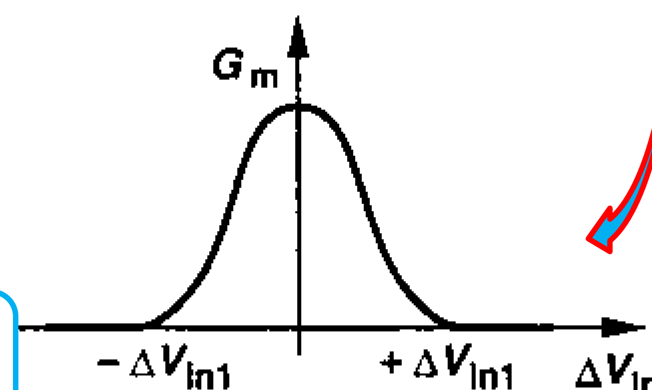
G_m falls to zero for

ΔV_{in1}

$$\Delta V_{in} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

ΔV_{in1} represents the maximum differential signal a differential pair can handle.

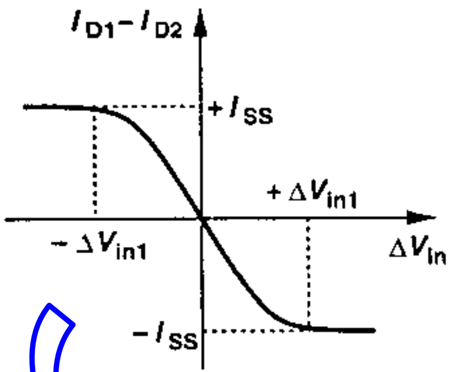




Beyond $|\Delta V_{in1}|$, only one transistor is ON and therefore draws all of the I_{SS}

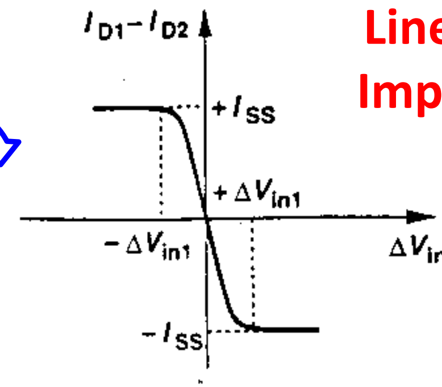
Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input



I_{SS} Constant

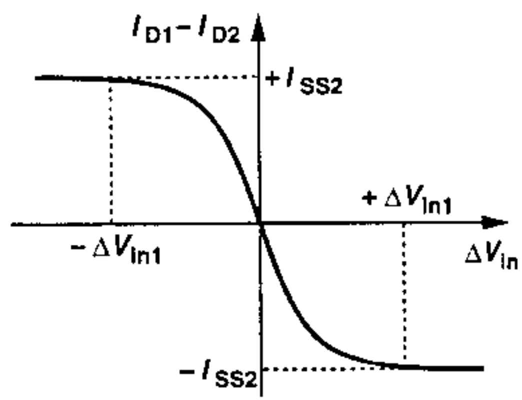
Reduce ΔV_{in1} → by increasing W/L



Linearity Improves

W/L Constant

Increase ΔV_{in1} → by increasing I_{SS}



Linearity Improves

Linearity of a differential pair can be improved by decreasing W/L and/or increasing I_{SS}

MOS Differential Pair – small signal analysis

Quantitative Analysis – differential input

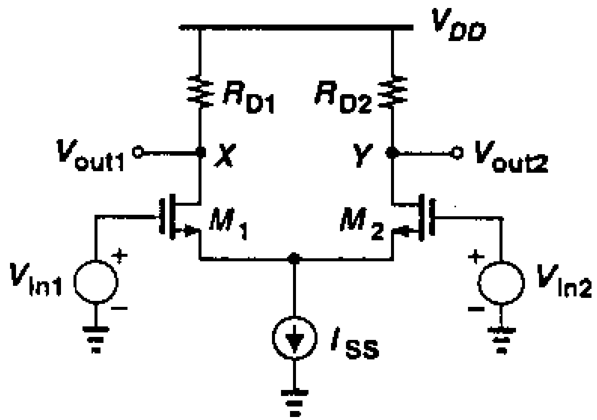
- From large signal analysis we achieved:

$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} R_D$$

At equilibrium, this is g_m

$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = g_m R_D$$

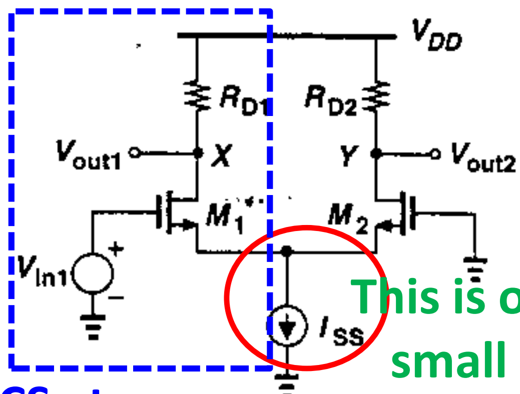
- We apply small signals to V_{in1} and V_{in2} and assume M_1 and M_2 are already operating in saturation.



- How to arrive at this result using small signal analysis?
  - Two techniques
    - Superposition method
    - Half-circuit concept

MOS Differential Pair – small signal analysis

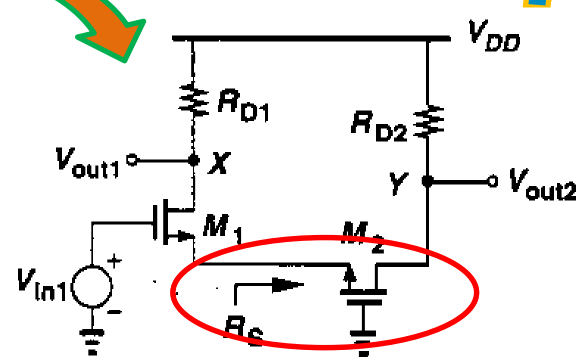
- Method-I: Superposition technique – the idea is to see the effect of V_{in1} and V_{in2} on the output and then combine to get the differential small signal voltage gain
- First set, $V_{in2} = 0$
- Then let us calculate V_X/V_{in1}

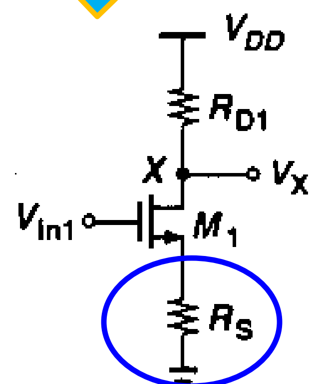


CS-stage

This is open for small signal analysis

Simplified Circuit





Input impedance of M_2 Provides degeneration resistance to CS-stage of M_1

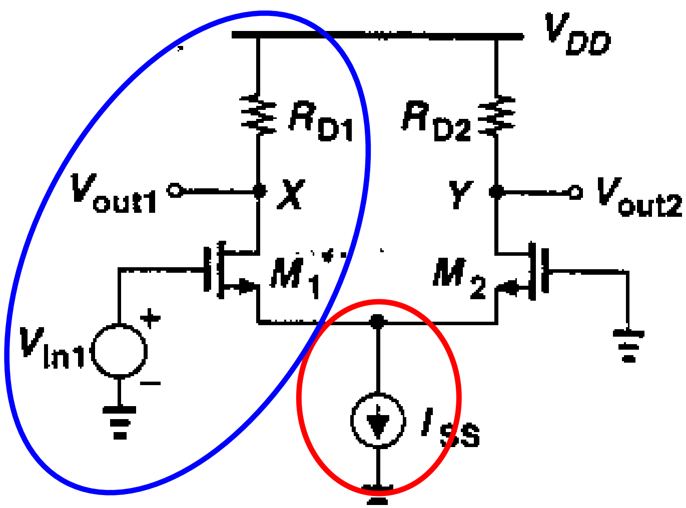
$$\frac{1}{g_{m1}} + \frac{1}{g_{m2}}$$

$$\frac{V_X}{V_{in1}} = \frac{-R_{D1}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$\therefore \frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

MOS Differential Pair – small signal analysis

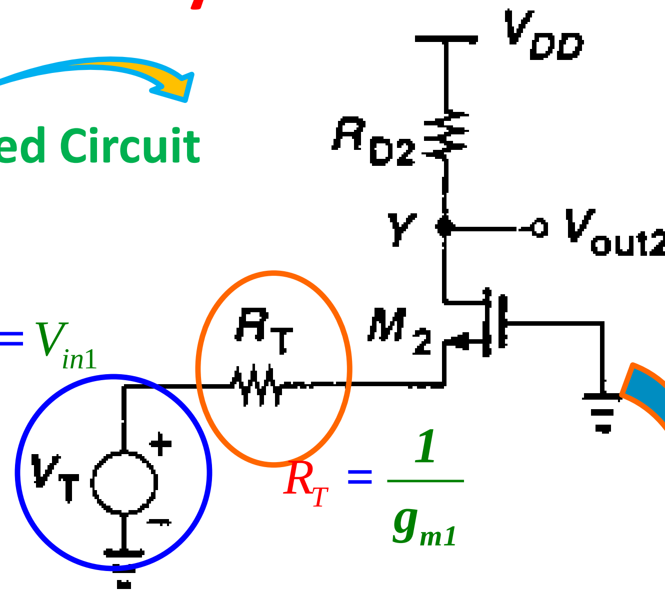
- **Superposition technique**
  - **Now calculate V_Y/V_{in1}**



Replace M_1 by its Thevenin Equivalent Circuit

This is open for small signal analysis

Simplified Circuit



CG-Stage

$$\therefore \frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

- **combine the expressions to calculate small signal voltage only due to V_{in1}**

$$\frac{(V_X - V_Y)|_{due\_to\_V_{in1}}}{V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

MOS Differential Pair – small signal analysis

For matched transistors: $(V_X - V_Y)|_{due\_to\_V_{in1}} = -g_m R_D V_{in1}$

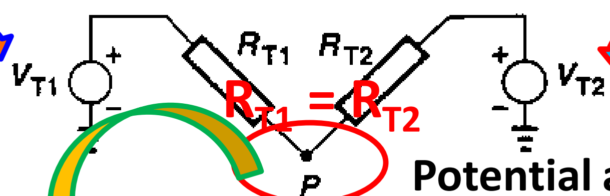
- **Similarly:** $(V_X - V_Y)|_{due\_to\_V_{in2}} = g_m R_D V_{in2}$

- **Superposition gives:** $A_v = \dfrac{(V_X - V_Y)_{total}}{V_{in2} - V_{in1}} = -g_m R_D$

- **The magnitude of differential gain is $g_m R_D$ regardless of how the inputs are applied**
- **The gain will be halved if single ended output is considered**

- **Half Circuit Approach**
  - If a fully symmetric differential pair senses differential inputs (i.e, the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of half circuit can be applied.

Change this by ΔV_T



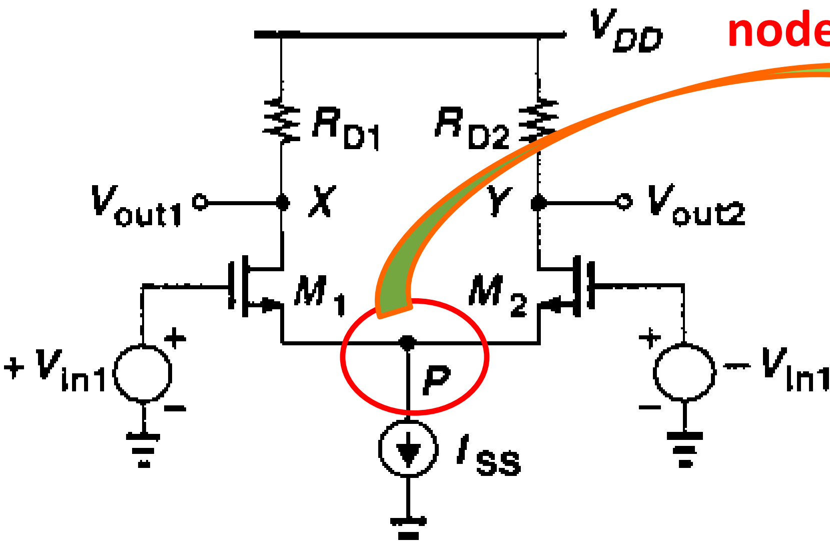
Change this by $-\Delta V_T$

Node is said to be ac-grounded

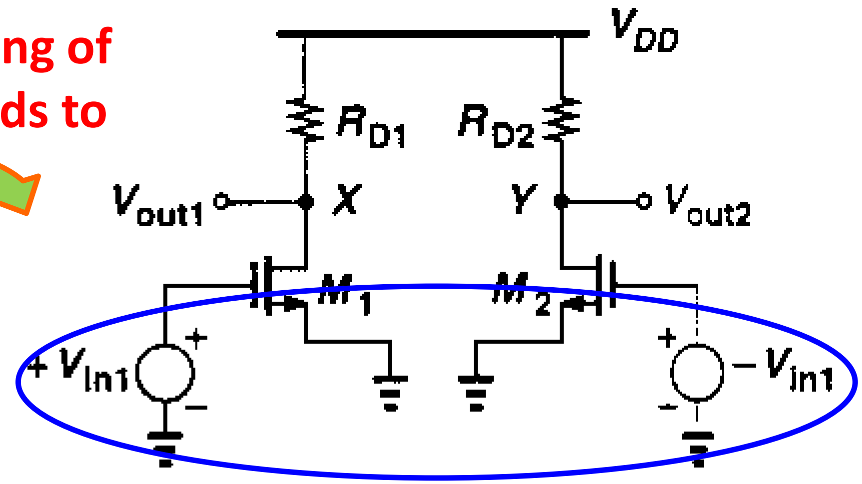
Potential at node P will remain unchanged

MOS Differential Pair – small signal analysis

- **Half Circuit Approach**



Ac grounding of node P leads to



V_{in1} and $-V_{in1}$ are the change in input voltage at each side

We can write:

$$\frac{V_X}{V_{in1}} = -g_m R_D$$

$$\frac{V_Y}{-V_{in1}} = -g_m R_D$$

Therefore the differential output can be expressed as:

$$V_X - V_Y = 2V_{in1}\left(-g_m R_D\right)$$

Thus the small signal voltage given is:

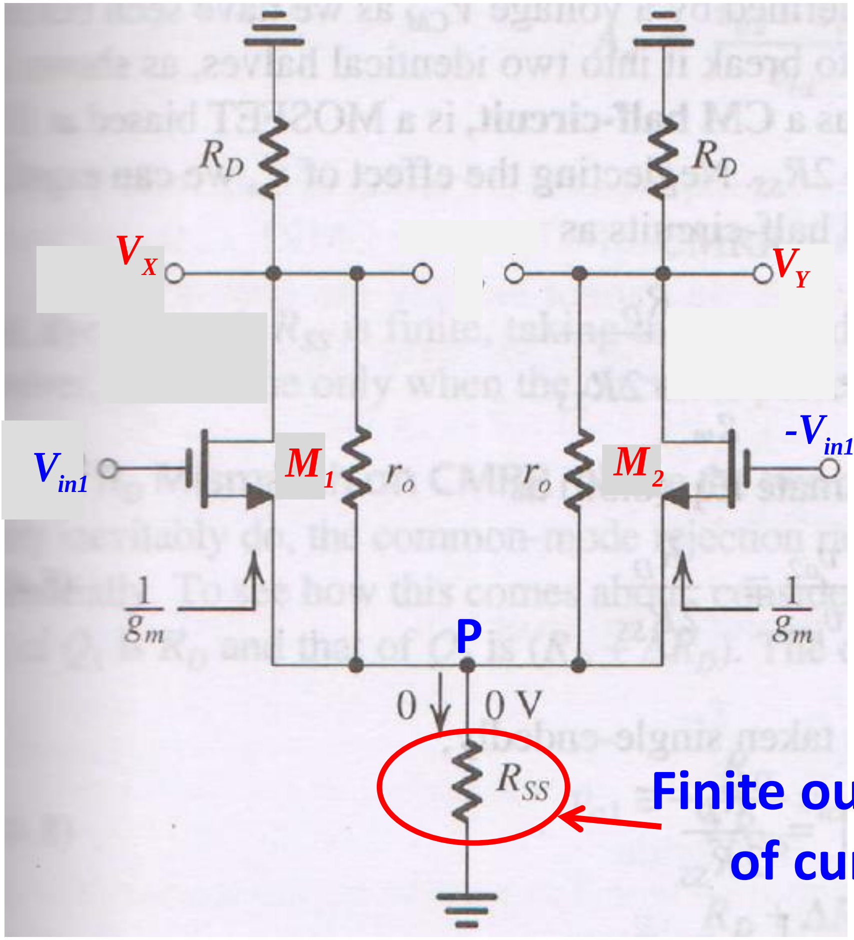
$$A_v = \frac{V_X - V_Y}{2V_{in1}} = -g_m R_D$$

MOS Differential Pair – small signal analysis

- How does the gain of a differential amplifier compare with a CS stage?
  - For a given total bias current I_{SS}, the value of equivalent g_m of a differential pair is $^1/_{\sqrt{2}}$ times that of g_m of a single transistor biased at the I_{SS} with the same dimensions. Thus the total gain is proportionally less.
  - Equivalently, for given device dimensions and load impedance, a differential pair achieves the same gain as a CS stage at the cost of twice the bias current.
- What is the advantage of differential stage then?
  - Definitely the noise suppression capability. Right?

MOS Differential Pair – small signal analysis

- **How is gain affected if channel length modulation is considered?**



Finite output resistance of current source

- **Effect of r_0 on the gain**

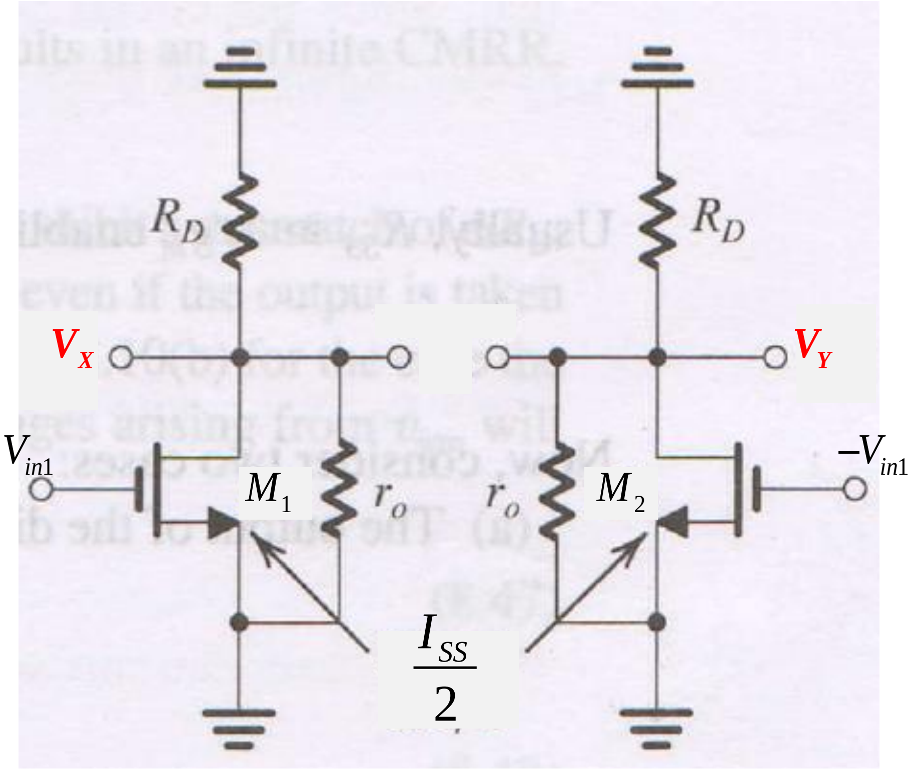
→ the circuit is still symmetric → the voltage at node P will be zero

No current through R_{SS}

R_{SS} plays no role in differential gain

MOS Differential Pair – small signal analysis

- The virtual ground on the source allows division of two identical CS amplifiers: → differential half circuits



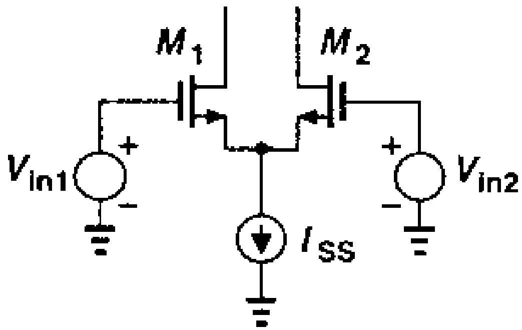
$$V_X = -g_m V_{in1}\left(R_D \,||\, r_o\right)$$

$$V_Y = g_m V_{in1}\left(R_D \,||\, r_o\right)$$

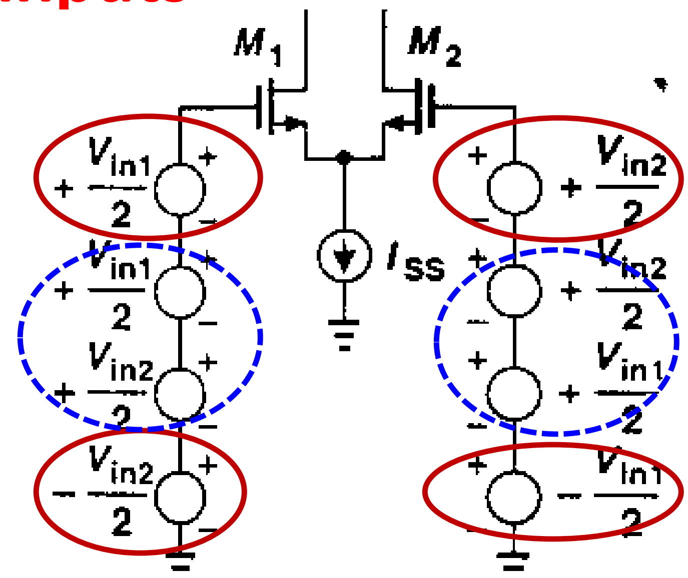
$$\Rightarrow V_X - V_Y = -g_m\left(2V_{in1}\right)\left(R_D \,||\, r_o\right)$$

$$\therefore A_v = \frac{V_X - V_Y}{2V_{in1}} = -g_m\left(R_D \,||\, r_o\right)$$

Small signal analysis – asymmetric inputs

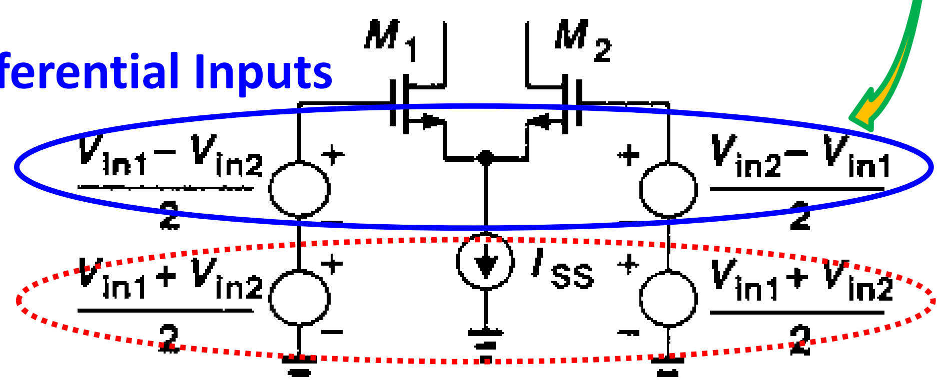


Transform the inputs as

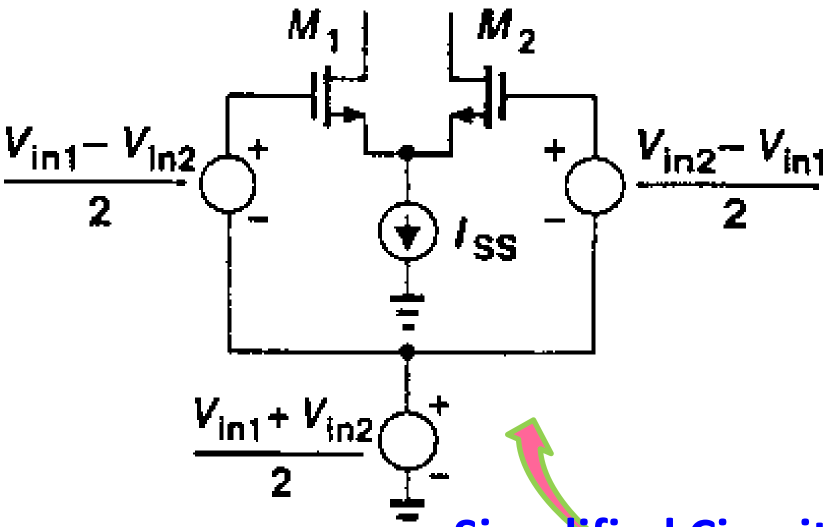


Simplify

Differential Inputs

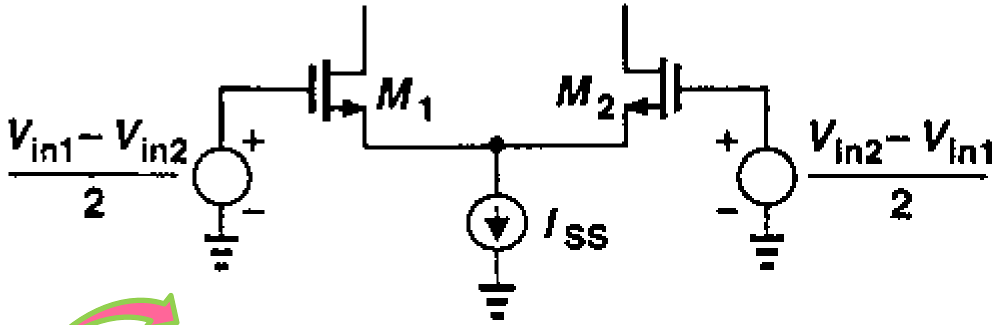


Common Mode Inputs



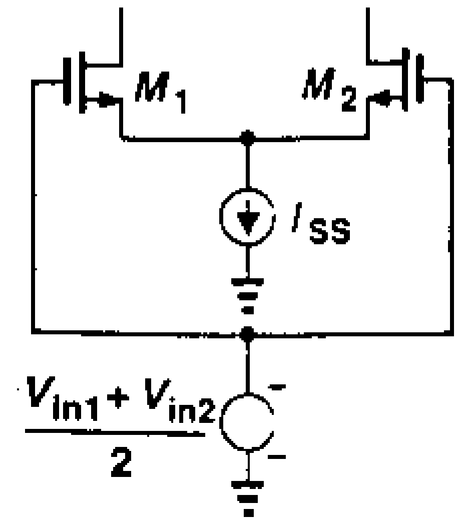
Simplified Circuit

Small signal analysis – asymmetric inputs



Circuit for Differential Mode

$$V_X - V_Y = -g_m \left(R_D \parallel r_o\right)\left(V_{in1} - V_{in2}\right)$$



Circuit for Common Mode

If the circuit is fully symmetric and I_{SS} is ideal current source, then M_1 and M_2 draws half of I_{SS} and is independent of $V_{in,CM}$. The V_X and V_Y experience no change as $V_{in,CM}$ varies. In essence, the circuit simply amplifies the difference between V_{in1} and V_{in2} while eliminating the effect of $V_{in,CM}$.