Lecture – 10 **Date: 12.09.2016**

- Differential Amplifier
- Differential Signaling
- Advantage of Differential Signaling
- MOS Differential Pair

Differential Amplifier

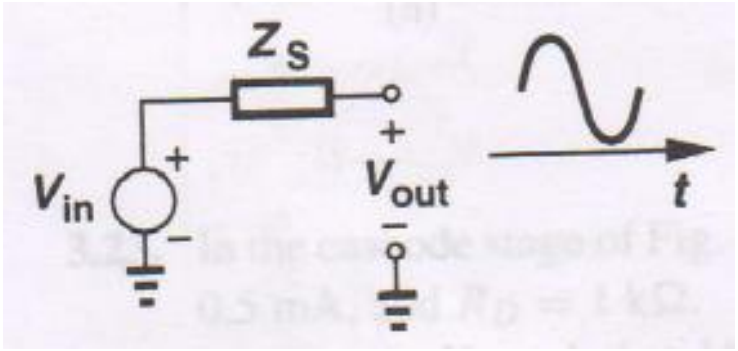
- **Why differential?**
- What do we want from an amplifier?
  - robust operation → free from external effects such as noise
  - High output voltage swing → optimal headroom / legroom
  - High gain → such as cascode configuration
  - Linear Performance
- Differential amplifiers exhibit/provide following features:
  - robust operation → noise do not affect its performance
  - Higher output voltage swing
  - Higher gain in comparison to single-stage amplifiers
  - Linear Performance and simpler biasing

Major Drawback: more area on a chip (however not always true!)

Differential Signaling

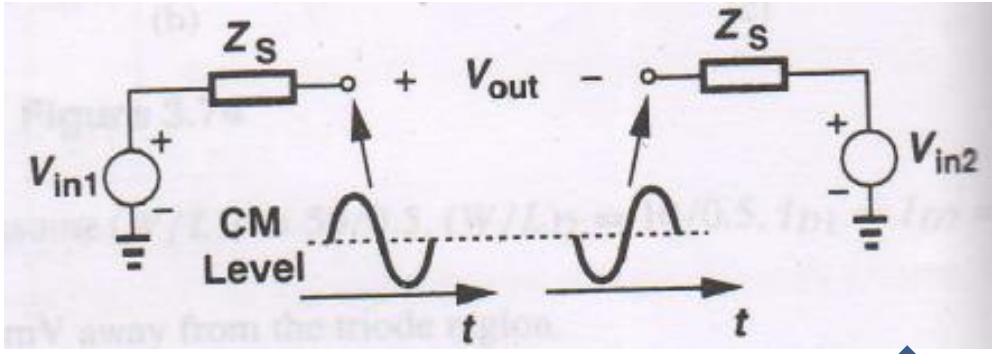
Differential amplifier deals with differential signals

Single-ended signals



Defined with respect to a fixed potential (usually ground)

Differential signals

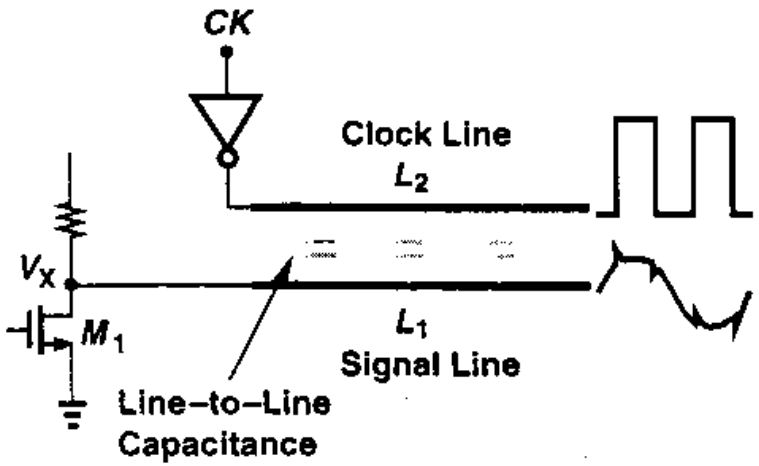


Defined between two nodes that have equal and opposite signal excursions around a fixed potential

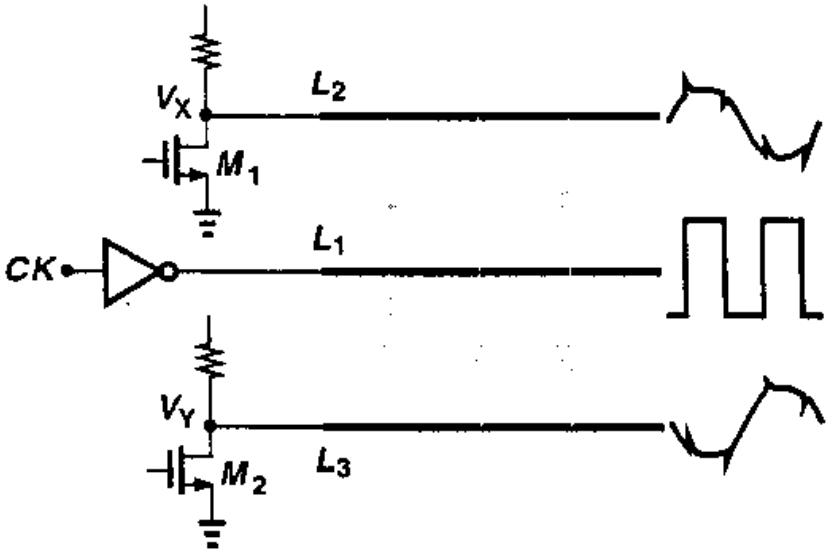
The fixed potential in differential signal is called "common-mode" CM level

Advantages of Differential Signaling

1. Immunity to Environmental Noise



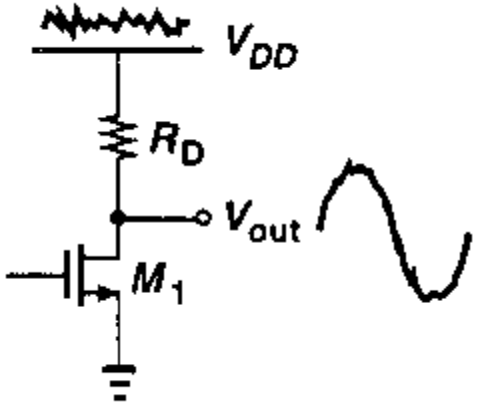
- Line L_1 carries a small and sensitive signal
- Line L_2 carries a large clock waveform
- Due to capacitive coupling between the lines, the transitions on line L_2 corrupt signal on line L_1

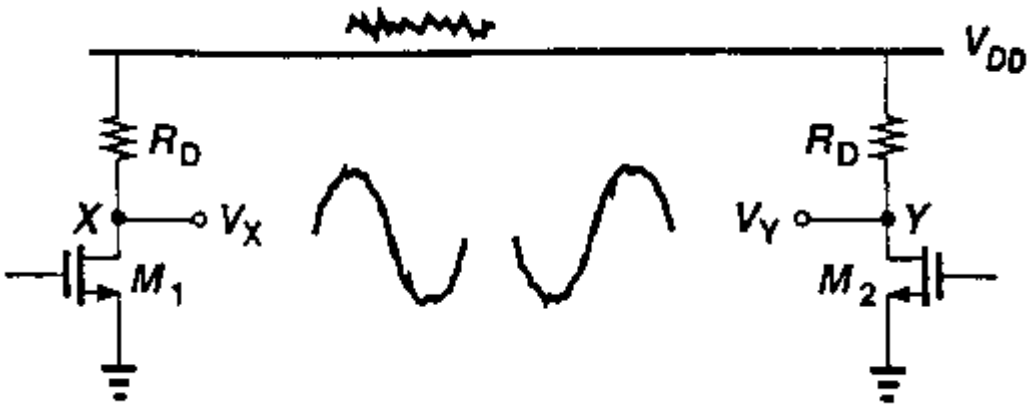


- The small and sensitive signal is distributed as two equal and opposite phases
- The clock signal is placed between the two
- The transition disturb the differential phases by equal amounts, leaving the difference intact

Advantages of Differential Signaling

2. Immunity to Supply Noise



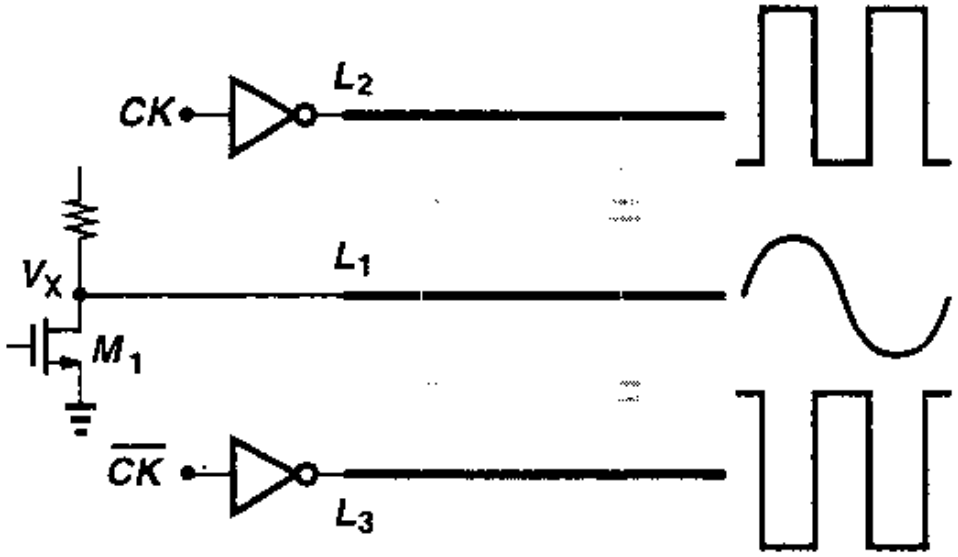


- If V_{DD} changes by ΔV, V_{out} changes by the same amount.
- Noise in V_{DD} affects V_X and V_Y, but not $V_X - V_Y$

Advantages of Differential Signaling

3. Reduction of Coupled Noise

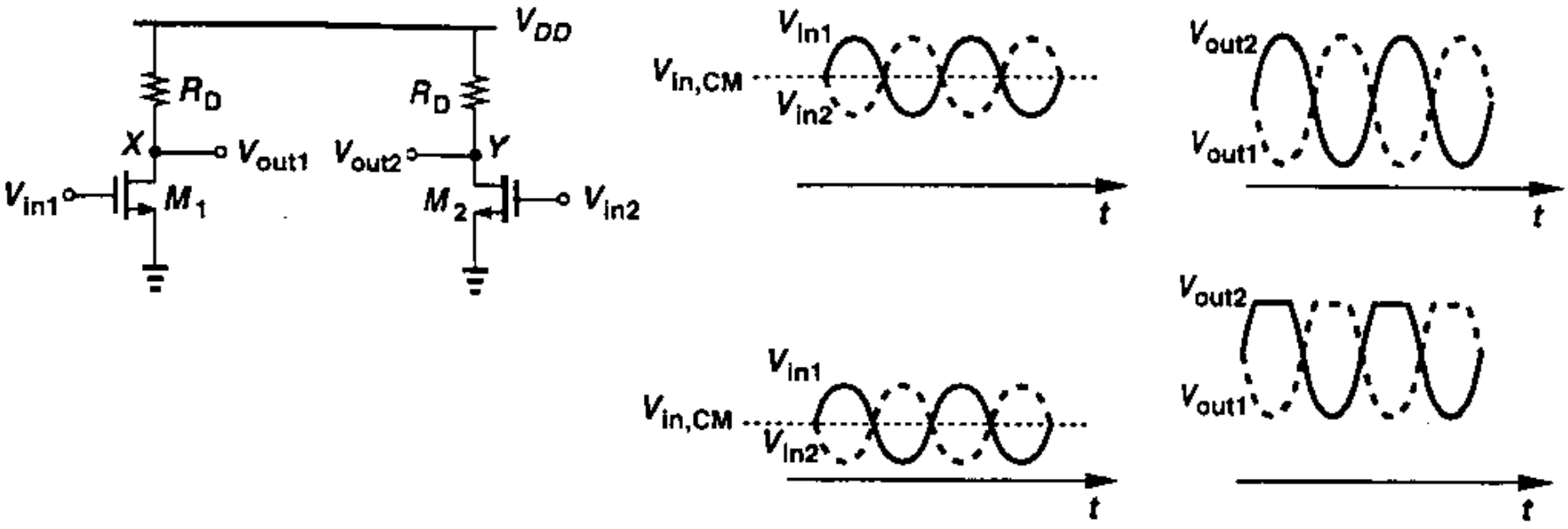
- Differential signaling can also be employed in noisy lines → for example, distributed clock can help in removing noise from signals



Noise coupled from L_3 to L_1 and L_2 to L_1 cancel each other.

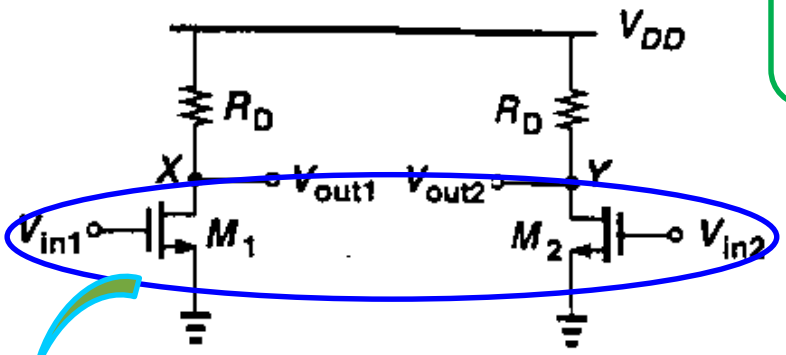
Issues with Differential Signaling

- Sensitivity to the Common Mode Level



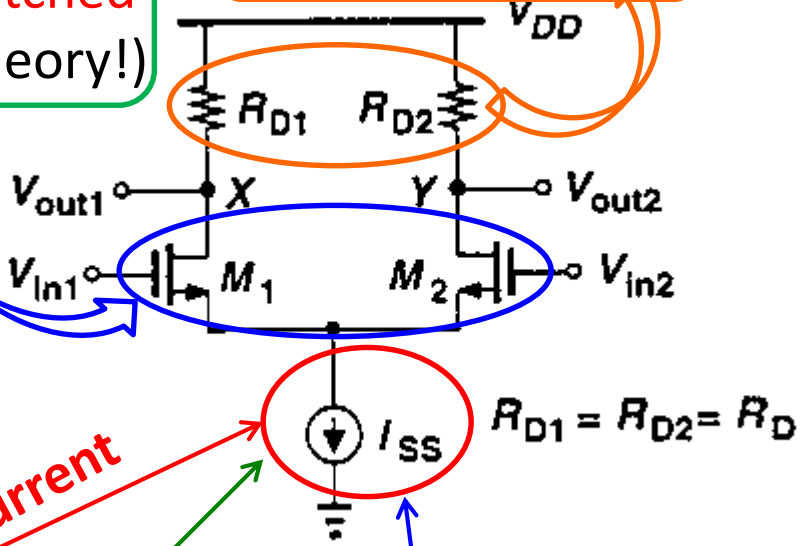
- Excessive low $V_{in,CM}$ turns off Devices → leads to clipping at the output
- Solution?

MOS Differential Pair



M_1 and M_2 are perfectly matched (at least in theory!)

ensures M_1 and M_2 in saturation



Variation of input CM level regulates the bias currents of M_1 and M_2 → Undesired!!!

Solution?? **Tail Current**

Need?

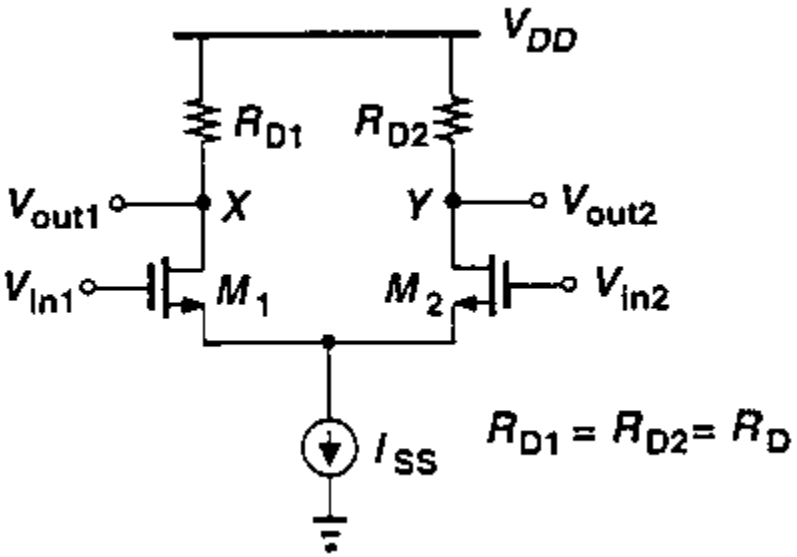
Current source is ideal: constant current, infinite output impedance

To overcome the issues emanating from non-ideal CM level

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from $-\infty$ to ∞

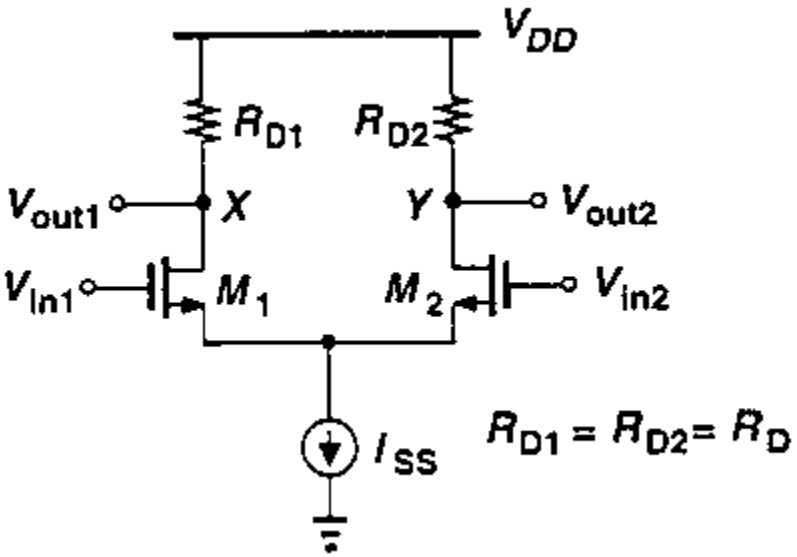


- V_{in1} is much more –ve than V_{in2} then:
  - M_1 if OFF and M_2 is ON
  - $I_{D2} = I_{SS}$
  - $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - I_{SS}R_D$
- V_{in1} is brought closer to V_{in2} then:
  - M_1 gradually turns ON and M_2 is ON
    - Draws a fraction of I_{SS} and lowers V_{out1}
  - I_{D2} decreases and V_{out2} rises
- $V_{in1} = V_{in2}$
  - $V_{out1} = V_{out2} = V_{DD} - I_{SS}R_D/2$

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from $-\infty$ to ∞

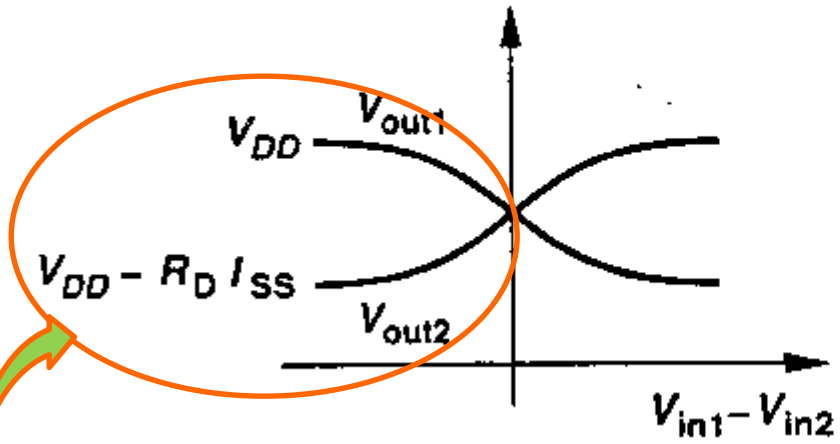


- V_{in1} becomes more +ve than V_{in2} then:
  - M_1 if ON and M_2 is ON
  - M_1 carries greater I_{SS} than M_2
- For sufficiently large $V_{in1} - V_{in2}$:
  - All of the I_{SS} goes through M_1 → M_2 is OFF
  - $V_{out1} = V_{DD} - I_{SS}R_D$ and $V_{out2} = V_{DD}$

MOS Differential Pair

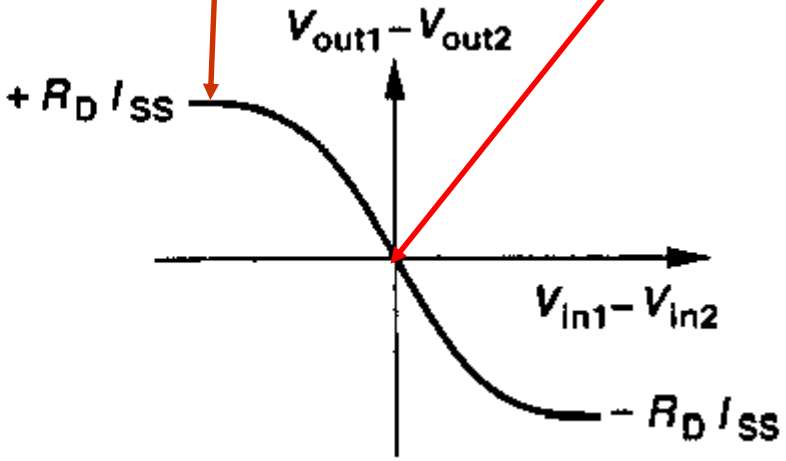
Qualitative Analysis – differential input

- Plotting $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$



Minimum Slope ↔ Minimum Gain

Maximum Slope ↔Maximum Gain



The maximum and minimum levels at the output are well defined and is independent of input CM level ($V_{in,cm}$)

The circuit becomes more nonlinear as the input voltage swing increases (i.e., $V_{in1} - V_{in2}$ increases) ↔ at $V_{in1} = V_{in2}$, the circuit is said to be in equilibrium

MOS Differential Pair

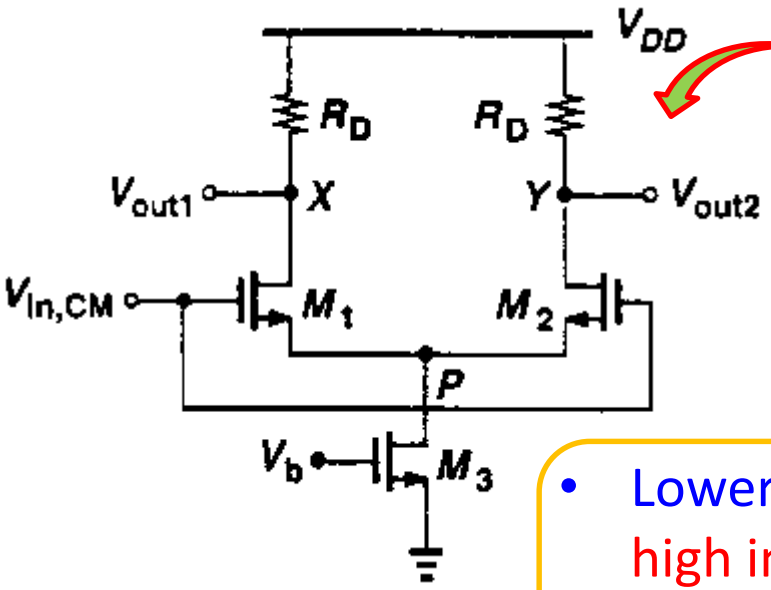
Qualitative Analysis – common mode input

- Now let us consider the common mode behavior of the circuit

As mentioned, the tail current source is used to suppress the effect of input CM level variation ($V_{in,cm}$)

⇔

Does this enable us to set any arbitrary level of input CM ($V_{in,cm}$)



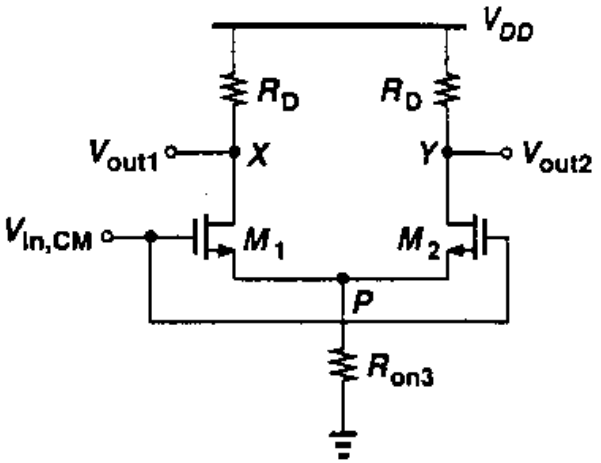
To understand this:

- Set $V_{in1} = V_{in2} = V_{in,CM}$
- Then vary $V_{in,CM}$ from 0 to V_{DD}
- Also implement I_{SS} with an NFET

- Lower bound of $V_{in,cm}$: V_P should be sufficiently high in order for M_3 to act as a current source.
- Upper bound of $V_{in,\ cm}$: M_1 and M_2 need to remain in saturation.

MOS Differential Pair

Qualitative Analysis – common mode input



- What happens when $V_{in,CM} = 0$?
  - M_1 and M_2 will be OFF and M_3 can be in triode for high enough V_b
  - $I_{D1} = I_{D2} = 0$ ← circuit is incapable of amplification

- Now suppose $V_{in,CM}$ becomes more +ve
  - M_1 and M_2 will turn ON if $V_{in,CM}$ exceeds V_T
  - I_{D1} and I_{D2} will continue to rise with the increase in $V_{in,CM}$
  - V_P will track $V_{in,CM}$ as M_1 and M_2 work like a source follower
  - For high enough $V_{in,CM}$, M_3 will be in saturation as well

- If $V_{in,CM}$ rises further
  - M_1 and M_2 will remain in saturation if:

$$V_{in,CM} - V_T \le V_{out1} \quad \Rightarrow \quad V_{in,CM} \le V_{DD} - \frac{I_{SS}}{2} R_D + V_T$$

MOS Differential Pair

Qualitative Analysis – common mode input

- For M_1 and M_2 to remain in saturation:

$$V_{GS1,2} - V_T \le V_{DS1,2} \quad \Rightarrow V_{in,CM} - V_T \le V_{DD} - \frac{I_{SS}}{2} R_D \quad \Rightarrow V_{in,CM} \le V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

$$\therefore (V_{in,CM})_{\max} = V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

- The lowest value of $V_{in,CM}$ is determined by the need to keep the constant current source operational:

$$V_{in,CM} - V_{GS1,2} \ge V_{GS3} - V_T$$

$$\Rightarrow V_{in,CM} \ge V_{GS1,2} + (V_{GS3} - V_{T3})$$

$$V_{GS1,2} + (V_{GS3} - V_T) \le V_{in,CM} \le \min\left[V_{DD} - \frac{I_{SS}}{2} R_D + V_T, V_{DD} \right]$$

MOS Differential Pair

Qualitative Analysis – common mode input

- Thus, $V_{in,CM}$ is bounded as:

$$V_{GS1,2} + (V_{GS3} - V_T) \le V_{in,CM} \le \min\left[V_{DD} - \frac{I_{SS}}{2} R_D + V_T, V_{DD}\right]$$

- Summary: