Start with
Synopsys DesignCompiler

Design File

Create a hdl file for the desired design. For example *up_down_counter.v*

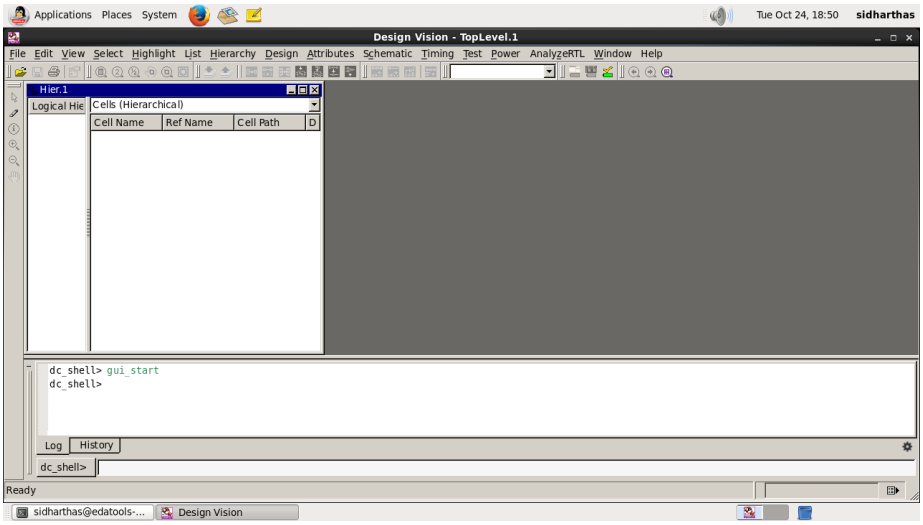
Steps to Access Synopsys Design Compiler

(i) Log in to your account on EDA Server

(ii) Open a new terminal

(iii) Run the command *dc_shell -gui*

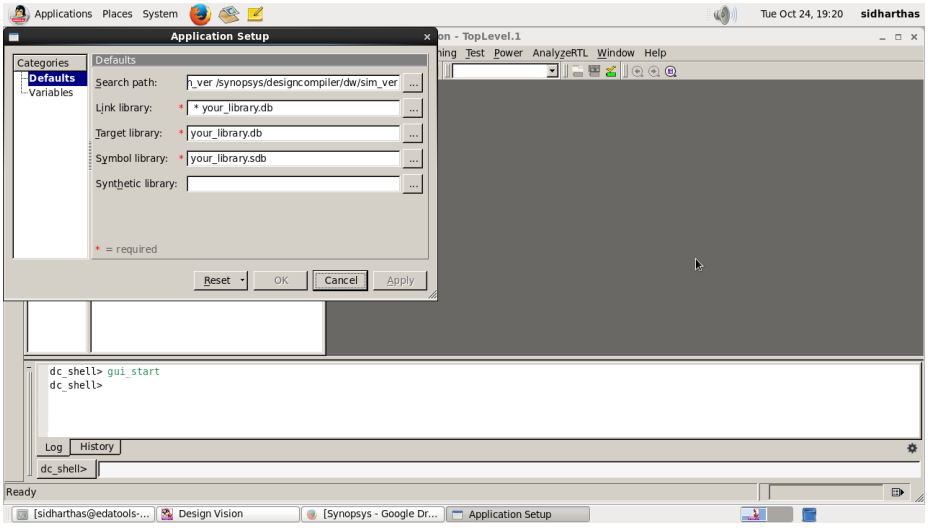
Following window will open



Set the Technology Library Path

(i) Go to File -> Setup

You will find the following window



(ii) Now you have to give the path of the technology library file as follows:

Search path: /synopsys/designcompiler/dvd_la_library

Note – delete all the pre-existing paths and give the new path as above

Link library: saed90nm_typ.db (90nm)

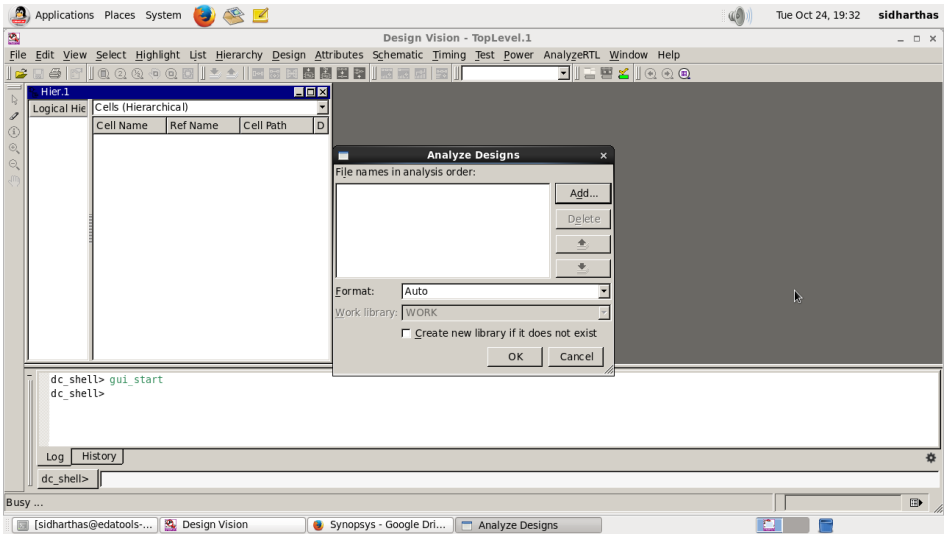
Target library: saed90nm_typ.db

Leave the *Symbol library* and the *Synthetic library* as it is.

(iii) Click ok

Analyse the Design

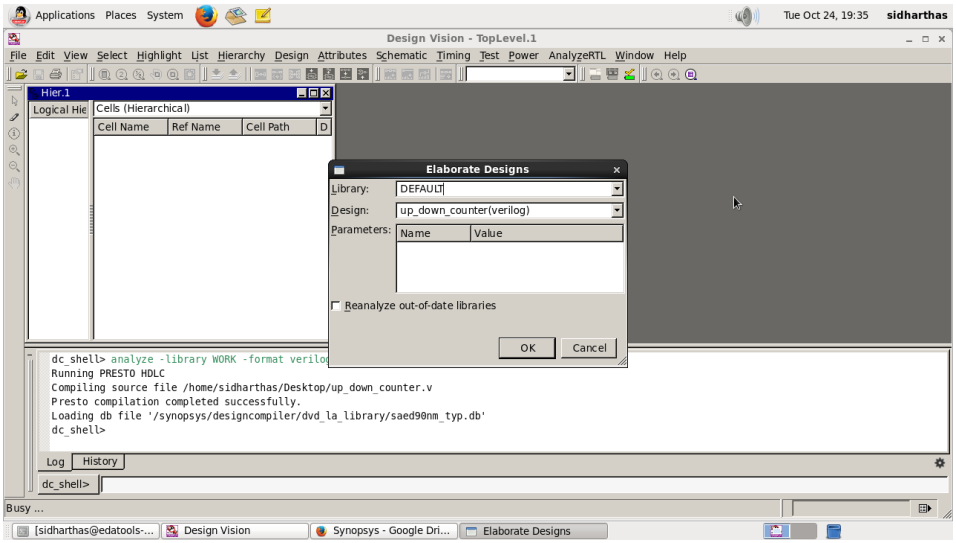
(i) Go to File -> Analyse
You will find the following window



(ii) Add the pre-designed HDL file
(iii) Keep the *work library* as WORK

Elaborate the Design

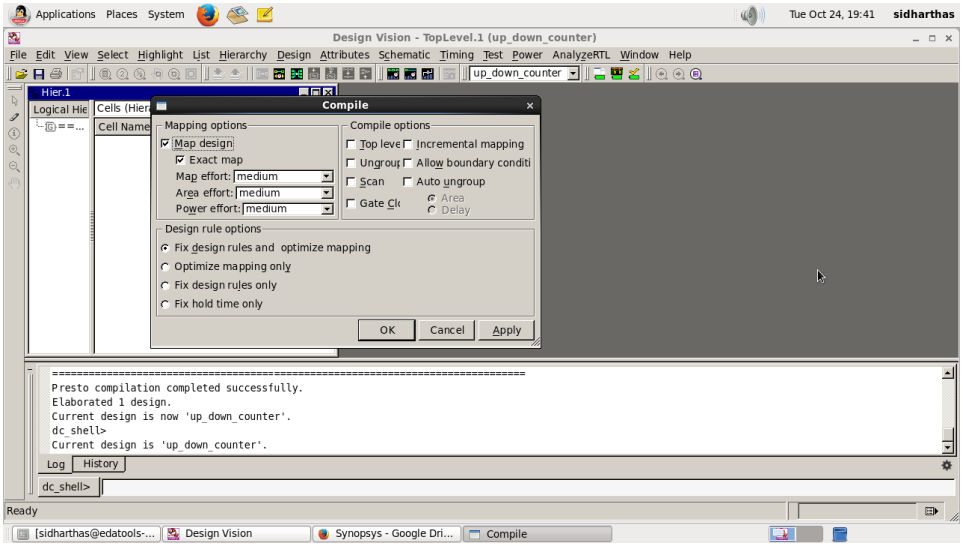
(i) Go to File -> Analyse
You will find the following window



(ii) Change the *Library* to WORK
(iii) Click ok
(iv) Check the log, whether any error or warning is coming! If everything fine, then proceed to the next step

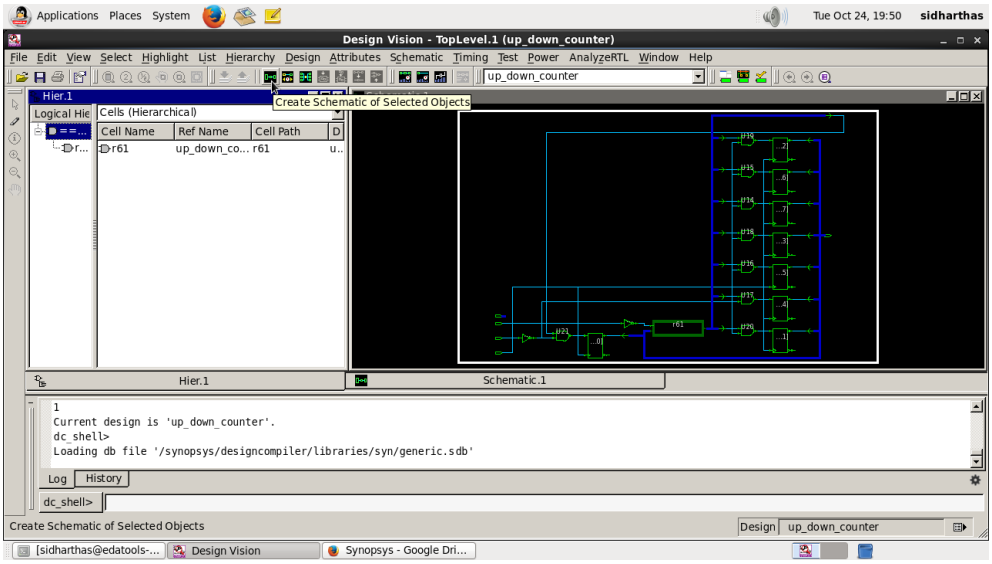
Compile Design

(i) Go to Design -> Compile Design
You will find the following window



(ii) Click ok

Now the design is compiled (synthesized). The gate level schematic can be seen as below (in 90nm Technology)



Report Generation

Now you can generate different synthesis reports for area, power etc.

For generating report you have to go to Design -> Report Area; Design -> Report Power etc.

Note: If you find any discripancy in this manual or you want to add any valuable information to this manual, please drop a mail to sidharthas@iiitd.ac.in