One Day Workshop on Network-on-Chip
March 29, 2015 (Sunday)
Organized By IIIT Delhi
In Collaboration with MNIT Jaipur and IEEE Student Branch, IIITD

About the Workshop
Current commercial System-on-Chip (SoC) designs integrate an increasingly large number of predesigned cores and their number is predicted to increase significantly in the near future. These state-of-the-art commercial SoC designs with a large number of intellectual property (IP) blocks, commonly known as cores, on a single die are made feasible by the continuing progress and integration levels in silicon technologies. This massive level of integration makes modern multi-core chips all pervasive in domains ranging from weather forecasting, astronomical data analysis and biological applications, to consumer electronics and smartphones. The growing complexity of integration as well as aggressive technology scaling introduces multiple challenges for the design of such big multi-core SoCs. An important feature of such Multi-Processor SoCs (MP-SoC) is the interconnection fabric, which must allow seamless integration of numerous cores performing various functionalities. The Network-on-Chip (NoC) design paradigm, based on a modular packet-switched mechanism, can address many of the on-chip communication issues such as performance limitations of long interconnects, and integration of large number of cores on a chip.

Key Goals
- Participants will learn about important concepts related to design, testing and analysis of on-chip communication infrastructures
- To discuss the challenges faced in developing low power designs and efficient communication architectures for many core systems
- To provide a forum for researchers to present and discuss innovative ideas and solutions pertaining to the design of many core SoCs and NoCs

Workshop Organization
The workshop will have lectures on topics related to emerging on-chip communication infrastructures, low-cost NoC routers, NoC design & testing, NoC for high performance computing, etc. by invited speakers followed by interactive sessions

Target Audience
- B.Tech students doing research/projects in this field
- M.Tech, Ph.D & Research scholars
- Faculty members
- Professionals from Industry

Invited Speakers
- Dr. Madhu Mutyam, Associate Professor, IIT Madras
- Dr. Virendra Singh, Associate Professor, IIT Bombay
- Dr. Turbo Majumdar, Assistant Professor, IIT Delhi
- Dr. Manoj Singh Gaur, Professor, MNIT Jaipur
- Dr. Sujay Deb, Assistant Professor, IIIT Delhi

Organizing Committee
- Dr. Sujay Deb, IIIT Delhi
- Dr. Manoj Singh Gaur, MNIT Jaipur

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Registration Details:
Registration Fees:
Students (including Ph.D & research scholars) - INR 500
Professionals - INR 1000

Registration Deadline: March 20, 2015
Registration Link: http://www.iiitd.edu.in/noc/