RF Energy Harvesting

Student Name: Ankush Jolly
Roll Number: 2012128

Student Name: Siddhant Verma
Roll Number: 2012165

BTP report submitted in partial fulfillment of the requirements
for the Degree of B.Tech. in Electronics & Communication Engineering
on April 19, 2016

BTP Track: Engineering

BTP Advisor
Dr. Vivek Bohara

Indraprastha Institute of Information Technology
New Delhi

Student's Declaration

I hereby declare that the work presented in the report entitled **"RF Energy Harvesting"** submitted by us for the partial fulfillment of the requirements for the degree of *Bachelor of Technology* in *Electronics & Communication Engineering* at Indraprastha Institute of Information Technology, Delhi, is an authentic record of my work carried out under guidance of **Dr. Vivek Bohara**. Due acknowledgements have been given in the report to all material used. This work has not been submitted anywhere else for the reward of any other degree.

Ankush Jolly
Siddhant Verma

Place & Date: IIIT-Delhi, April 19, 2016

Certificate

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Dr. Vivek Bohara
Assistant Professor

Place & Date: IIIT-Delhi, April 19, 2016

Abstract

Wireless Sensor network(WSN) is the important component in implementing Internet of Things(IOT) on a large scale. This vast network of sensors requires regular energy and replacing batteries of this wide array of sensors is a tedious task. So in order to have an efficient use of these sensors, harvesting energy from ambient Radio Frequency(RF) sources is an attractive approach towards the power constraint problem. We have tried to approach this problem by making a dual-band multi-stage rectifier at 915 MHz and 2.42 GHz respectively so that harvested power is more than that of harvested at one frequency. We have also made a conventional quadrupler circuit at 915 MHz with an inductor to enhance the efficiency and output voltage. The peak efficiency for dual-band circuit is 67% percent at 915 MHz and 66% at 2.4 GHz respectively at 10 dBm input power. For the quadrupler circuit, peak efficiency is 71% at 10 dBm input power.

Keywords: Efficiency, inductor, output voltage, quadrupler, rectifier

Acknowledgments

We would like to thank Dr. Vivek Bohara for giving us the opportunity to do the project titled RF Energy Harvesting and providing us with all the support and guidance. It was his guidance and morale support that helped us in the process of learning and completing the last phase of this project. We would like to express our sincere gratitude to our parents, colleagues and TAs who have been a constant support of inspiration throughout the course of this project.

Work Distribution

Almost everything was done in collaboration especially experimental part. As far as simulation is concerned, Ankush Jolly simulated dual band and doubler circuit while Siddhant Verma simulated triper and quadrupler circuit.

Contents

1 Introduction **1**

2 System Overview **2**

2.1 Voltage Doubler 2

2.2 DC Voltage Tripler Circuit 3

2.3 DC Voltage Quadrupler Circuit 4

2.4 Dual-band Matching 5

3 Simulation/Experimental Results **7**

3.1 Prototype 7

3.2 Experimental Results (LED glow experiment) 9

3.3 Voltage Doubler Results 12

3.4 Voltage Tripler Results 14

3.5 Voltage Quadrupler with inductor results 16

3.6 Multi-Stage Dual-band Rectifier 19

4 Conclusion and work left **22**

Chapter 1

Introduction

In our previous semester, we succeeded in building up a prototype of our RF energy circuit which we thought could give us promising results. The prototype was fabricated on FR4 substrate and could only give us results for output voltage. Measuring current was a hassle with our design as we didnt leave any gap in our circuit according to the ammeter configuration. So, without the value of current obtained, we couldnt tell about the power conversion efficiency of our circuit. Moreover, high tangent loss of FR4 resulted in less efficiency and thats why we decided to use Rogers Substrate for better results.

This semester, we tweaked our circuit by leaving a gap in our design from where we could attach a wire, connect to a multimeter and measure current to calculate the power conversion efficiency.

We also designed two new circuits: A dual-band RF energy harvesting circuit (915 MHz and 2.42 GHz) and a Quadrupler circuit (0.915 GHz) which gave us pretty good results in simulations compared to our previous designs and perfect DC voltage which we werent able to get earlier. Our end goal is to fabricate these designs and take measurement results in the coming week itself. We also tried to glow an LED but due to the received power constraint from the cellular towers, we did the experiment in RF lab itself and used signal generator for the same.

Chapter 2

System Overview

Firstly, we rebuilt the circuit that we had made last semester but this time we left a gap in our circuit to measure current and changed the substrate from FR4 to Rogers. We designed its layout, made changes in the EM model accordingly and got two models of the same circuit fabricated.
We couldnt measure the output current despite leaving a gap this time and there could be multiple reasons behind this. We tried to analyze the circuit using Vector Network Analyzer(VNA) but it didnt show any dip at our design frequency of 2.1 GHz. A possible reason could be that of poor soldering.
As for the second prototype, even that didnt show any reading when we tried measuring current or any dip at our design frequency. Even though the components were very well soldered compared to the first prototype, we got negligible voltage drop across our load but it showed a good DC voltage across the diode. **The very minute size of capacitor which is difficult to see even with a naked eye created a short in the circuit connecting our load to the ground**. The gap in the circuit might also be a reason for that.

2.1 Voltage Doubler

A voltage doubler is an electronic circuit which charges capacitors from the input voltage and switches these charges in such a way that, in the ideal case, exactly twice the voltage is produced at the output as that of its input.
A simple form of a rectifier takes an AC voltage as input and outputs a doubled DC voltage. The switching elements are simple diodes and they are driven to switch state merely by the alternating voltage of the input. DC-to-DC voltage doublers cannot switch in this way and require a driving circuit to control the switching. They frequently also require a switching element that can be controlled directly, such as a transistor, rather than relying on the voltage across the switch as in the simple AC-to-DC case.
Voltage doublers are a variety of voltage multiplier circuit. Many, but not all, voltage doubler

circuits can be viewed as a single stage of a higher order multiplier: cascading identical stages together achieves a greater voltage multiplication.

Working:

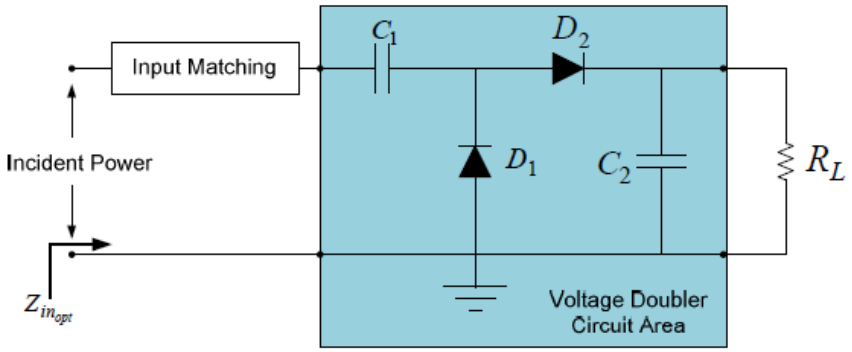

Figure 2.1: DC Voltage Doubler circuit[1]

The voltage clamp (D1 and C1) and a peak rectifier (D2 and C2) are the main components that rectify the full-wave peak-to-peak voltage of the incident RF signal(V_{in}). The current flow through D1 and is stored by C1 while D2 is cut-off on the negative half-cycle of the incident signal (V_{in}-). The voltage across D1 is close to its threshold voltage (V_{th1}) and the stored voltage of C1 (V_{C1}) can be determined by equation 2.1.

$$V_{C1} = V_{in-} - V_{th1} \tag{2.1}$$

During the positive half-cycle of the incident signal (V_{in+}), the current flows through D2 while D1 is cutoff. The stored voltage of C1 combined with the positive half cycle gives twice the incident signal(V_{in+}). Therefore, the output voltage (V_{out}) of the circuit can be calculated by equation 2.2.

$$V_{Out} = 2V_{in} - V_{th1} - V_{th2} \tag{2.2}$$

The advantage of Voltage Multiplier Circuits is that it allows higher voltages to be created from a low voltage power source without a need for an expensive high voltage transformer.

2.2 DC Voltage Tripler Circuit

This is just another voltage multiplier circuit that is made by adding an additional single diode-capacitor stage to the half-wave voltage doubler circuit and it increases its input voltage by a factor of three and producing what is called a Voltage Tripler Circuit.

A voltage tripler circuit consists of one and a half voltage doubler stages. This voltage mul-

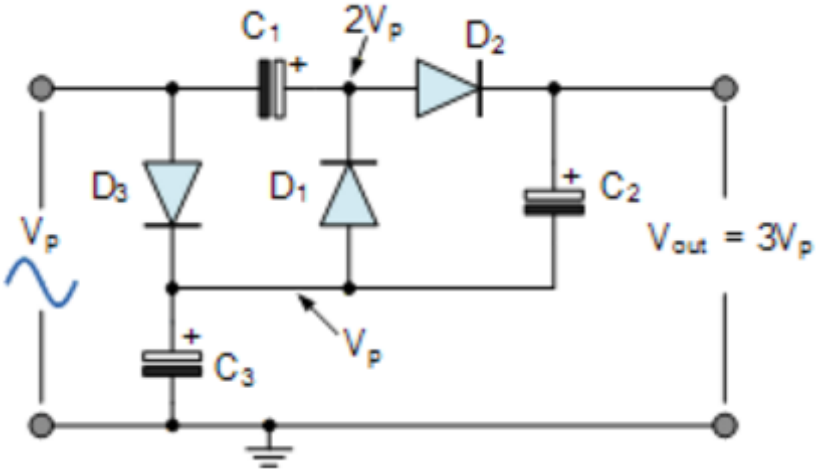

Figure 2.2: DC Voltage tripler circuit[1]

tiplier circuit gives a DC output equal to three times the peak voltage value ($3V_p$) of the sinusoidal input signal (V_p). Just like the voltage doubler, the diodes within the voltage tripler circuit charge and block the discharge of the capacitors depending upon the direction of the input half-cycle. Then $1V_p$ is dropped across C3 and $2V_p$ across C2 and as the two capacitors are in series, this results in the load seeing a voltage equivalent to ($3V_p$).
But there is some discharge of voltage because of turn on voltage of diodes and effectively the real output voltage will be three times the peak input voltage minus the voltage drops across the diodes used, $3V_p$ - V(diode).

2.3 DC Voltage Quadrupler Circuit

The first voltage multiplier stage doubles the peak input voltage and the second stage doubles it again, giving a DC output equal to four times the peak voltage value ($4V_p$) of the sinusoidal input signal and hence the name Quadrupler circuit.

We conclude that Voltage Multipliers are simple circuits made from diodes and capacitors that can increase the input voltage by two, three, or four times and by cascading together individual half or full stage multipliers in series to apply the desired DC voltage to a given load without the need for a step-up transformer.
Depending upon the ratio of the output voltage to the input voltage, Voltage multiplier circuits are classified as voltage doublers, triplers or quadruplers etc. In theory any desired amount of voltage multiplication can be obtained and a cascade of N doublers, would produce an output voltage of 2N x V_p volts.
Also, a very important point to be kept in mind while increasing the number of Voltage multiplier stages is that increasing the number of stages gives a higher voltage at the load, and yet

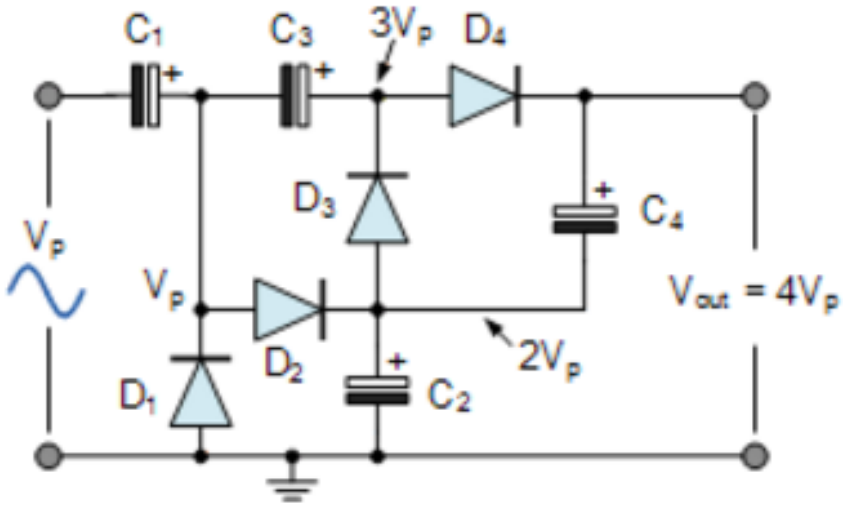

Figure 2.3: DC Voltage Quadrupler Circuit[1]

reduces the current through the final load branch. This may result in unacceptable charging delays for the energy storage capacitor. Conversely, fewer stages of the multiplier will ensure quick charging of the capacitor, but the voltage generated across it may be insufficient.

2.4 Dual-band Matching

We have designed a dual-band RF energy harvesting circuit that works for 2 different frequencies(915 MHz and 2.42 GHz) using dual-band matching network technique that uses dual-band quarter wavelines. This technique helps in simultaneous matching of two Frequency dependent complex loads(FDCL) having different values at two arbitrary frequencies to a real source impedance Z_o.

The basic structure of the transformer is shown in Figure 1. The FDCL is assumed to have values as $Z_L = R_1 + jX_1$ @ f1 and $Z_L = R_2 + jX_2$ @f2. Yin1 is the admittance looking into Section A, Y_{in2} is the admittance looking into Section B whereas Z_{in3} is the impedance looking into the combination of Section A and Section B.

It is apparent from Figure 1 that transformer A converts the FDCL to produce Y_{in1} such that Y_{in1} | f1 = Y^*_{in1} | f2, that is, if Y_{in1}| f1 = G - jB then Y_{in1}| f2 = G + jB. Section B, which is primarily a dual-band susceptance, cancels out the imaginary parts of Yin1 at the two specified frequencies. Thus, as a last step there is a need to match $Z_{in3} = 1/G$ to Z_o at the two frequencies. It is well known that a real impedance (such as Z_{in3}) can be matched to another real impedance (such as Z_o) using a $\lambda/4$ line; the only additional requirement in the present case is to have a dual-band $\lambda/4$ line which is what Section C essentially is.

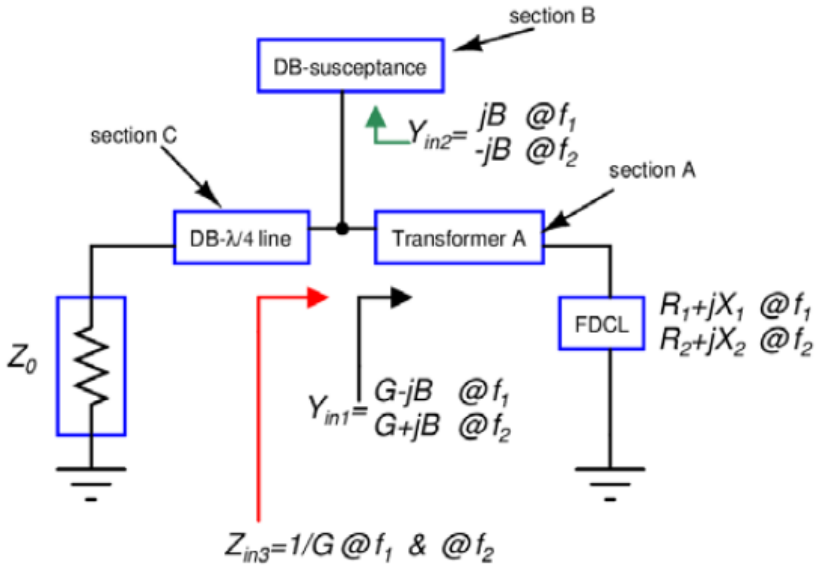

Figure 2.4: Pictorial illustration of the matching scheme (DB: dual-band)[2]

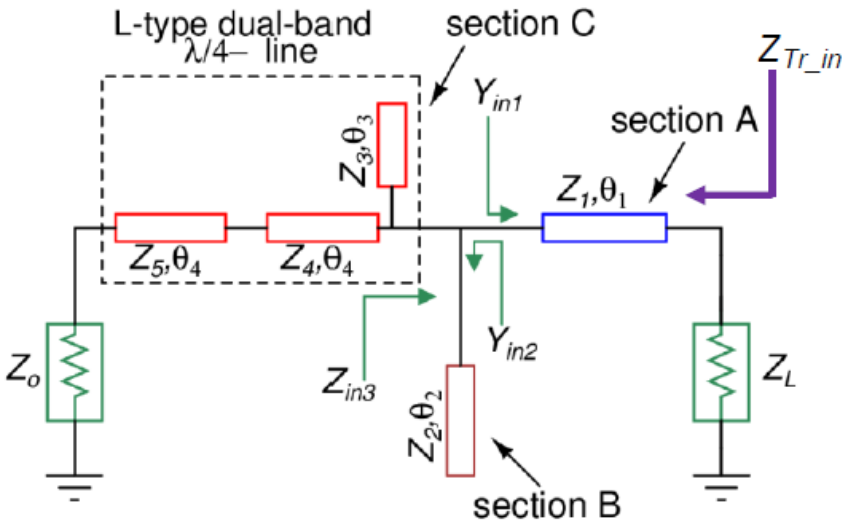

Figure 2.5: Implementation of Dual Band Matching [2]

Chapter 3

Simulation/Experimental Results

3.1 Prototype

This chapter presents the experimental results of the prototype that was fabricated using Rogers Substrate. Moving on, we have also included the simulation results of the conventional doubler, tripler and quadrupler rectifier along with the dual-band multi-stage rectifier. The simulation results include plots of efficiency vs input power, output dc voltage vs input power, circuit schematic and S11 plot.

We will start with simulation results of the initial 2.1 GHz centred circuit that was our prime focus last semester. As expected, Rogers substrate gave better simulation results than FR4 substrate due to lower value loss tangent. Figure 3.1 shows the schematic of the circuit. The frequency of operation is 2.1 GHz.

Figure 3.2 shows the comparison between the efficiencies obtained from circuit with Rogers

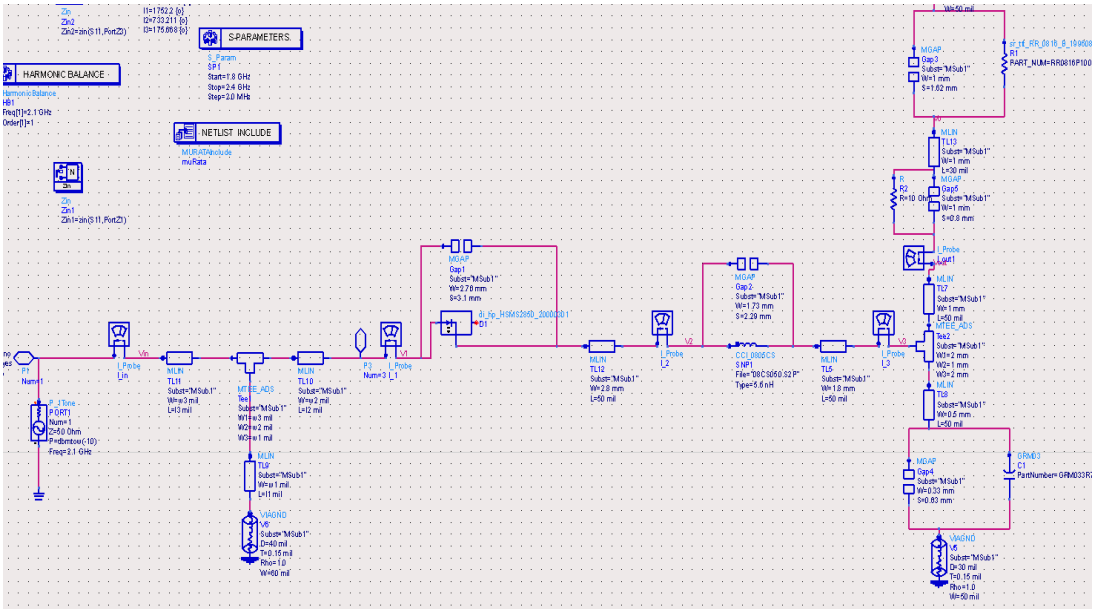

Figure 3.1: Energy Harvester @2.1 GHz

substrate and FR4 substrate. Figure 3.3 shows the S11 plot while Figure 3.4 shows the plot of Output DC voltage vs Input Power. Since, the efficiency obtained with Rogers was better than FR4, we decided to go with fabrication and soldering process.

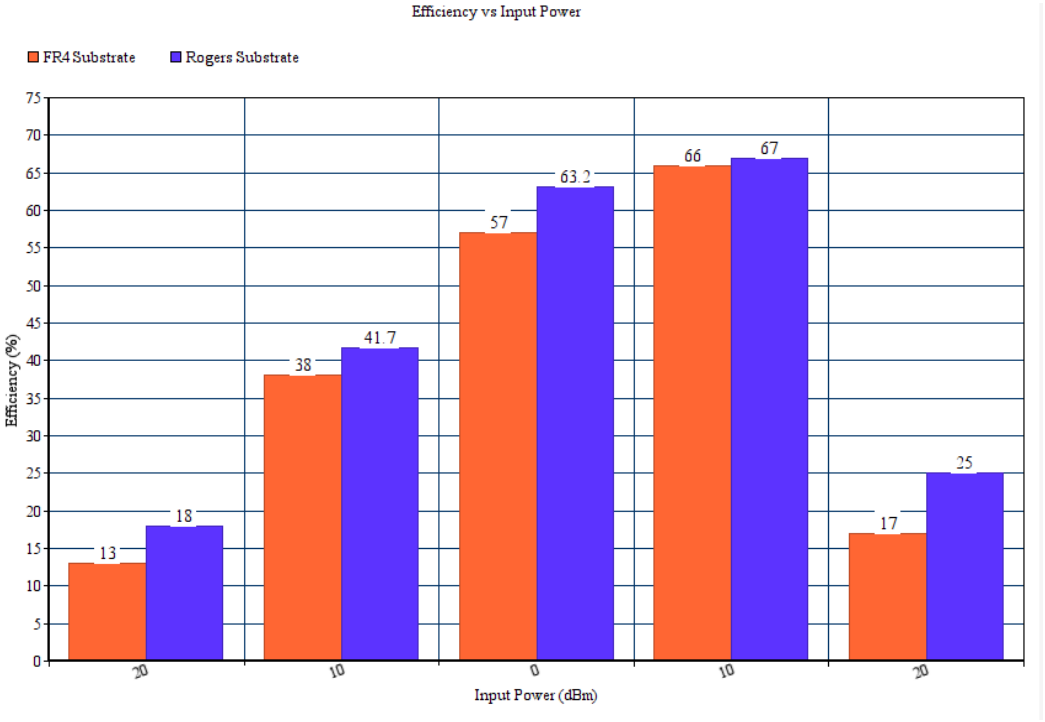

Figure 3.2: Efficiency comparison between 2 materials

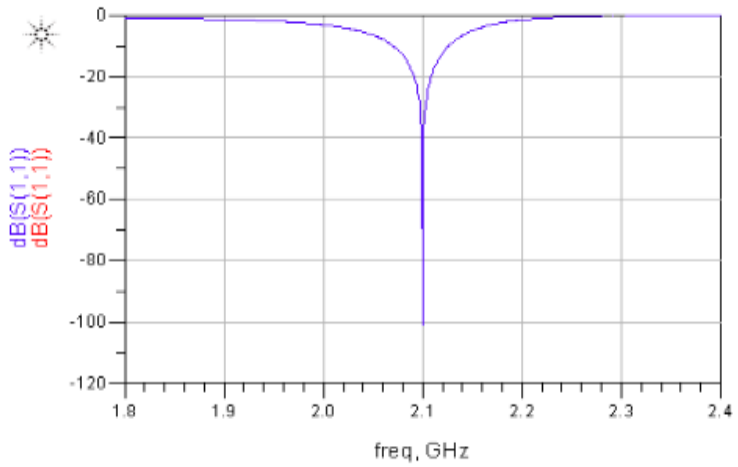

Figure 3.3: S11 plot

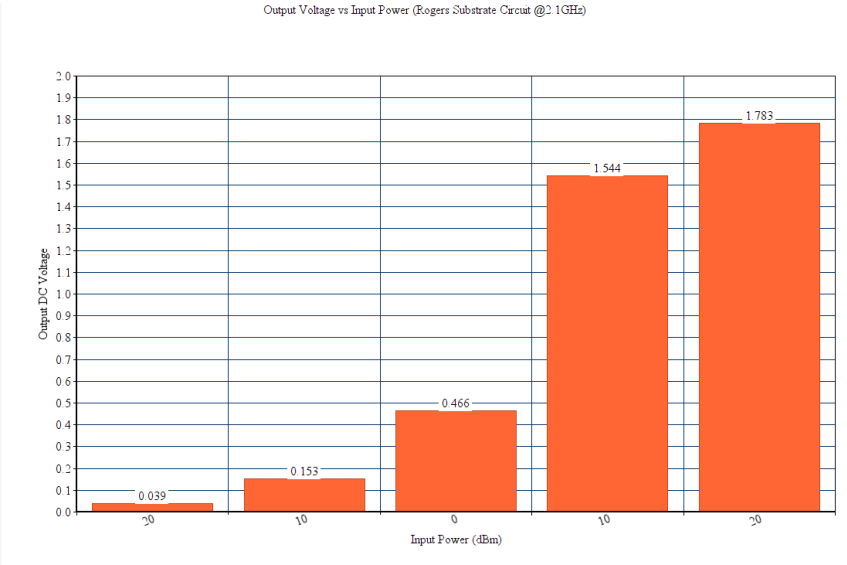

Figure 3.4: Output DC voltage vs Input Power

3.2 Experimental Results (LED glow experiment)

Figure 3.5 shows the soldered fabricated prototype. We faced a major soldering problem in the circuit as the capacitor size is too small to be soldered by an unprofessional person and also the gap that we had left for measuring current might also be the reason for shorting of the circuit near the load. So, we measured values of the DC voltage across the inductor and the ground. Since our major interest is to try to generate the desired voltage that can glow an LED using as minimum power as required, we connected our prototype with the Signal generator as shown in Figure 3.6. Table 3.1 shows the output voltage generated at three different input power levels. We analysed that 2.6V is the minimum voltage required for the white LED to glow and also a white LED causes a 0.3 V drop across it, so 2.9V has to be generated across the load resistor for the same. Figure 3.7 shows the setup and it was measured that a minimum of 15 dBm power was given at signal generator for the LED to glow.

Figure 3.5: Fabricated Prototype

Figure 3.6: Prototype connected to Signal Generator

Table 3.1: DC voltage values generated during setup shown in Figure 3.6

Input Power(dBm)	Output DC voltage(V)
0	0.7
10	2.1
20	4.2

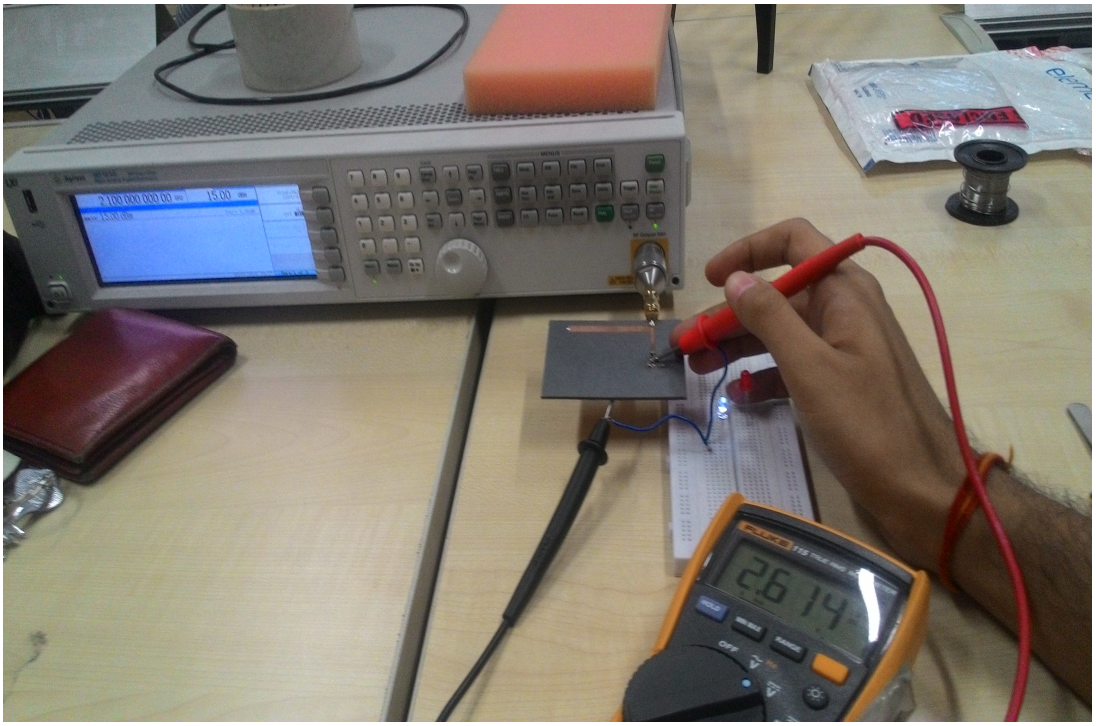

Figure 3.7: LED glow setup

Since, LED glowed when prototype was connected to the signal generator but a main accomplishment would be to repeat the same experiment wirelessly. So, for that we did an experiment using Yagi Antennas with the help of a power amplifier. The maximum input power from signal generator was 15 dBm as after this amount of power, power supply of Power Amplifier starts fluctuating which results in disturbance in the setup.

We found out that wireless results were very poor and the maximum voltage at output was 0.28V when both of the antennas were almost near to each other as shown in Figure 3.8. **We did the same experiment using older prototype that was fabricated last semester and the maximum output voltage was 0.12V which did give us a proof that newer prototype is still better than previous one.**

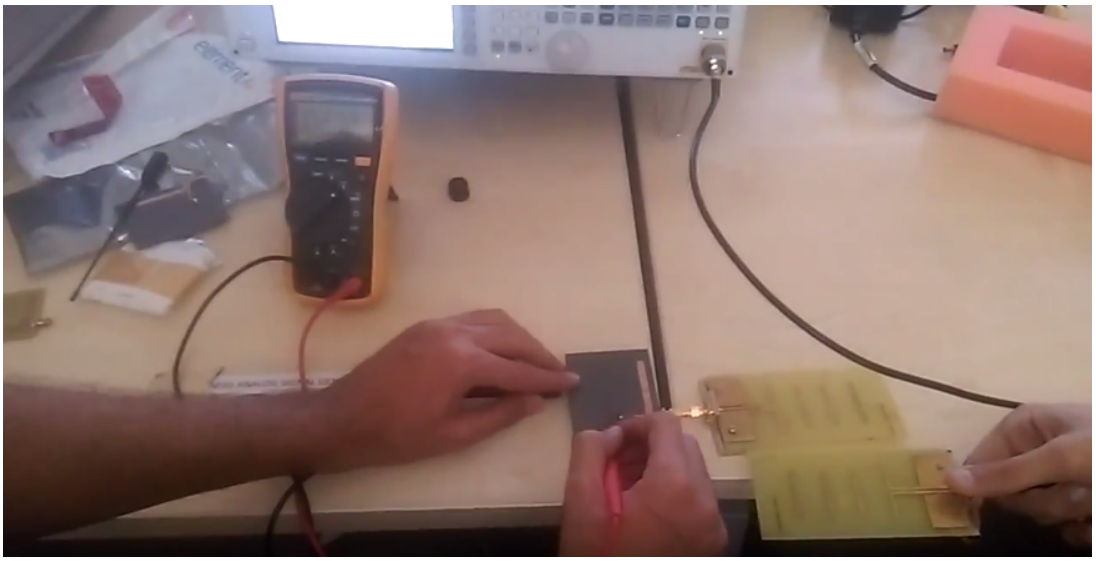

Figure 3.8: Power Amplifier setup as discussed above

After these experiments, we decided to take a look at the conventional voltage doubler, tripler and quadrupler configurations as they give much higher output voltage which is desired to complete LED glow experiment. The frequency of interest in all the three configurations was 915 MHz. Moreover, we get a complete DC voltage during simulation unlike our previous rectifier circuit in which the output was not pure DC. We also came up with a conventional multi-stage rectifier and converted it to a dual-stage rectifier. We will discuss the problems faced during converting a circuit to a dual stage design.

3.3 Voltage Doubler Results

Figure 3.9 shows the schematic of a voltage doubler circuit while figure 3.10 shows the efficiency plot and figure 3.11 shows the output voltage plot.

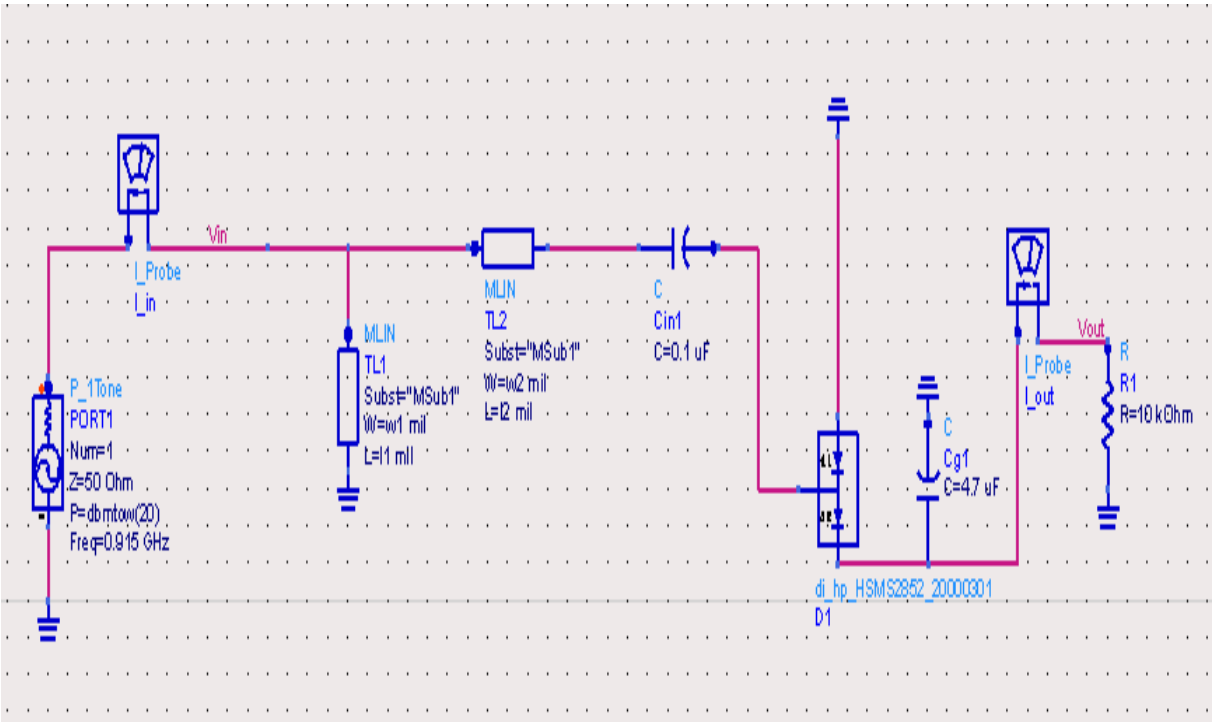

Figure 3.9: Voltage Doubler Schematic

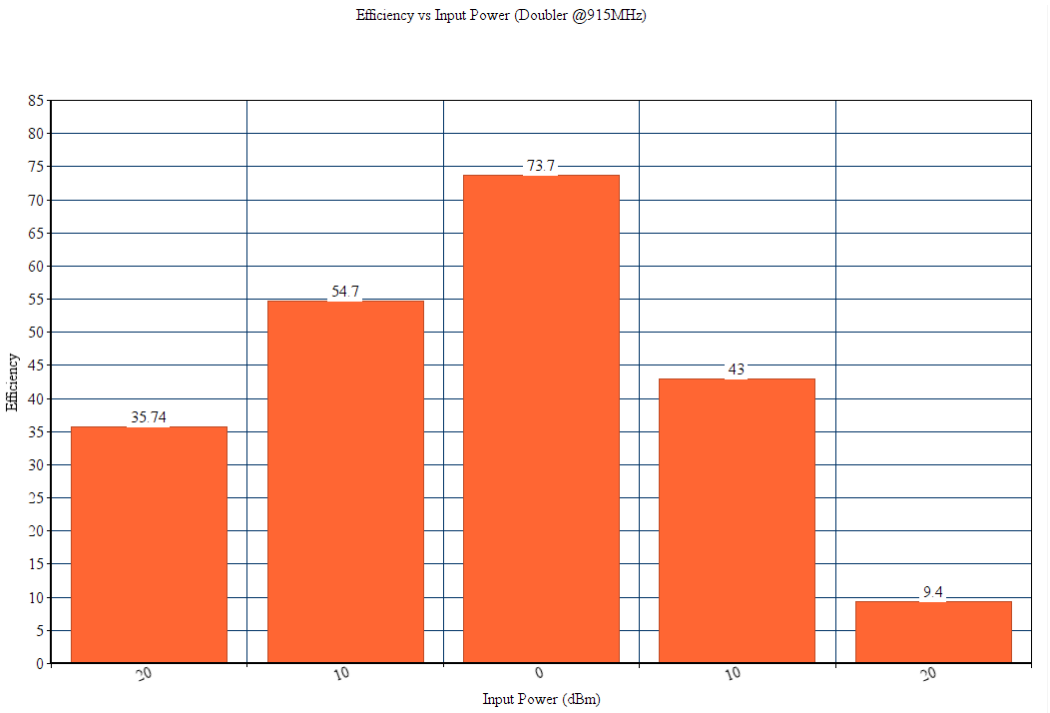

Figure 3.10: Efficiency Vs Input Power

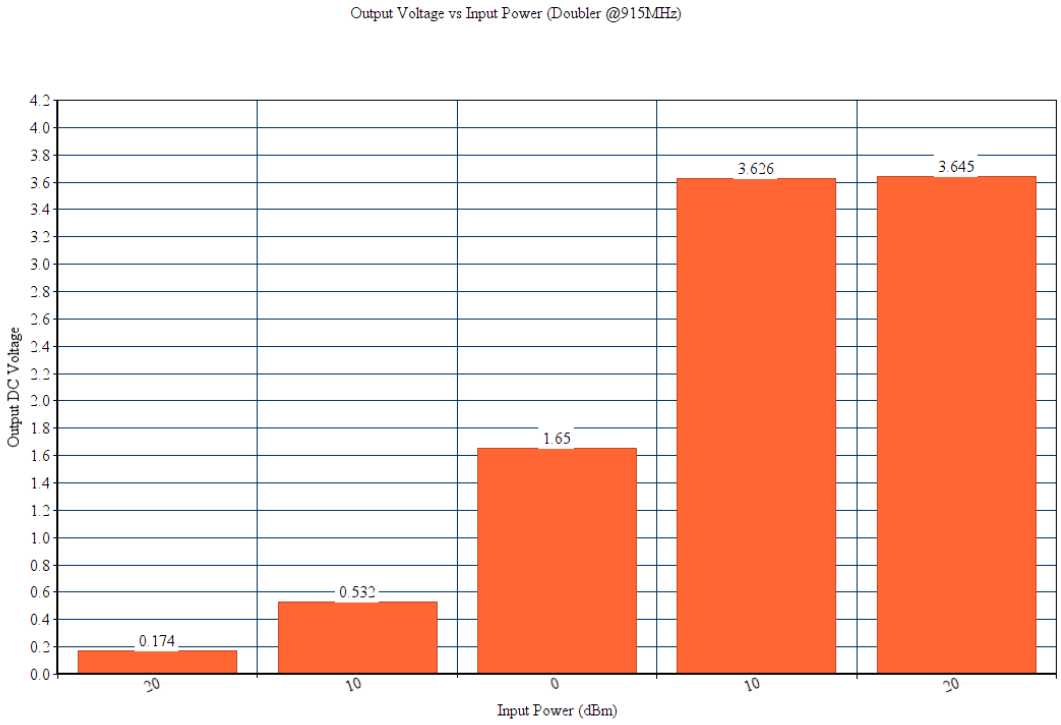

Figure 3.11: Output DC voltage vs Input Power

3.4 Voltage Tripler Results

Figure 3.12 shows the schematic of a voltage tripler circuit while figure 3.13 shows the efficiency plot and figure 3.14 shows the output voltage plot.

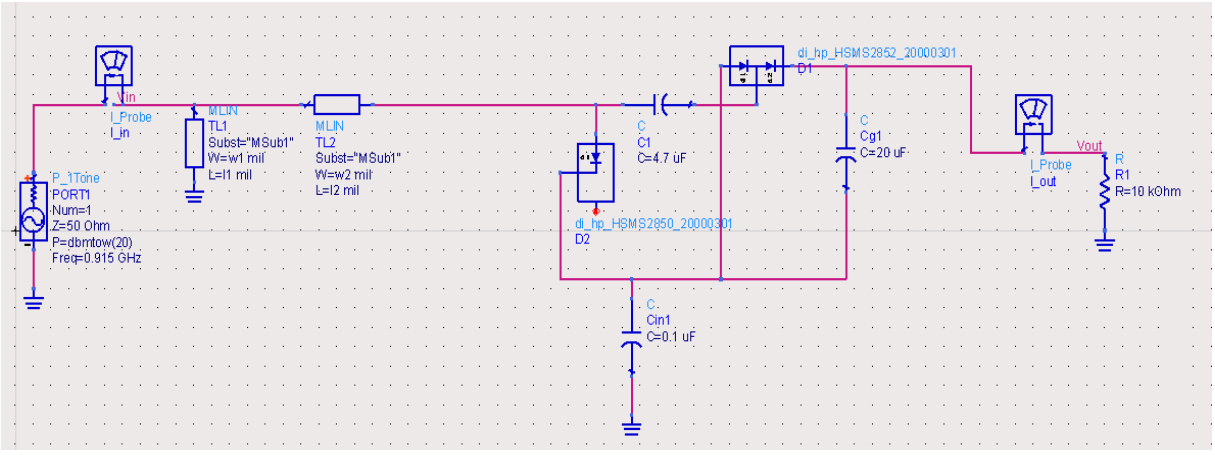

Figure 3.12: Voltage Tripler Schematic

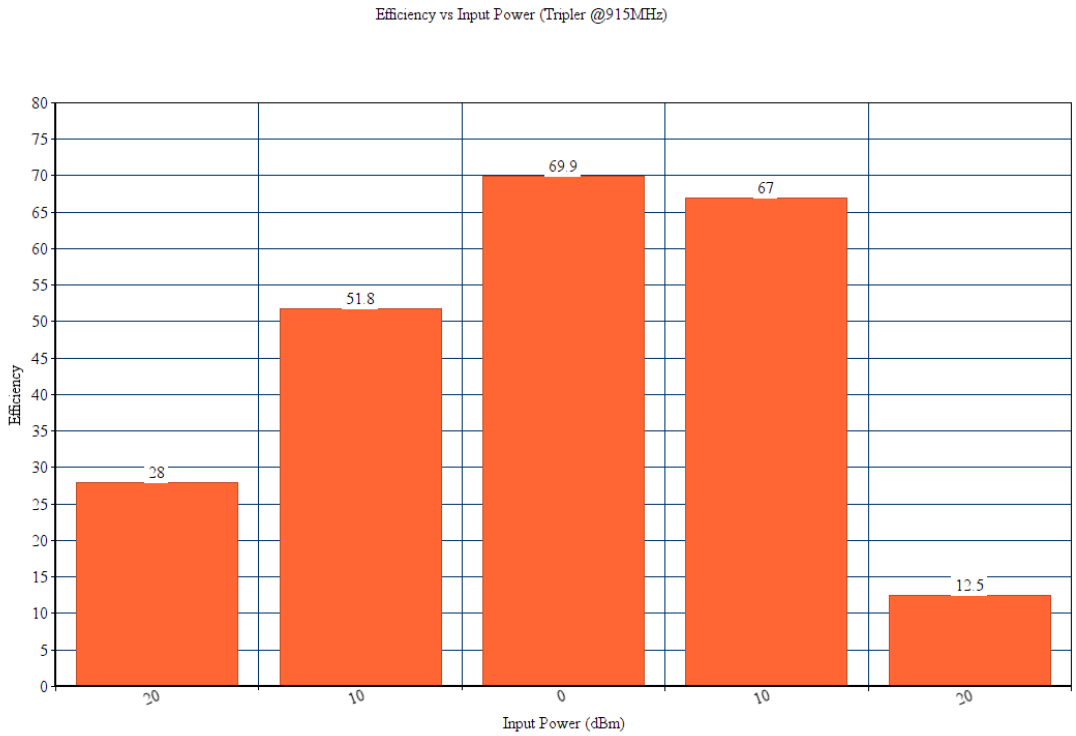

Figure 3.13: Efficiency vs Input Power

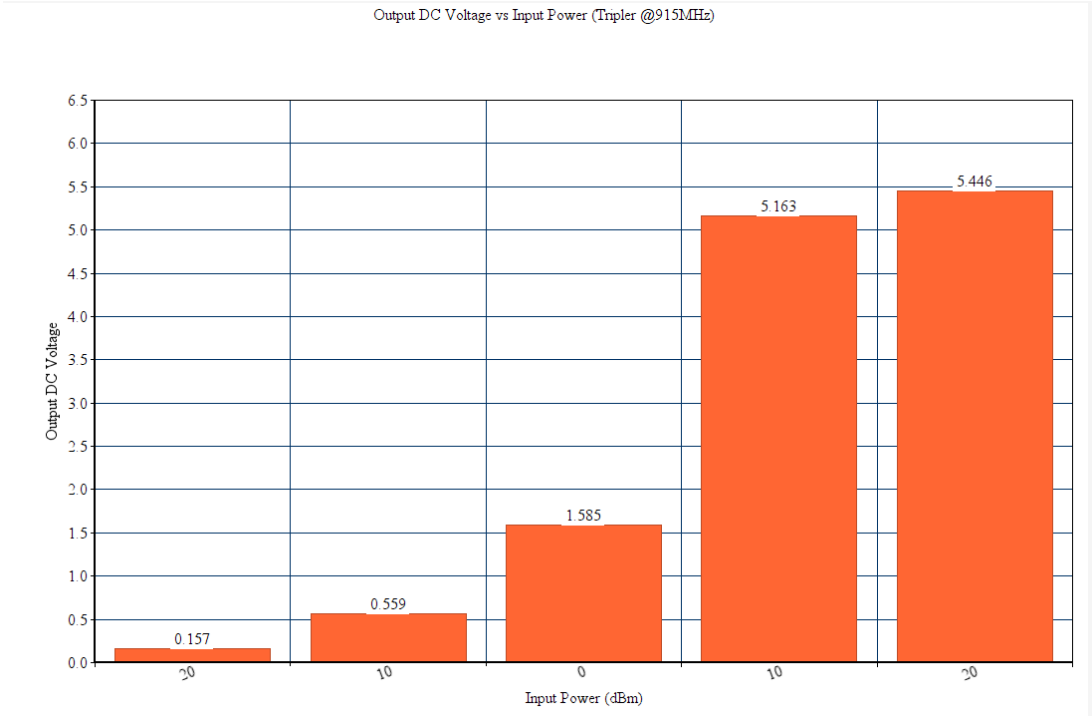

Figure 3.14: Output voltage vs Input Power

3.5 Voltage Quadrupler with inductor results

While designing voltage quadrupler in ADS 2013, we included an inductor in our design and it resulted in enhanced efficiency and output voltage value. So, we decided to include an inductor of 20nH in our design. While high value of inductor resulted in unrealisable values of transmission lines and low value resulted in less efficiency, so **there is a tradeoff in selecting inductor value**. Figure 3.15 shows the schematic of the quadrupler while figure 3.16 shows the efficiency plot and figure 3.17 shows the output voltage plot. Figure 3.18 shows the S11 plot of the quadrupler circuit. Figure 3.19 and 3.20 shows the comparison among the conventional rectifier configurations on the basis of efficiency and output voltage respectively. These two figures clearly indicate quadrupler with an inductor is the best configuration in terms of simulation results. **Hence, we have decided to prepare a final layout of the quadrupler with inductor and get it fabricated.**

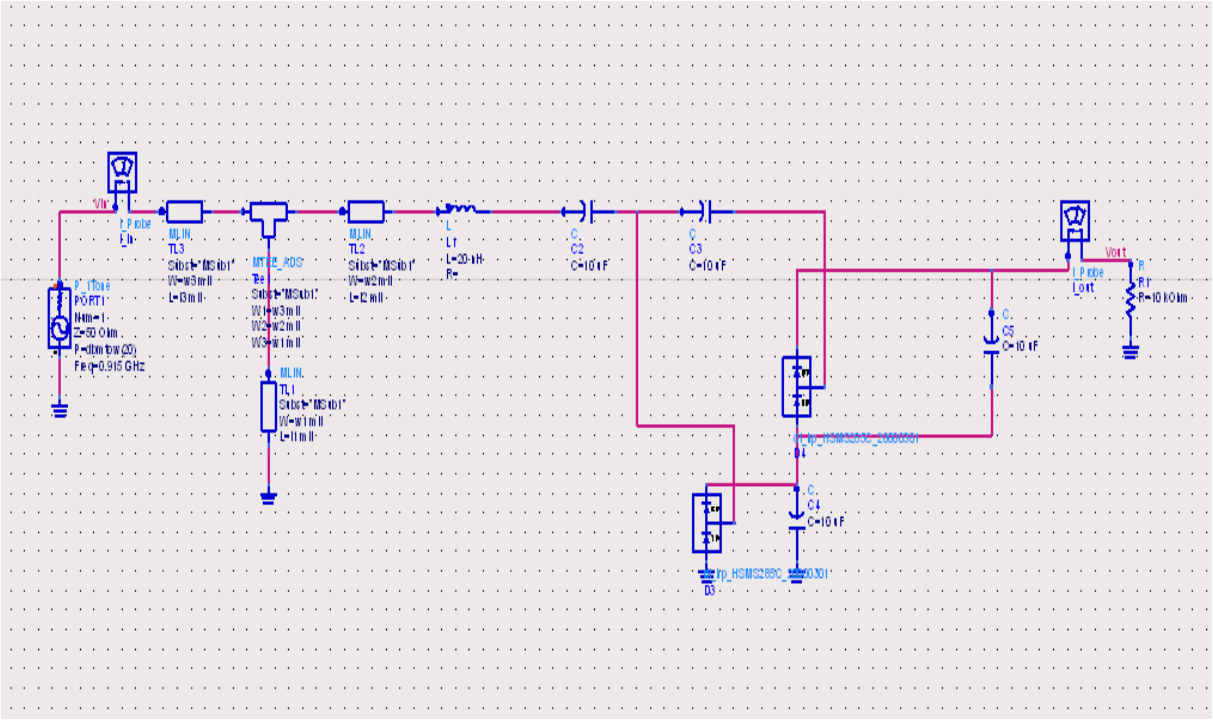

Figure 3.15: Voltage Quadrupler Schematic

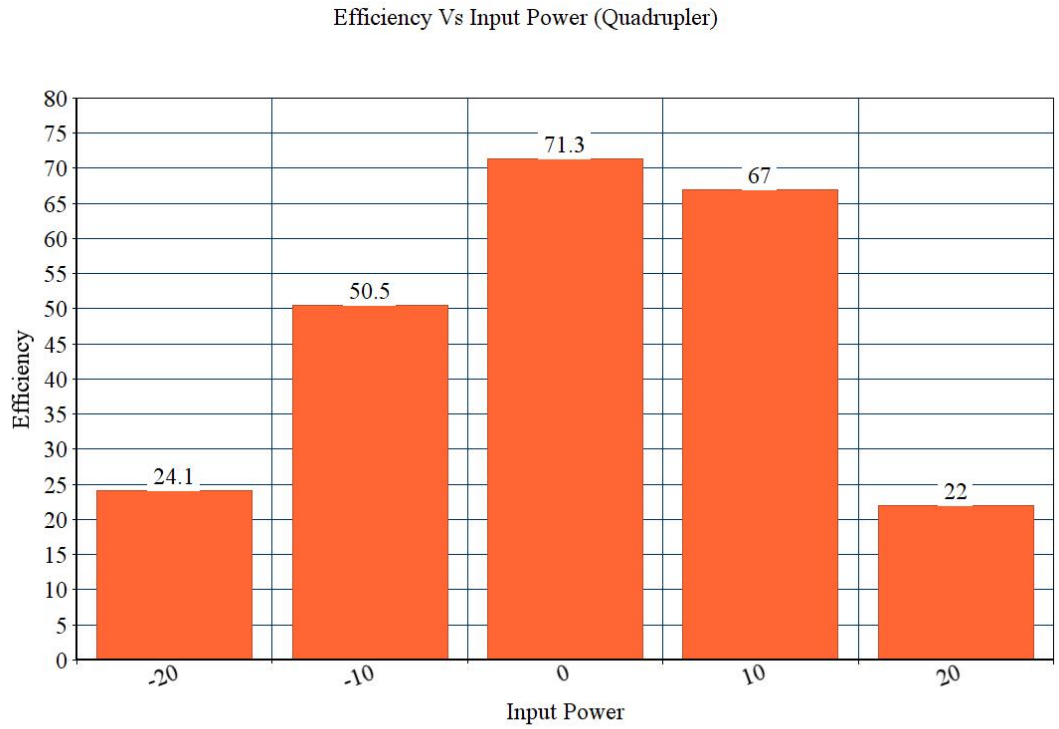

Figure 3.16: Efficiency Vs Input Power

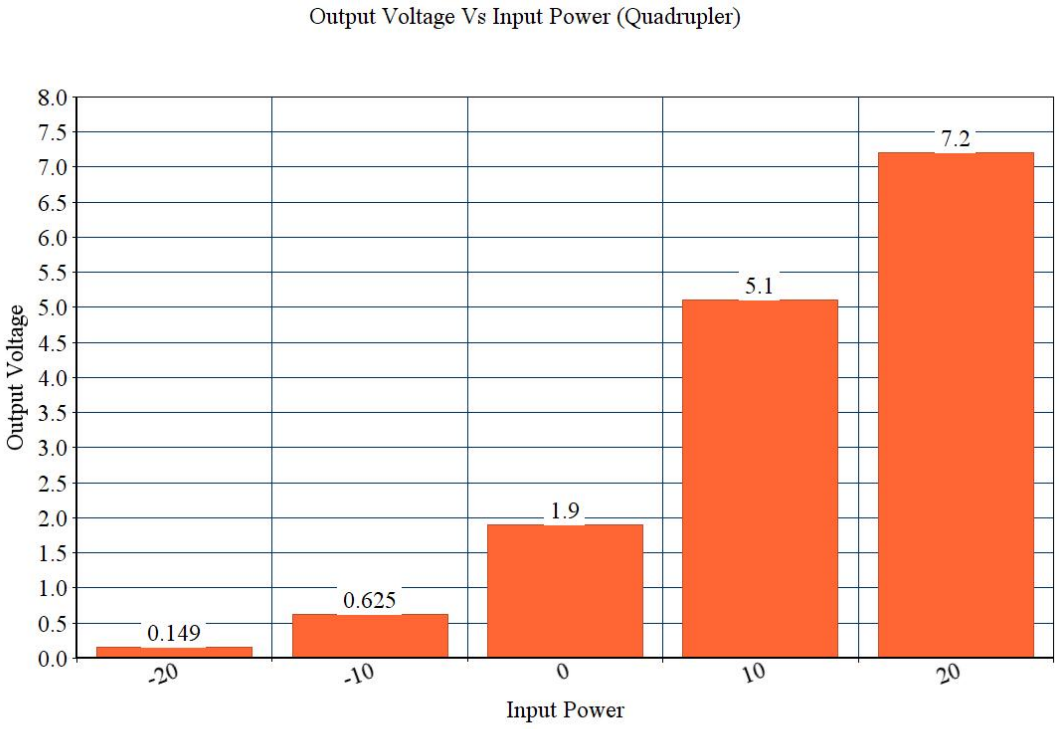

Figure 3.17: Output Voltage Vs Input Power

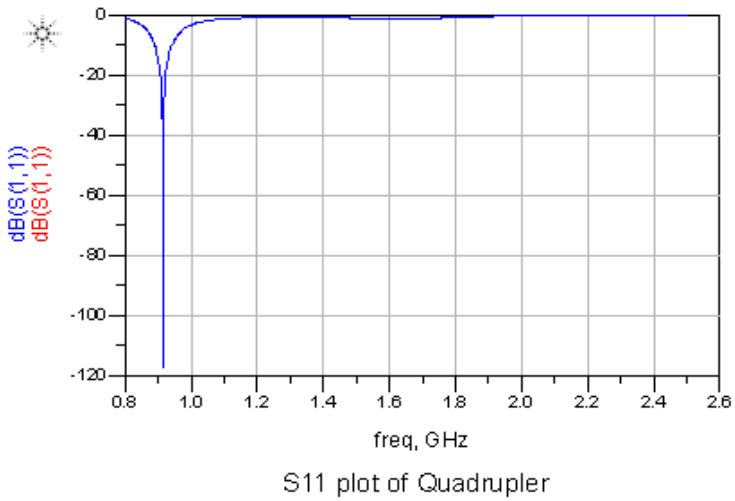

Figure 3.18: S11 plot of quadrupler

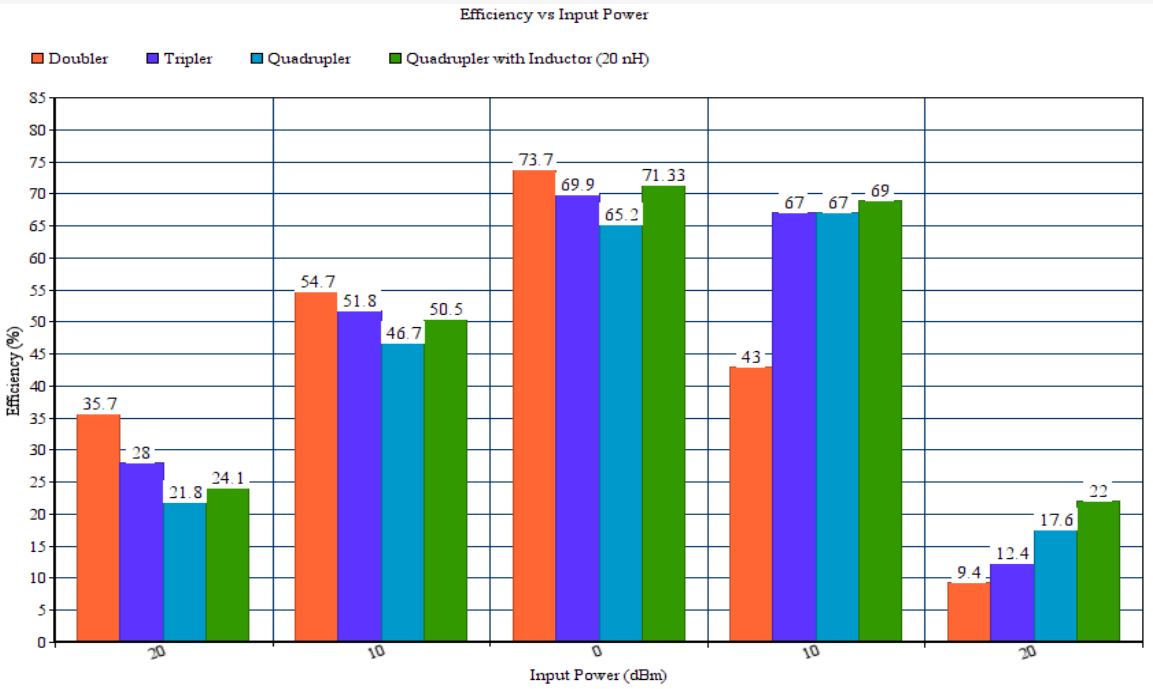

Figure 3.19: Efficiency comparison

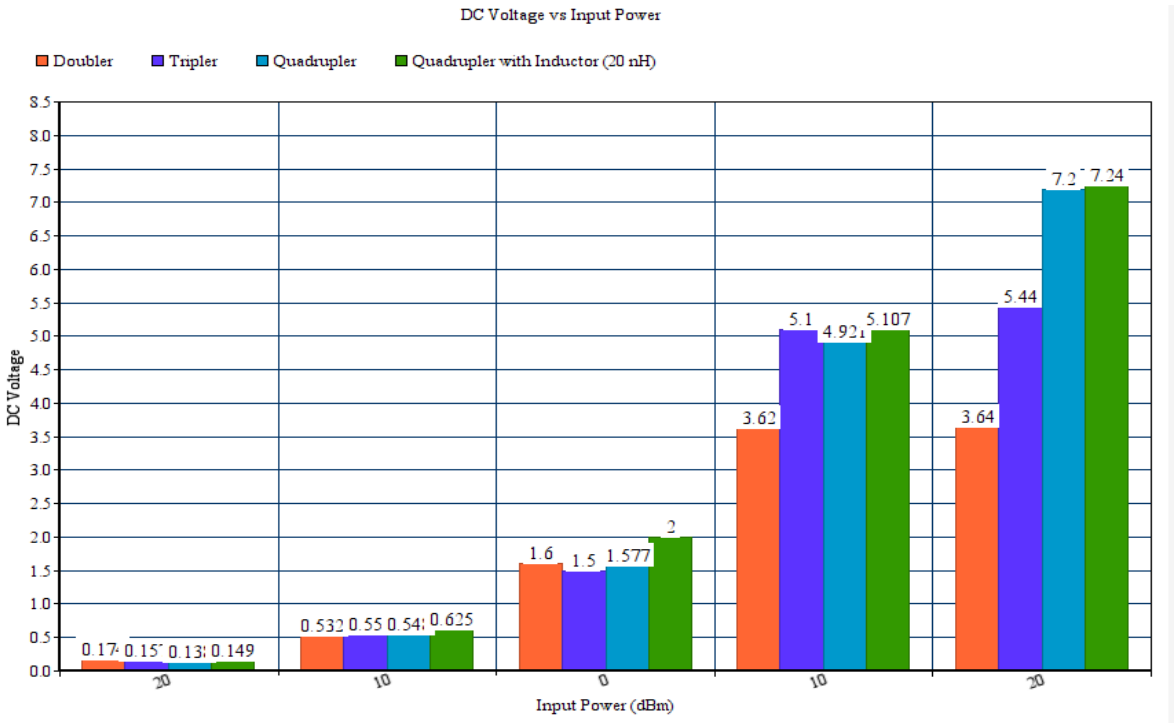

Figure 3.20: Output voltage comparison

3.6 Multi-Stage Dual-band Rectifier

As discussed in last semester presentation, we had talked about converting the single band circuit @2.1 GHz to a multi-band one. We tried to do the same but due to very high complex impedance, we werent able to get realisable transmission lines. So, we decided to implement a multi-stage rectifier and performed dual band matching on it using the paper as cited in previous chapter. We also added an inductor of 5.6nH to get enhanced efficiency and voltage value.
We did TL matching at 915 MHz (2G) and 2.42 GHz (Wifi band). Figure 3.21 shows the schematic of the circuit that was made in ADS while figure 3.22 shows the efficiencies at 915 MHz and 2.42 GHz and figure 3.23 shows the output voltages at desired frequencies. Since, we couldnt use HB simulation for both frequencies simultaneously as ADS doesnt allow that, we checked our results at a particular frequency one at a time. While doing experimentation, we will try to get 2 signal generators so that simultaneous transmission is possible and hence generated power is more than that of accumulated at one frequency.

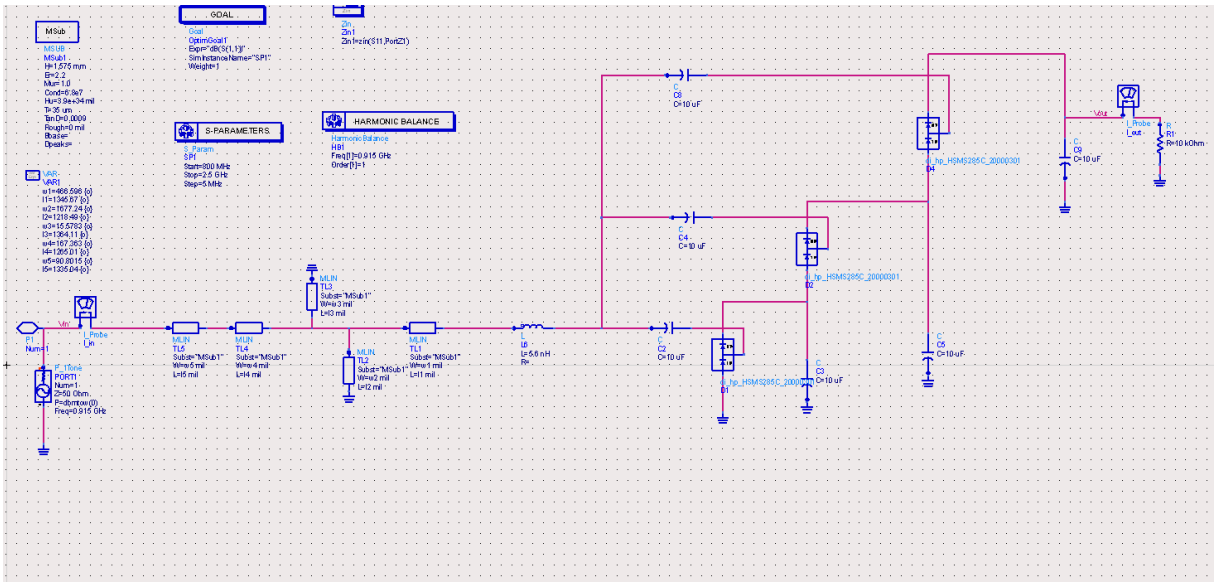

Figure 3.21: Schematic of dual band rectifier circuit

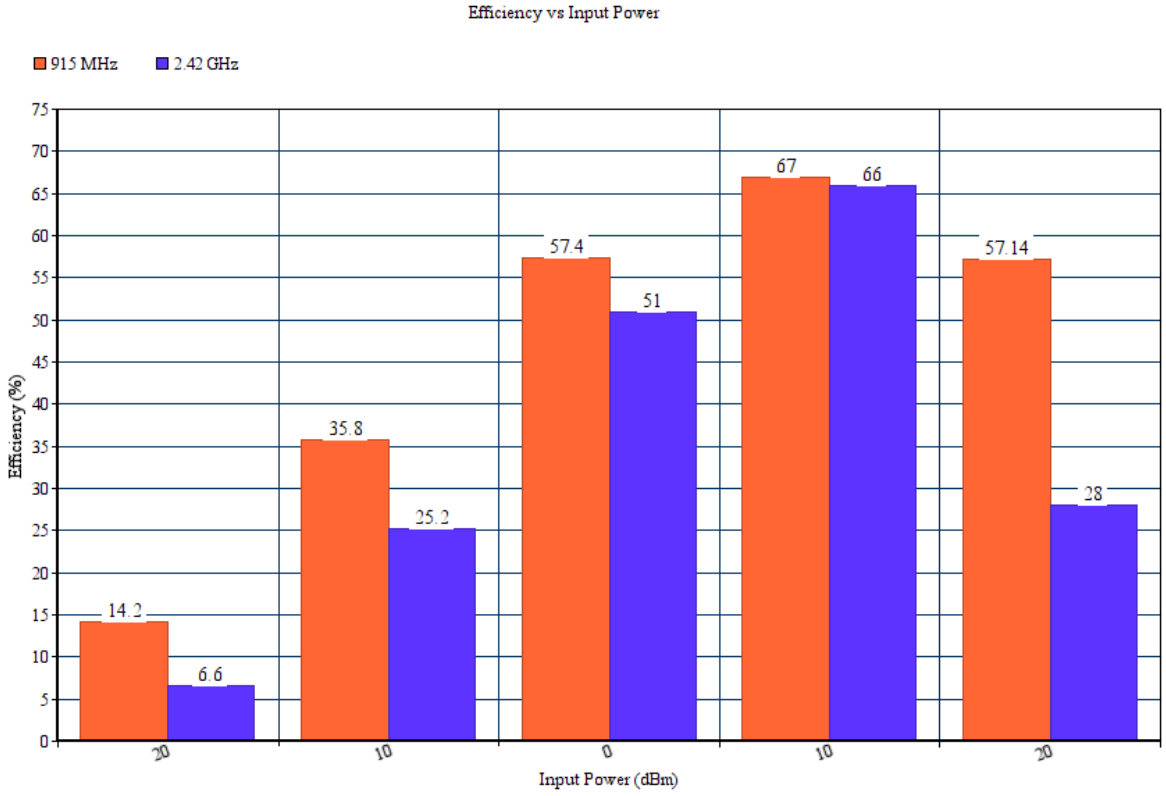

Figure 3.22: Efficiency vs Input Power

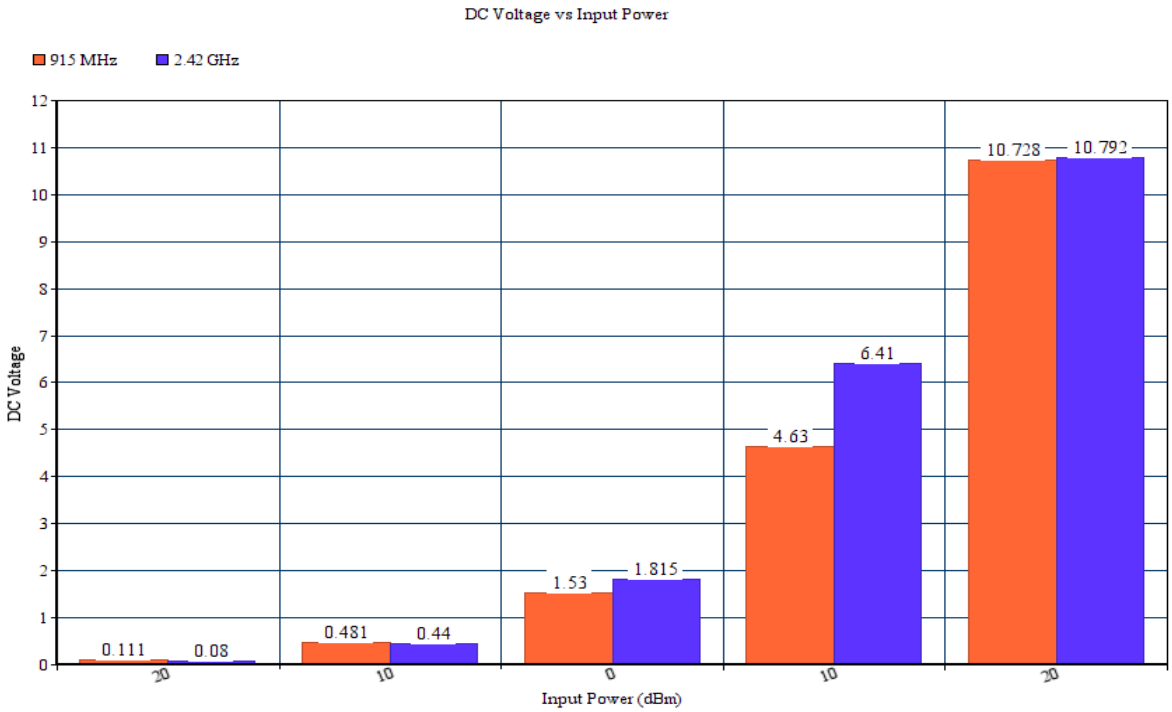

Figure 3.23: Output voltage vs Input Power

Figure 3.24 shows the S11 plot that clearly indicates matching at two desired frequencies of interest.

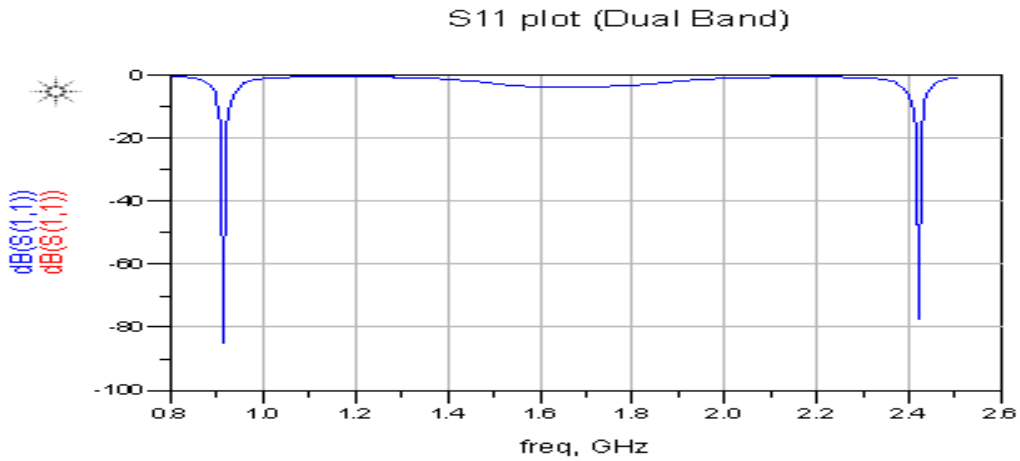

Figure 3.24: S11 plot of dual band rectifier

Hence, we have decided to prepare a final layout of this circuit too and get it fabricated. The optimisation process will decrease the voltage and efficiency values as we move towards the practical circuit implementation including using SMT components library, viaGND and TLs to solder passive elements.

Chapter 4

Conclusion and work left

Since simulation results of the quadrupler and multi-stage rectifier are much better than that of made during last semester, we have decided to give a last shot at fabricating the design and trying to generate enough voltage to glow an LED. We will be finishing with the layout preparation before BTP fair and then try to complete the fabrication and soldering process along with measurements as soon as possible. Some other things that can be done if time permits is the use of DC-DC converter(if possible) so that voltage can be hiked to a desired level which can be enough to power a sensor. This field has a lot of untapped potential and we hope that rise of IOT will also lead to many researchers and professionals working in this domain and making the final product economically viable.

[1] http://www.electronics-tutorials.ws/blog/voltage-multiplier-circuit.html

[2] Mohammad A. Maktoomi, Mohammad S. Hashmi and Vipul Panwar, *A Dual-Frequency Matching Network for FDCLs using Dual-Band $\lambda/4$-Lines*, *Progress In Electromagnetics Research Letters, Vol. 52, 2330, 2015*