

Design of Low Complexity Variable Digital Filters and Reconfigurable Filter Banks for Multi-standard Wireless Communication Receivers

SUMIT JAGDISH DARAK SCHOOL OF COMPUTER ENGINEERING 2013

Design of Low Complexity Variable Digital Filters and Reconfigurable Filter Banks for Multi-standard Wireless Communication Receivers

SUMIT JAGDISH DARAK

SCHOOL OF COMPUTER ENGINEERING

A thesis submitted to the Nanyang Technological University in partial fulfillment of the requirement for the degree of Doctor of Philosophy

2013

To my parents, sister and teachers.

Acknowledgements

It gives me great pleasure in expressing my gratitude to all those people who have supported me and had their contributions in making this thesis possible.

It is hard to overstate my gratitude to my PhD supervisor, Dr. Vinod A. Prasad. Without his inspirational guidance, encouragements and financial support, I could never finish my doctoral work in Nanyang Technological University. I remain amazed that despite his busy schedule, he was always ready to meet me for discussions and reviewed my papers and thesis drafts with comments and suggestions on almost every page. He is an inspiration.

I express my most sincere gratitude towards Dr. E. M-K Lai, Associate Professor at Massey University, Auckland, for providing me precious technical guidance throughout my PhD as well as for the financial support during conferences and internship. The six month long internship at Massey University played a major role in shaping my PhD work. Special thanks to Dr. Anoop Kumar Krishna, Senior Expert at EADS Innovation Works, for providing me an internship opportunity in the final stage of my PhD.

My acknowledgement will never be complete without the special mention of my lab mates, Dr. Mahesh, Dr. Smitha, Dr. Navin, Narendar, Neethu, Sumedh and Abhishek, for all their help and wonderful days at CHiPES. I also would like to thank CHiPES lab technical staff, Mr. Jeremiah and Ms. Merilyn, for providing an easy and quick access to lab facilities. Words fail me to express my appreciation to my best friend Mukesh for his support, generous care, motivation and the homely feeling at Singapore. *I find myself lucky to have a friend like him in my life*. It is also a pleasure to mention my good friends, Sonal, Ravikiran, Ravikishore, Manvi, Shubhadra, Manisha and Supriya. Thank you doesn't seem enough but it is said with appreciation and respect to all of them for their encouragement, precious friendship and awesome outings. PhD students often talk about loneliness but this is something which I never experienced at NTU mainly because of the warm support of all my friends. Thanks one and all.

Finally, I would like to acknowledge the people who mean world to me, my mom, dad, sister and brother-in-law. I especially thank my cousin, Yogesh, for taking good care of my parents in my absence. I consider myself the luckiest in the world to have such a supportive family, standing behind me with their love, care and support.

Abstract

Software defined radios (SDRs) and cognitive radios (CRs) empower mobile communication handsets to support multiple wireless communication standards and services, and improve the spectrum utilization efficiency. SDRs and CRs need multi-standard wireless communication receivers (MWCRs) to integrate existing as well as imminent communication standards into a single generic hardware platform. The limited reconfigurability of the analog front-end, sampling rate constraints of the currently available ADCs and extensive disparities between communication standards' specifications, lead to the shifting of stringent channel(s) selection task to the digital front-end (DFE). Thus, the DFE needs either variable digital filters (VDFs) that provide variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) responses and/or reconfigurable filter banks that provide independent and individual control over the bandwidth and the center frequency of subbands. Realizing such filters and filter banks with low area complexity, power consumption, group delay and reconfiguration delay is a challenging task. In this thesis, five VDFs and three reconfigurable filter banks have been proposed to address this research problem.

The first work is a low complexity reconfigurable filter bank based on the coefficient decimation method (CDM) and frequency response masking (FRM) (termed as CDM-FRM filter bank). It offers coarse control over the bandwidth and the center frequency of subbands. In the next work, a linear phase VDF based on modified second order frequency transformation (termed as MFT-VDF) have been proposed. The MFT-VDF, with wide cut-off frequency range, overcomes the constraint of limited cut-off frequency range in existing VDFs and also provides variable LP, HP, BP and BS responses from a

fixed-coefficient prototype filter. Using the MFT-VDF, a reconfigurable fast filter bank (RFFB) has been proposed which offers an unabridged control over subband bandwidths on a desired range, compared to the coarse control in the CDM-FRM filter bank. It also provides fine control over the center frequency of fixed bandwidth subbands which is useful in scenarios where channels have fixed bandwidth but varying center frequencies.

The implementation complexity of the filter banks can be reduced significantly if its resolution is independent of the channel bandwidth and is equal to the number of channels concurrently handled by subsequent digital signal processing algorithms. To achieve this, a filter bank which provides independent and individual control over the bandwidth and the center frequency of subbands is desired. With this goal, a new low complexity and reduced delay VDF and reconfigurable filter bank have been proposed. The linear phase VDF is designed by combining new modified CDM (MCDM) in [29] with spectral parameter approximation (SPA) (termed as SPA-MCDM VDF) while non-linear phase VDF is designed by combining the MCDM with allpass transformation (APT) (termed as APT-MCDM VDF). Both these VDFs provide variable LP, HP, BP and BS responses over entire Nyquist band and offer substantial savings in gate counts over existing VDFs. The non-linear phase APT-MCDM VDF requires less gate counts than the linear phase VDFs and is suitable for energy detection based spectrum sensing. A new APT-VDF obtained by combining first and second order APT with the CDM has been proposed which requires even less gate count than the APT-MCDM VDF.

The linear phase SPA-MCDM filter bank designed using the SPA-MCDM VDF allows independent and individual control over the bandwidth and center frequencies of subbands. The gate count and group delay comparisons show that the SPA-MCDM filter bank is superior compared to other filter banks.

Publications

Journals

- J1. S. J. Darak, A. P. Vinod and E. M-K. Lai, "A low complexity reconfigurable non-uniform filter bank for channelization in multi-standard wireless communication receivers," *Journal of Signal Processing Systems*, vol. 68, no. 1, pp. 95-111, July 2012.
- J2. S. J. Darak, A. P. Vinod, K. G. Smitha and E. M-K. Lai, "A low complexity non-uniform fast filter bank for multi-standard wireless receivers," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, accepted in May 2013.
- J3. S. J. Darak, A. P. Vinod and E. M-K. Lai, "Efficient implementation of reconfigurable warped digital filters with variable lowpass, highpass, bandpass and bandstop responses," *IEEE Transactions on Very Large Scale Integration* (VLSI) Systems, vol. 21, no. 6, pp. 1165-1169, July 2012.

Conferences

- C1. S. J. Darak, R. Mahesh, A. P. Vinod and E. M-K. Lai, "Reconfigurable uniform and semi non-uniform filter bank based on coefficient decimation, interpolation and frequency masking techniques," 17th International Conference on Telecommunications (ICT), pp. 951-956, Doha, Qatar, May2010.
- C2. S. J. Darak, A. P. Vinod and E. M-K. Lai, "A low complexity spectrum sensing scheme for estimating frequency band edges in multi-standard military communication receivers," *IEEE Conference on Communication, Science and Information Engineering (CCSIE),* London, U.K, ISBN: 978-0-9556254, July 2011, in print.

- C3. S. J. Darak, A. P. Vinod and E. M-K. Lai, "A new variable digital filter design based on fractional delays," *IEEE International Conference on Acoustics, Speech* and Signal Processing (ICASSP), pp. 1629-1632, Prague, Czech Republic, May 2011.
- C4. S. J. Darak, A. P. Vinod and E. M-K. Lai, "Design of variable linear phase FIR filters based on second order frequency transformations and coefficient decimation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3182-3185, Seoul, South Korea, May 2012.
- C5. S. J. Darak, A. P. Vinod and E. M-K. Lai, "Design of variable bandpass filters using first order allpass transformation and coefficient decimation," 18th *Electronics New Zealand Conference (ENZCON)*, New Zealand, Nov. 2011.
- C6. S. J. Darak, A. P. Vinod and E. M-K. Lai, "An area and power efficient twostage parallel spectrum sensing scheme for cognitive radios," *IEEE International Symposium on Communications and Information Technologies (ISCIT)*, pp. 263-267, Gold Coast, Australia, Oct. 2012.

Papers Under Review

- J4. S. J. Darak, A. P. Vinod, E. M-K. Lai, H. Zhang and J. Palicot, "Linear phase VDF with unabridged bandwidth control over the entire Nyquist band," resubmitted to *IEEE Transactions on Circuits and Systems-II (TCAS-II)* (major revision).
- C7. S. J. Darak, A. P. Vinod and E. M-K. Lai, "Design of low complexity and reduced delay reconfigurable filter banks using SPA-VDFs," to be submitted to *ICASSP 2014*.

Contents

A	cknov	wledgementsii
A	bstra	ctiv
Pι	ıblica	ıtionsvi
Li	st of	Figuresxii
Li	st of	Tablesxvii
Li	st of	Abbreviationsxviii
Li	st of	Symbolsxxi
1	Intr	oduction1
	1.1	Background1
	1.2	Motivation6
	1.3	Objectives and Contributions9
	1.4	Organization15
2	Literature Review: Variable Digital Filters and Reconfigurable	
	Filt	er Banks16
	2.1	Multi-standard Wireless Communication Receivers17
	2.2	Digital Front-end (DFE)21
	2.3	Literature Review: Digital Filter Banks24
		2.3.1 Filter Bank using Per-channel (PC) Approach26
		2.3.2 Modulated Filter Bank Approach27
		2.3.3 Fast Filter Banks
		2.3.4 Coefficient Decimation Method (CDM) Based Filter Banks34
	2.4	Variable Digital Filters (VDFs)
		2.4.1 Programmable Filters40

		2.4.2	Transformation Based Variable Digital Filters	41
			(a) Allpass Transformation Based Variable Digital Filter	s41
			(b) Frequency Transformation Based Variable Digital Fi	lters44
		2.4.3	Spectral Parameter Approximation Based VDFs	47
		2.4.4	Frequency Response Masking Based VDFs	50
		2.4.5	Coefficient Decimation Based VDFs	54
	2.5	Sum	mary	55
3	Rec	onfigu	rrable Filter Bank Based on Coefficient Decimation Meth	od
	and	Frequ	uency Response Masking	58
	3.1	Coef	fficient Decimation Method and Interpolation Technique	59
	3.2	Prop	oosed CDM-FRM Filter Bank	61
		3.2.1	First Stage – Design of Prototype Filter	63
		3.2.2	Second Stage – Design of Masking Filter	66
		3.2.3	Third Stage – Adder Block	68
	3.3	Arch	nitecture of CDM-FRM Filter Bank	69
	3.4	Impl	lementation Complexity Comparison	
	3.5	Appl	lication: Non-uniform Channelization	81
	3.6	Appl	lication: Detection of Frequency Band Edges	85
		3.6.1	CDM-FRM Filter Bank Based Energy Detector	86
		3.6.2	Edge Detection Algorithm	89
		3.6.3	Simulation Results and Complexity Analysis	91
			(a) Error vs. Complexity	92
			(b) Error vs. Detection Time	
	3.7	Sum	mary	94
4	Lov	v Com	plexity Reconfigurable Fast Filter Bank	96
	4.1	Revi	iew of Variable Digital Filters (VDFs)	97
	4.2	Mod	lified Farrow Structure Based Variable Digital Filter	98

		4.2.1	Relation Between Cut-off Frequency, Fractional Delay (FD)	
			and Transition Bandwidth (TBW)	99
		4.2.2	Selection of Fractional Delay (FD) Structure	101
		4.2.3	Design Example	104
		4.2.4	Conclusion	105
	4.3	Frequ	uency Transformation Based Variable Digital Filters	107
	4.4	Mod	ified Frequency Transformation Based Variable Digital Filter	110
		4.4.1	Architecture of the MFT-VDF	110
		4.4.2	Design Example	111
		4.4.3	Implementation Complexity Comparison	113
	4.5	Prop	osed Reconfigurable Filter Bank (RFFB)	114
		4.5.1	First Stage – Variable Digital Filter	115
		4.5.2	Remaining (k-1) Stages – Fixed-coefficient Sub-filters	117
		4.5.3	Design Example	119
		4.5.4	Implementation Complexity	122
	4.6	Sum	mary	124
5	Mo	dified	CDM Based Variable Digital Filters and Reconfigurable	
	Filt	er Ban	ks	127
	5.1	Prop	osed Modified CDM Based Variable Digital Filter and	
		Reco	nfigurable Filter Bank	128
		5.1.1	Modified Coefficient Decimation Method-I (MCDM-I)	129
		5.1.2	Basic Principle	133
		5.1.3	Selection of Prototype Variable digital Filter	139
			(a) First Order Allpass Transformation Based Variable	
			Digital Filters	141
			(b) Spectral Parameter Approximation Based Variable	
			Digital Filter	143
		5.1.4	Proposed Variable Digital Filter Architectures	145

	5.2	Complexity Comparison For Variable Digital Filters	147
	5.3	Complexity Comparison For Filter Banks	152
	5.4	Combined Channelization and Spectrum Sensing	156
	5.5	Filter Bank For Digital Hearing Aids	. 159
	5.6	Summary	. 160
6	Red	uced Second Order Allpass Transformation Based Variable	
	Digi	ital Filters	.162
	6.1	Allpass Transformation Based Variable Digital Filters	163
	6.2	Proposed Variable Digital Filter	. 166
		6.2.1 Design of the APT-CDM VDF	167
		6.2.2 Mathematical Derivation	. 169
	6.3	Design Example	170
	6.4	Implementation Complexity	173
	6.5	Applications	. 175
		6.5.1 Application 1: Energy Detection Based Spectrum Sensing	.175
		6.5.2 Application 2: Audio Signal Processing	. 176
	6.6	Filter Bank Complexity Comparisons	178
	6.7	Summary	. 179
7	Con	clusions and Future Works	180
	7.1	Conclusions	180
	7.2	Future Work	. 189
		7.2.1 Exploiting the Redundancies in SPA-VDF Architecture	189
		7.2.2 Low Complexity Variable Fractional Delay (VFD) Filters	. 190
		7.2.3 Area and Power Efficient Two-Stage Spectrum Sensing	191
Bi	bliog	raphy	. 193

List of Figures

1.1	A multi-standard wireless communication receiver architecture4
2.1	A feasible multi-standard wireless communication receiver (MWCR)17
2.2	Illustration of channelization and spectrum sensing tasks in the
	DFE of MWCRs
2.3	Filter bank using per-channel (PC) approach
2.4	Discrete Fourier transform filter bank (DFTFB)
2.5	Modulated perfect-reconstruction filter bank (MPRFB)30
2.6	Variable cut-off frequency responses obtained using the CDM-II31
2.7	Coefficient decimation based DFT filter bank (CDM-DFTFB)32
2.8	16-subband fast filter bank (FFB)
2.9 (a)	Frequency response of the prototype filter
2.9 (b)	Frequency responses obtained using the CDM-I from prototype
	filter in (a) for $D_I = 2$ and $D_{II} = 1, 2, 3$
2.9 (c)	Frequency responses obtained using the CDM-I from prototype
	filter in (a) for $D_I = 4$ and $D_{II} = 1, 2, 3$
2.10	Progressive decimation filter bank
2.11	Allpass transformation based variable digital filter (APT-VDF)
2.12	First order allpass transformation
2.13	<i>P</i> th order frequency transformation based VDF
2.14	<i>P</i> th order frequency transformation
2.15	Spectral parameter approximation based VDF with FIR sub-filters
	in transposed direct form

2.16	Sharp TBW digital filter based on the FRM technique51
2.17	Frequency response illustration of the FRM technique51
2.18	SPA-FRM VDF53
3.1 (a)	Frequency response of the prototype filter
3.1 (b)	Frequency response obtained from filter in (a) using the CDM-I
	for $D_I = 2$
3.1 (c)	Frequency response obtained from filter in (a) using the CDM-I
	for $D_I = 4$
3.1 (d)	Frequency response obtained from filter in (a) using the CDM-II
	for $D_{II} = 2$
3.1 (e)	Frequency response obtained by interpolating the filter in (a)
	by <i>M</i> = 860
3.2	Block diagram of the CDM-FRM filter bank
3.3	Multi-band responses obtained using first stage of the CDM-FRM
	filter bank65
3.4	Frequency responses of prototype and complementary filters of
	the CDM-FRM filter bank for different values of D_{II}
3.5	Frequency plot indicating the passband and stopband frequencies
	of masking filters when $D_{II} = D_{IImax}$
3.6	Simulink diagram of the CDM-FRM filter bank Architecture69
3.7	Simulink diagram of the three stages of the CDM-FRM filter bank70
3.8	Architecture of the prototype filter71
3.9	Architecture of masking filter bank (Bank 1)73
3.10	Architecture of masking filter bank (Bank 2)73
3.11	Architecture of the Adder block75
3.12 (a)	Input signal
3.12 (b)-(f)	Extracted channels using the CDM-FRM filter bank

3.13 (b)-(e)	Extracted channels using the CDM-FRM filter bank	33
3.14 (a)	Input signal	34
3.14 (b)-(e)	Extracted channels using the CDM-FRM filter bank	35
3.15 (a)	Input signal	34
3.15 (b)-(d)	Extracted channels using the CDM-FRM filter bank	34
3.16	The CDM-FRM filter bank based spectrum sensing scheme	37
3.17	Illustrative frequency responses of filter bank, (a) Prototype filter	
	response (b) Complementary filter response	39
3.18	Percentage error vs. complexity comparison) 3
3.19	Percentage error vs. detection time comparison	94
4.1	Proposed fractional delay based variable digital filter) 9
4.2 (a)	Second order modified Farrow structure of Lagrange Interpolation	104
4.2 (b)	Proposed MF-VDF	104
4.3 (a)	Variable cut-off frequency responses obtained using the MF-VDF	106
4.3 (b)	Phase delay responses of the MF-VDF	106
4.4 (a)	Second order frequency transformation based VDF	109
4.4 (b)	Second order frequency transformation	109
4.5	Architecture of the MFT-VDF	111
4.6	Variable lowpass response range for the MFT-VDF and the VDF	
	in [40]	112
4.7	Variable bandpass responses obtained using the MFT-VDF	113
4.8	Proposed reconfigurable fast filter bank (RFFB)	115
4.9 (a)	Response of the MFT-VDF	118
4.9 (b)	Original response, <i>O</i> ₁	118
4.9 (c)	Complementary response, <i>C</i> ₁	118
4.10	Variable bandwidth responses for subband 9 obtained using the RFFB	120
4.11	Uniform bandwidth responses using the RFFB	121
4.12	Variable center frequency responses using the RFFB	121

5.1 (a)	Frequency response of lowpass prototype filter131
5.1 (b)	Original and complementary frequency responses using the
	MCDM-I with $D_I = 1$
5.1 (c)	Original and complementary frequency responses using the
	CDM-I with $D_I = 2$
5.1 (d)	Original and complementary frequency responses using the
	MCDM-I with $D_I = 2$
5.2 (a)	Frequency response of lowpass prototype VDF, $H_{\alpha}(z)$ 134
5.2 (b)	Frequency response, $H_{\alpha 1}^{m}(z)$, obtained using MCDM-I with $D_{I} = 1$ 134
5.2 (c)	Complementary response, $H^m_{\alpha c1}(z)$
5.2 (d)	Frequency response, $H_{\alpha 2}^{m}(z)$, obtained using MCDM-I with $D_{I} = 2134$
5.2 (e)	Complementary response, $H^m_{\alpha c2}(z)$
5.2 (f)	Frequency response of masking filter, $H_m(z)$
5.2 (g)	Frequency response of 134
	$[H^m_{\alpha c2}(\mathbf{z})H_m(\mathbf{z})]$
5.2 (h)	$[H_{\alpha c2}^{m}(z)H_{m}(z)]$ Frequency response of $[H_{\alpha c2}^{m}(z)H_{m}(z)+H_{\alpha 2}^{m}(z)]$
5.2 (h) 5.3	$[H^m_{\alpha c2}(z)H_m(z)]$ 134 Frequency response of $[H^m_{\alpha c2}(z)H_m(z) + H^m_{\alpha 2}(z)]$ 134 Frequency response illustration of a 4-subband reconfigurable
5.2 (h) 5.3	$[H^{m}_{\alpha c2}(z)H_{m}(z)]$ Frequency response of $[H^{m}_{\alpha c2}(z)H_{m}(z)+H^{m}_{\alpha 2}(z)]$ 134 Frequency response illustration of a 4-subband reconfigurable filter bank137
5.2 (h) 5.3 5.4	$[H^{m}_{\alpha c2}(z)H_{m}(z)]$ Frequency response of $[H^{m}_{\alpha c2}(z)H_{m}(z)+H^{m}_{\alpha 2}(z)]$ 134 Frequency response illustration of a 4-subband reconfigurable filter bank137 APT-VDF, $H_{\alpha}(z)$ 142
5.2 (h) 5.3 5.4 5.5	$ [H^m_{\alpha c2}(z)H_m(z)] 134 $ Frequency response of $[H^m_{\alpha c2}(z)H_m(z) + H^m_{\alpha 2}(z)] 134 $ Frequency response illustration of a 4-subband reconfigurable filter bank 137 APT-VDF, $H_{\alpha}(z)$ 142 First order allpass transformation, $A(z)$ 142
5.2 (h) 5.3 5.4 5.5 5.6	$[H^m_{\alpha c2}(z)H_m(z)]$
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a)	$[H^m_{\alpha c2}(z)H_m(z)]134$ Frequency response of $[H^m_{\alpha c2}(z)H_m(z)+H^m_{\alpha 2}(z)]134$ Frequency response illustration of a 4-subband reconfigurable filter bank137 APT-VDF, $H_a(z)$ 142 First order allpass transformation, $A(z)$ 142 The SPA-VDF with FIR sub-filters in transposed direct form143 Architecture of the SPA-MCDM VDF146
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a) 5.7 (b)	$[H^m_{\alpha c2}(z)H_m(z)]134$ Frequency response of $[H^m_{\alpha c2}(z)H_m(z)+H^m_{\alpha 2}(z)]134$ Frequency response illustration of a 4-subband reconfigurable filter bank137 APT-VDF, $H_{\alpha}(z)$ 142 First order allpass transformation, $A(z)$ 142 The SPA-VDF with FIR sub-filters in transposed direct form143 Architecture of the SPA-MCDM VDF146
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a) 5.7 (b) 5.8	$[H^m_{\alpha c2}(z)H_m(z)]$
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a) 5.7 (b) 5.8 5.9	$[H^m_{\alpha c2}(z)H_m(z)]$
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a) 5.7 (b) 5.8 5.9 5.10	$[H^m_{\alpha c2}(z)H_m(z)]$
5.2 (h) 5.3 5.4 5.5 5.6 5.7 (a) 5.7 (b) 5.8 5.9 5.10	$[H^m_{ac2}(z)H_m(z)]$

5.12	Combined channelization and spectrum sensing approach157
5.13	Gate count of filter bank vs. number of subbands processed158
6.1	Variable bandpass responses using the APT-VDF where $ \alpha < 1$ 163
6.2	Variable bandpass responses using the APT-VDF with bandpass
	prototype filter, first order APT and the CDM-II164
6.3	Proposed APT-CDM VDF167
6.4	Variable lowpass responses using the APT-CDM VDF171
6.5	Variable bandpass responses using the APT-CDM VDF for $\alpha = 0.15171$
6.6	Variable bandpass responses using the APT-CDM VDF for $\alpha = -0.15172$
6.7	Variable bandpass responses using second design example
	for $\alpha = -0.55$
6.8	Relation between APT coefficient, α and desired center frequency of
	bandpass response (<i>f_{center}</i>)
6.9	Total gate count vs. number of VDF outputs (Number of energy
	detectors)177
6.10	Total gate count vs. number of subbands 178
7.1	SPA-VDF
7.2	Modified SPA-VDF189

List of Tables

1.1	Bandwidth parameters of different communication standards	3
1.2	Summary of contributions presented in this thesis	14
2.1	Comparison of different linear phase filter banks	38
2.2	Comparison of different VDFs	56
3.1	Specifications of channels extracted by Adder block for different values of	
	Sel_band	76
3.2	Gate count complexity comparison of CDM-FRM filter bank with other	
	Filter banks	79
3.3	Implementation complexity comparison for CDM-FRM filter bank	81
3.4	Bandwidth and MSE for different channels	82
3.5	Channel edge frequencies	92
4.1	Gate count complexity comparison of MFT-VDF with other VDFs	113
4.2	Gate count complexity comparison of RFFB with other filter banks	123
5.1	Gate count complexity comparison of variable digital filter	148
5.2	Gate count complexity comparison of filter banks	153
5.3	Gate count complexity comparison of combined channelization and	
	spectrum sensing approaches	158
5.4	Gate count complexity comparison for 3-subband filter banks	159
6.1	Gate count complexity comparison of APT-VDFs	174
6.2	Gate count comparison of APT-CDM VDF, APT-MCDM VDF and	
	SPA-MCDM-VDF	176
7.1	Comparison of different VDFs	187
7.2	Comparison of different linear phase filter banks	188

List of Abbreviations

ADC	Analog-to-digital Converter
APT	All Pass Transformation
ASIC	Application Specific Integrated Circuits
BP	Bandpass
BS	Bandstop
BW	Bandwidth
CDM	Coefficient Decimation Method
CDM-DFTFB	Coefficient Decimation Method based Discrete Fourier Transform
	Filter Bank
CDMA	Code Division Multiple Access
CFD	Cyclostationary Feature Detector
CR	Cognitive Radio
DAC	Digital-to-analog Converter
DC	0 Hz
DFE	Digital Front-end
DFT	Discrete Fourier Transform
DFTFB	Discrete Fourier Transform Filter Bank
DSP	Digital Signal Processing
FD	Fractional Delay
FFB	Fast Filter Bank
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FRM	Frequency Response Masking

GDB	Goertzel Filter Bank
GHz	Gigahertz
GSM	Global System for Mobile Communications
GSPS	Giga Samples Per Second
HP	Highpass
HSPA	High Speed Packet Access
IIR	Infinite Impulse Response
KHz	Kilohertz
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Lowpass
LTE	Long Term Evolution
LUT	Look-up Table
MCDM	Modified Coefficient Decimation Method
MF	Modified Farrow
MFT	Modified Frequency Transform
MHz	Megahertz
mi	Miles
MMCR	Multi-standard Military Communication Receiver
MPRFB	Modified Perfect Reconstruction Filter Bank
MWCR	Multi-standard Wireless Communication Receiver
OLU	Output Logic Unit
PC	Per-Channel
RF	Radio Frequency
RFFB	Reconfigurable Fast Filter Bank
SDR	Software Defined Radio
SNR	Signal-to-Noise Ratio
SPA	Spectral Parameter Approximation

TBW	Transition Band Width	
TDFTFB	Tree-Structured Discrete Fourier Transform Filter Bank	
TQMFB	Tree-structured Quadrature Mirror Filter Bank	
UMTS	Universal Mobile Telecommunication Systems	
VDF	Variable Digital Filter	
VFD	Variable Fractional Delay	
W-CDMA	Wideband Code Division Multiple Access	
WiMAX	Worldwide Interoperability for Microwave Access	
WLAN	Wireless Local Area Network	

List of Symbols

δ_p	Passband ripple
δ_s	Stopband ripple
Δf	Transition bandwidth
Ω_c	Cut-off frequency of $H_P(Z)$
Ω_{c1}	Lower cut-off frequency of $H_P(Z)$
Ω_{c2}	Upper cut-off frequency of $H_P(Z)$
$\theta_c(\omega)$	Phase response of first order allpass transformation
β	Minimum subband bandwidth of the CDM-FRM filter bank
α	Control parameter of APT-VDF, SPA-VDF, APT-MCDM VDF and SPA-
	MCDM VDF
A_k	Frequency transformation coefficients in MFT-VDF
A(z)	First order allpass transformation
B(z)	Second order allpass transformation
$B_r(z)$	Reduced second order allpass transformation
BW_{c1}	Bandwidth of subbands in complementary response
<i>BW</i> ₀₁	Bandwidth of subbands in original response
BW _{min}	Minimum subband bandwidth of RFFB
BW _{max}	Maximum subband bandwidth of RFFB
D	Total delay
d	Fractional part of delay, D
D_I	CDM-I or MCDM-I factor

D_{II}	CDM-II or MCDM-II factor
D _{IImax}	Maximum value of CDM-II or MCDM-II factor
D _{IImin}	Minimum value of CDM-II or MCDM-II factor
E_{χ}	Signal energy in the subband x
factual	Actual edge frequency of channel in hertz
f_{approx}	Approximate edge frequency of channel in hertz
f_c	Cut-off frequency in hertz
f_{c0}	Cut-off frequency of prototype filter of APT-VDF
$f_{c\alpha}$	Cut-off frequency of APT-VDF
f_{cD}	Cut-off frequency of MF-VDF
f_{cD1}	Lower cut-off frequency of MF-VDF
f_{cD2}	Upper cut-off frequency of MF-VDF
f _{cM}	Falling frequency band edge of <i>M</i> th subband of SPA-MCDM filter bank
fcenter	Center frequency in hertz
f _{pass}	Passband frequency in hertz
$f_{pass(max)}$	Maximum passband frequency of prototype filter of CDM-FRM filter bank
$f_{pass(min)}$	Minimum passband frequency of prototype filter of CDM-FRM filter bank
$f_{p(mask)}$	Passband frequency of masking filter in hertz
f_s	Sampling frequency
f_{stop}	Stopband frequency in hertz
$f_{s(mask)}$	Stopband frequency of masking filter in hertz
G(z)	Transfer function of APT-VDF
h_n	Impulse response coefficients of digital filter
$h_k(n)$	Impulse response coefficients of k^{th} digital filter

- H(z) Transfer function of prototype filter
- $H(e^{i\omega})$ Fourier transform of prototype filter
- $H(z, \alpha)$ Transfer function of SPA-VDF
- $H_{\alpha}(z)$ Transfer function of prototype filter
- $H_{\alpha}(z^{M})$ Transfer function of interpolated prototype filter
- $H_{\alpha}\left(z^{M/D_{II}}\right)$ Transfer function of interpolated and coefficient decimated prototype filter
- $H_c(z)$ Transfer function of complementary filter
- $H_c(z^M)$ Transfer function of interpolated complementary filter
- $H_c(z^{M/D_{II}})$ Transfer function of interpolated and coefficient decimated complementary filter
- $H_{D_I}(z)$ Transfer function of coefficient decimated digital filter
- $H_{D_I}(e^{i\omega})$ Fourier transform of coefficient decimated digital filter
- $H_{D_I}^m(z)$ Transfer function of modified coefficient decimated digital filter
- $H_{D_{i}}^{m}(e^{i\omega})$ Fourier transform of modified coefficient decimated digital filter
- $H^m_{\alpha D_{II}k}(z)$ Transfer function of SPA-MCDM VDF or APT-MCDM VDF
- $H_m(z)$ Transfer function of masking filter of SPA-MCDM VDF
- $H_m(e^{i\omega})$ Fourier transform of masking filter of SPA-MCDM VDF
- $H_{ma}(z)$ Transfer function of masking filter for prototype filter of FRM
- $H_{mc}(z)$ Transfer function of masking filter for complementary filter fRM
- $H_P(z)$ Transfer function of VDF based on P^{th} order frequency transformation
- *k* Number of stages of RFFB
- *L* Number of sub-filters in SPA-MCDM VDF
- *M* Interpolation factor (chapter 3 and 4)

Μ	Resolution of proposed filter bank (chapter 5)
Ν	Order of prototype filter
N _D	Effective order of MF-VDF for delay D
N _{fd}	Order of FIR FD structure
N _{FIR}	Order of finite impulse response digital filter
P_{DM}	Decision metric for subband M and decimation factor D_{II}
P _d	Probability of detection
P _{fa}	Probability of false alarm
S _{ec}	Samples of extracted channel
S _{in}	Samples of input signal
$ au_p(\omega)$	Phase delay
T ₀	Threshold for the energy detector
ω _c	Cut-off frequency in rad/sec
ω_{c0}	Cut-off frequency of prototype filter of APT-VDF in rad/sec
ω _{cα}	Cut-off frequency of APT-VDF in rad/sec
ω_{c1}	Upper cut-off frequency in rad/sec
ω_{c2}	Lower cut-off frequency in rad/sec
ω_{cpa}	Cut-off frequency of prototype SPA-VDF of SPA-MCDM VDF
<i>x</i> (<i>n</i>)	Input signal to the filter or filter bank
<i>y</i> (<i>n</i>)	Output signal of the filter
Y(z)	Frequency response of the filter's output
$Y_k(z)$	Frequency response of the k^{th} subband of the filter bank
$Y_{kl}(z)$	Frequency response of the combined k^{th} and l^{th} subband of the filter bank
z^{-N}	N unit delays

Chapter 1 Introduction

1.1 Background

Mobile communication is one of the fastest growing fields in the world over the last three decades in terms of number of benefitted customers as well as technological breakthroughs starting from short text message transfer service to the cellphone games and revolutionizing voice telephony services. This is followed by more exciting and beneficial mobile internet access as well as data transfer add-on services and at present video calling services bringing the world virtually close to each other. The advancements in mobile communications have also made prominent impact on improving education, health, public safety, disaster management, banking services etc [1]. Research in mobile communications is very active in order to improve the connectivity and the range of services, with the vision of realizing next-generation cellphone as a most secured point of contact of humans with the outside world.

A number of mobile communication standards or protocols have been developed to facilitate wide range of services. For example, Global System for Mobile Communications (GSM), Code Division Multiple Access (CDMA) and Universal Mobile Telecommunications System (UMTS) support voice communication. Standards such as wireless local area networks (WLAN), Worldwide Interoperability for Microwave Access (WiMAX), High Speed Packet Access (HSPA), and Long Term Evolution (LTE) provide data connectivity of various speed while protocols such as Bluetooth, ZigBee, and WiFi-Direct are useful for connecting various peripherals. A communication standard is uniquely defined by the format of message and set of guidelines to communicate those messages. The specifications, throughputs, mobility, range and power consumption are distinct for each communication standard [2]. For example, the channel bandwidth specifications of different communication standards are given in Table 1.1 where bandwidth varies from 25 kHz to 22 MHz. To support wide range of services, multistandard wireless communication receivers (MWCRs), which allow multiple communication standards to be implemented on a single generic platform, are desired.

In the beginning, e.g. in cellphones supporting GSM as well as CDMA, MWCRs consist of two parallel architectures i.e. one for GSM and other for CDMA, then the reconfigurability is achieved by switching between two architectures. This is an inefficient approach since it will lead to huge area penalties as the number of standards grow. Software defined radio (SDR) has been proposed as a solution to this problem where MWCR supports and provides seamless mobility between multiple communication standards by means of software reconfiguration of the architecture [3-7]. Such SDRs would also support new standards by means of in-field upgrade. Realizing ideal SDR is a challenging task considering the range of existing and imminent communication standards as well as area, speed, power and reconfigurability limitations of resource-constrained battery operated cellphones.

Standards	Channel Bandwidth
Personal Digital Cellular (PDC)	25 kHz
Digital Advanced Mobile Phone System (D-AMPS)	30 kHz
Cordless Telephony 2 (CT2)	100 kHz
Global System for Mobile Communications (GSM)	200 kHz
Personal Handyphone System (PHS)	300 kHz
Bluetooth	1 MHz
Code Division Multiple Access (CDMA)	1.25 MHz
Digital Audio Broadcasting (DAB)	1.712 MHz
Digital Enhanced Cordless Telecommunications (DECT)	1.728 MHz
ZigBee	2 MHz
Universal Mobile Telecommunications System (UMTS)	5 MHz
Wideband – CDMA (W-CDMA)	5 MHz
Digital Video Broadcasting – Terrestrial (DVB-T)	7-8 MHz
Worldwide Interoperability for Microwave Access (WiMAX)	1.25-10 MHz
Long Term Evolution (LTE)	1.25-20 MHz
Wi-Fi	22 MHz

TABLE 1.1. BANDWIDTH PARAMETERS OF DIFFERENT COMMUNICATION STANDARDS

The scarcity of electromagnetic spectrum is another major obstacle that mobile communication will face in near future [8]. The exponentially increasing number of customers and rapid development of various radio access technologies led to huge demand for spectrum which is limited and non-growing. On the other hand, spectrum utilization measurement surveys conducted all over the world found that spectrum utilization is only 10-30% primarily due to static spectrum allocation strategies [8-11]. In static spectrum allocation, each licensed user is allocated a part of the spectrum and other users (licensed or unlicensed) cannot use that spectrum even if it is vacant. The dynamic spectrum access based cognitive radio (CR) has been proposed to improve the spectrum

utilization efficiency [12, 13]. The CR networks allow secondary users (unlicensed users) to use the licensed spectrum when primary users (licensed users), to whom the spectrum is allocated, are inactive. The MWCRs in CRs are functionally identical to those in SDRs except the former need to perform additional tasks of spectrum sensing (searching the huge swaths of spectrum for vacant band(s)), adapting transmission within vacant band without causing interference to adjacent licensed users and quickly releasing the spectrum when licensed user arrives.

In general, the MWCR architecture consists of four serial blocks which are: 1) Analog front-end (AFE), 2) Analog-to-digital Convertor (ADC), 3) Digital front-end (DFE) and 4) Digital signal processing (DSP) algorithms [7, 14], as shown in Fig. 1.1. The wideband radio frequency (RF) input signal received by antenna is passed to the analog front-end which performs analog filtering to prevent aliasing as well as RF to intermediate frequency conversion. An ADC converts wideband analog intermediate frequency signal from the analog front-end to the digital intermediate frequency signal and pass it to the DFE. The DFE selects the desired channel(s) from wideband digitized intermediate frequency signal, shifts frequency bands to the baseband and perform necessary sample rate conversion for further processing by subsequent DSP algorithms.



Fig. 1.1. A multi-standard wireless communication receiver architecture.

The main goal of the MWCR in SDRs and CRs is to shift the ADC as close to antenna as possible which will provide DFE the direct access to wideband digitized input signal so that analog signal processing can be replaced by digital signal processing [3-6]. This is because, to support wide range of services, MWCRs must be able to simultaneously select the desired channel(s) corresponding to distinct communication standards from wideband input signal. However, there are some technological limitations which make the ideal MWCR non-realizable in practice at present [14]. For example, shifting of the ADC close to antenna requires direct digitization of wideband input RF signal of approximately 5 GHz bandwidth. However, existing direct RF-sampling ADCs can sample only up to 2.7 GHz of bandwidth and their power consumption is around 2W - 4.4W which is more than the power budget of an entire MWCR [15-17]. Even if such ADCs are employed, they will impose substantial burden of computations and data rate on subsequent DFE and DSP algorithms [4, 5]. Alternatively, the analog front-end can perform coarse frequency selection task which will provide the DFE an access to wideband input signal of the desired bandwidth instead of entire RF bandwidth. The stringent channel selection task can be efficiently accomplished using digital filters which are known to be highly flexible compared to analog filters [7]. Hence, a feasible MWCR in SDRs and CRs consists of an analog front-end for coarse frequency selection task which can be accomplished using existing analog filters, ADC, the DFE to perform stringent frequency selection task and the DSP algorithms for baseband processing such as signal detection, demodulation etc. Thus, analog front-end and ADC are largely independent of individual communication standards and hardware reconfigurations needed to support distinct communication standards must be done in the DFE. In addition, the performance and computational

complexity of subsequent DSP algorithms significantly depend on the filtering performance of the DFE. Thus, the DFE in SDRs and CRs needs significant amount of enhancement compared to the DFE in existing MWCRs in terms of incorporating the reconfigurability with minimum overhead of area, power, delay etc. and is the focus of the work presented in this thesis.

1.2 Motivation

The DFE is one of the most computationally intensive blocks in the MWCR [7, 18-20]. In emerging MWCRs, the DFE along with the subsequent DSP algorithms are required to perform two main tasks: 1) Channelization: - Extraction of individual channel(s) of uniform or non-uniform bandwidth from the wideband input signal, 2) Spectrum sensing: - Detecting the presence and absence of channel(s) (or vacant frequency band(s)) in the wideband input signal. The DFE is responsible for extracting the desired channel(s) of interest from the wideband digitized intermediate frequency signal. To accomplish this, the DFE needs to perform various tasks such as channel(s) filtering, digital down conversion to bring the channel(s) to DC, sample rate conversion to decimate the signal to the standard-specific symbol rate, pulse shaping etc [7, 18-20]. Out of these, digital filtering is a key task of the DFE since it is the first task in the MWCR which takes into account the type of communication standard and involves a large number of computationally expensive multiplication and addition operations. In addition, the analog front-end does only coarse frequency band selection due to the limited flexibility of analog filters and most of the stringent filtering needs to be accomplished in the DFE. Thus, the DFE has to take care of dynamically changing bandwidths and center frequencies of multiple channels in wideband input signal which precludes the use of fixed-coefficient filter or filter bank architectures optimized for single communication standard. Depending on the number of channels concurrently processed by subsequent DSP algorithms, the DFE employs either variable digital filter(s) (VDFs) or filter bank. For example, VDF is used to extract or sense single channel at a time while filter bank is used to extract or sense multiple channels simultaneously. In general, the area complexity, delay and power consumption of VDF is less than that of filter bank. The factors to be taken into considerations while choosing VDFs or filter banks for the DFE are:

- Reconfigurability: The VDFs and filter banks should be reconfigurable to support distinct frequency specifications corresponding to existing as well as imminent communication standards.
- Reconfiguration delay: The reconfiguration delay is the delay in matching the frequency specifications of the architecture with the desired specifications. The lower the reconfiguration delay, the higher the achievable throughput.
- Linearity: The architecture should preserve the phase of input signal whenever required.
- Efficient hardware implementation: Incorporating reconfigurability incurs penalties in terms of area, power and delay. Hence, along with reconfigurability and

linearity, the architecture should be area and power efficient with minimal group delay to efficiently implement them in resource-constrained MWCRs.

Most of the existing filter and filter bank architectures [7, 20-22] are designed and optimized for supporting single communication standard. In the multi-standard communications scenario, these architectures incorporate reconfigurability either by using parallel structures to switch between communication standards or by updating the filter coefficients stored in memory beforehand, corresponding to different communication standards. This is not an efficient approach due to high penalties in area complexity, power consumption and reconfiguration delay. Lately, little advancement has been made in the design of reconfigurable architectures for multi-standard operations [23-34]. However, these architectures are moderately reconfigurable since they support fewer number of communication standards at the cost of huge penalties in terms of area, power and delay. Moreover, VDFs and filter bank architectures must take into account interstandard channel bandwidth variations in the upcoming standards such as high speed packet access (HSPA) and LTE in addition to intra-standard channel bandwidth variations as shown in Table 1.1. To support multi-standard operation, VDFs that provide variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) response on an unabridged normalized Nyquist band, and reconfigurable filter banks that provide independent and individual control over the bandwidth and the center frequency of subbands are desired. Realizing such architectures with the least area complexity, power consumption, group delay as well as reconfiguration delay is a challenging task. The motivation behind the work presented in this thesis is to address the research issues related to the realization of such VDFs and filter banks taking into account of the area, power and speed constraints of MWCRs.

1.3 Objectives and Contributions

This thesis addresses the design of low complexity, low delay VDFs and reconfigurable filter banks for channelization and spectrum sensing operations in the DFE of MWCRs. The VDF can be used in the DFE of mobile terminal to extract or sense single channel at a time while filter bank can be used in DFE of base stations to extract or sense multiple channels simultaneously. The VDFs and reconfigurable filter banks should be capable of adjusting frequency parameters such as bandwidth and center frequency as per the desired communication standard specifications. Moreover, they should meet the stringent specifications of minimum area, delay and power for efficient hardware implementation. In emerging CRs, higher reconfiguration delay reduces the time available for useful communications which in turn reduces the achievable throughput. Hence, the reconfiguration delay of the VDF and filter bank architectures should be as small as possible. In addition, the usefulness of the proposed architectures for audio signal processing applications like digital hearing aids, loudspeaker equalization etc. will also be addressed in this thesis. The objectives of the work presented in this thesis are:

- 1) To design the VDF that provides :
 - Variable LP, HP, BP and BS responses using fixed-coefficient prototype filter.
 - Overall, reduced (or equivalent) area complexity, group delay, reconfiguration delay and total power consumption compared to the existing VDFs.

2) To design a reconfigurable filter bank which provides :

- Unabridged control over the bandwidth and the center frequency of all subbands.
- Independent and individual control over the bandwidth and the center frequency of subbands.
- Overall, reduced (or equivalent) area complexity, group delay, reconfiguration delay and total power consumption compared to the existing filter banks.

The contributions of this thesis, which are published or under review as mentioned in 'Publication' section on pages vi-vii, are elaborated below:

- 1) A low complexity reconfigurable filter bank based on coefficient decimation method (CDM) and frequency response masking (FRM) technique (CDM-FRM filter bank) is the first contribution in this thesis [C1, J1]. The proposed CDM-FRM filter bank provides coarse control over the subband bandwidth without the need of hardware reimplementation, with low area complexity and power consumption. The applications of the CDM-FRM filter bank for channelization operation which involves extraction of channels of distinct bandwidths from wideband input signal is presented [C1, J1]. The usefulness of the CDM-FRM filter bank for detecting multiple channels present in wideband input signal using an energy detector is elaborated and an algorithm is proposed to accurately find the edge frequencies of all channels [C2].
- 2) The CDM-FRM filter bank provides coarse control over the bandwidth and the center frequency of subbands. In order to improve it further to achieve an unabridged
control over the bandwidth and the center frequency of subbands, the CDM based VDF (CDM-VDF) should be replaced with a VDF that offers an unabridged control over the cut-off frequency on a wide frequency range. A new linear phase VDF using second order modified Farrow fractional delay structure of Lagrange interpolation [35, 99] is proposed and it is called as modified Farrow based VDF (MF-VDF), which is the second contribution in this thesis [C3]. The MF-VDF is the first one where transition bandwidth (TBW) of the VDF is narrower than that of the prototype filter and offers an unabridged control over the cut-off frequency on either side of the cut-off frequency of the prototype filter. However, existing lower order fractional delay structures have flat magnitude and phase/group delay responses up to lower frequencies only [35, 99]. Hence, the MF-VDF, which employs second order fractional delay structure, is suitable for applications where unabridged control over the cut-off frequency on a lower frequency range is desired.

3) The third contribution in this thesis is a low complexity linear phase VDF based on modified second order frequency transformation (MFT-VDF) [C4]. The MFT-VDF, with wide cut-off frequency range, overcomes a major drawback of previous VDFs [36-40] where the cut-off frequency can only be varied within limited range which is approximately 12.5% of the sampling frequency. The MFT-VDF along with the CDM provides variable LP, HP, BP and BS responses from a fixed-coefficient prototype filter which makes them suitable for applications such as serial channelization, serial spectrum sensing etc.

- 4) A reconfigurable fast filter bank (RFFB) is proposed by replacing fixed-coefficient sub-filter in the first stage of FFB with the MFT-VDF, which forms the fourth contribution in this thesis [J2]. The RFFB offers an unabridged control over subband bandwidths and their center frequencies over the desired range without the need of hardware re-implementation. Other than channelization, the RFFB is useful in minimizing the dynamic power consumption of two-stage spectrum sensing by reducing the rate of activation of the second sensing stage [C6]. The RFFB also provides fine control over center frequencies of fixed bandwidth subbands. This unique property makes the RFFB suitable for the channelization or spectrum sensing scenario where the channel bandwidth is fixed but their locations may vary dynamically.
- 5) The fifth contribution in the thesis in is a new design of low complexity and reduced delay VDF [J4] using modified CDM (MCDM) in [29]. The proposed VDF is designed by replacing the prototype filter in the MCDM with the existing VDF that is required to provide an unabridged control only over narrow cut-off frequency range precisely over the second quarter of the normalized frequency. When linear phase spectral transformation (SPA) based VDFs [41-50] is used, the proposed VDF is called as SPA-MCDM VDF and when non-linear phase allpass transformation (APT) based VDFs [51] is used, the proposed VDF is called as APT-MCDM VDF. The SPA-MCDM VDF and APT-MCDM VDF provide variable lowpass, highpass, bandpass and bandstop responses over entire Nyquist band. Though the APT-MCDM VDF is a non-linear phase VDF, it can be useful for energy detection based spectrum

sensing as well as various audio signal processing applications. The SPA-MCDM VDF offers substantial savings in gate count over other linear phase VDFs while APT-MCDM VDF requires lowest gate counts than other linear and non-linear phase VDFs.

- 6) The sixth contribution of this thesis is a linear phase SPA-MCDM filter bank, designed using the SPA-MCDM VDF, and it provides independent and individual control over the bandwidth and the center frequency of subbands [C7]. The gate count complexity and the group delay of the proposed filter bank is lower compared to other filter banks. The usefulness of the SPA-MCDM filter bank for combined channelization and spectrum sensing in CRs is presented.
- 7) The seventh contribution in this thesis is a new architecture for efficient implementation of the APT-VDF by combining first and second order APT with the CDM. It is termed as APT-CDM VDF [C5, J3]. The APT-CDM VDF offered further saving in gate counts over the APT-MCDM VDF and other VDFs. This is achieved by reducing the number of APT branches and eliminating the need for complimentary response. At the end, gate count complexity analysis of the SPA-MCDM filter bank, APT-MCDM filter bank and APT-CDM filter bank is presented. The SPA-MCDM filter bank offers substantial savings in gate count over others and has advantage of linear phase characteristic.

For an easy evaluation, Table 1.2 summarizes the different contributions and the key results obtained in this thesis.

Contributions	Key Results				
Chapter 3 –	1)	Provides coarse control over subband bandwidth.			
CDM-FRM filter	2)	Needs 151%, 49% and 72% less gate counts than PC approach [7],			
bank [J1, C1]		CDM-DFTFB [25] and CDM filter bank [24], respectively.			
Chapter 3 –	1)	Useful for accurate detection of the frequency edges of multiple			
CDM-FRM filter		channels in wideband input signal.			
bank based edges	2)	Simulations show that proposed method is computationally more			
detector [C2]		efficient than other methods for a given error in edge frequency.			
Chapter 4 –	1)	Designed by replacing unit delays in digital filter with second order			
MF-VDF [C3]		modified Farrow structure.			
	2)	The TBW of VDF is narrower than the TBW of its prototype filt			
Chapter 4 –	1)	Designed by modifying 2 nd order frequency transform and provides			
MFT-VDF [C4]		wider cut-off frequency range with LP, HP, BP and BS responses.			
	2)	Offers total gate count reductions of 33% and 41% over the VDF in			
		[48] and [40] respectively.			
Chapter 4 –	1)	Designed by combining MFT-VDF [C4] with the FFB.			
RFFB [J2]	2)	Provides an unabridged control over the bandwidth and the center			
		frequency of subbands over the desired range.			
	3)	Filter banks in [25], [40] and [41] requires 135%, 45% and 78%			
		higher gate counts, respectively when compared with the RFFB.			
Chapter 5 –	1)	Deft integration of MCDM with SPA-VDF (linear phase SPA-			
SPA-MCDM		MCDM VDF) and MCDM with APT-VDF (non-linear phase APT			
VDF [J4] and		MCDM VDF). Both VDFs provide variable LP, HP, BP and BS			
APT-MCDM		responses over entire Nyquist band.			
VDF	2)	Substantial savings in gate count and delay over existing VDFs.			
	3)	APT-MCDM VDF needs lower gate count than SPA-MCDM VDF.			
Chapter 5 –	1)	Provides independent and individual control over subband			
SPA-MCDM		bandwidth as well as their center frequency and has linear phase.			
filter bank [C7]	2)	Substantial savings in gate count and delay over other filter banks.			
Chapter 6 –	1)	Designed by combining CDM-II with reduced 2 nd order APTs.			
APT-CDM VDF	2)	Needs 104% and 67% less gate count than SPA-MCDM VDF and			
[J3, C5]		APT-MCDM VDF, respectively but have non-linear phase.			

TABLE 1.2. SUMMARY OF CONTRIBUTIONS PRESENTED IN THIS THESIS

1.4 Organization

The thesis is organized as follows. Chapter 2 presents the overview of the various functionalities and research challenges in the spectrum sensing and channelization operations in the DFE of MWCRs. The detailed literature review of various uniform and non-uniform filter banks as well as VDFs along with the analysis of their implementation complexities and reconfiguration penalties is done in the latter part of Chapter 2. In Chapter 3, a low complexity reconfigurable CDM-FRM filter bank is presented. The applications of the CDM-FRM filter bank for channelization and accurate detection of frequency band edges of multiple channels present in wideband input signal are explained. A new design of the VDF namely MF-VDF is presented in Chapter 4. The designs of the MFT-VDF and a low complexity RFFB using the MFT-VDF are explained in the latter part of Chapter 4. Two new VDFs, namely SPA-MCDM VDF and APT-MCDM VDF, are presented in Chapter 5. A low complexity and reduced delay reconfigurable linear phase SPA-MCDM filter bank is presented in the latter part of Chapter 5. In chapter 6, a low complexity APT-CDM VDF for energy detection based serial spectrum sensing is presented. Finally, Chapter 7 has conclusions of the work presented in this thesis and possible future directions.

Realizing the digital front-end (DFE) of multi-standard wireless communication receivers (MWCRs) in emerging software defined radios (SDRs) and cognitive radios (CRs) is a challenging task due to the need to support wide range of services using single terminal as well as area, speed, power etc. constraints on the architecture. In MWCRs, analog front-end, owing to limited reconfigurability of an analog filter compared to its digital counterpart, performs only coarse channel selection efficiently. Consequently, the DFE is responsible for the stringent channel selection task which involves the intrastandard channel bandwidth variations, e.g. 1.25 MHz – 20 MHz in the long term evolution (LTE), as well as inter-standard channel bandwidth variations, e.g. 200 kHz in Global System for Mobile Communications (GSM), 1.25 MHz in code division multiple access (CDMA) etc. The emphasis of this chapter is to provide good insight of various functionalities of the DFE. In the latter part of this chapter, a detailed literature review of existing VDFs as well as reconfigurable filter banks for stringent channel(s) selection task in the DFE is presented.

2.1 Multi-standard Wireless Communication Receivers

The main goal of the MWCR architecture in emerging SDRs and CRs is to integrate distinct communication standards, each providing access to different kind of services, on a single generic hardware platform. To realize this goal, most of the analog signal processing must be replaced with the digital signal processing [3-6]. Also, in order to support multiple communication standards, application-specific integrated circuits (ASICs) should be replaced with programmable digital processors or field programmable gate arrays (FPGAs) [5-7]. This allows software implementations of intermediate frequency and baseband functions such as channelization, sensing, demodulation, modulation, equalization etc. as well as re-programmability of the MWCRs to guarantee multi-standard operation. Such MWCRs could also support in-field upgradeability, since new standard could be implemented with a simple over-the-air software update.

A detailed block diagram of the MWCR is shown in Fig. 2.1 [7, 14]. The MWCR in Fig. 2.1 can be divided into three stages based on the range of frequency and they are: 1) Radio frequency (RF) stage, 2) Intermediate frequency stage, and 3) Baseband stage.



Fig. 2.1. A feasible multi-standard wireless communication receiver (MWCR).

The RF stage consists of anti-aliasing filter and low noise amplifier (LNA). The task of anti-aliasing filters is to prevent aliasing while digitizing the signal and the LNA amplifies the signal to the desired level. The intermediate frequency stage consists of a mixer which performs RF to intermediate frequency conversion followed by analog-to-digital converter (ADC) and the DFE. The DFE selects the desired number of channel(s) from wideband digitized intermediate frequency signal, performs additional signal processing operations such as digital down conversion, sample rate conversion etc. The baseband stage consists of digital signal processing (DSP) algorithms to perform various tasks such as detection, de-modulation etc. The part of the MWCR before ADC is also known as analog front-end [7].

In emerging SDRs and CRs, the wideband RF input signal consists of multiple channels of uniform and non-uniform bandwidth corresponding to different communication standards. The combined task of the analog front-end, ADC and DFE is to select the desired number of channels from wideband RF input signal, perform necessary tasks such as signal amplification, image rejection, frequency conversion, sample rate conversion, digital down conversion etc. for further processing by subsequent DSP algorithms [7, 20]. Ideally, the ADC should perform the direct digitization of a wideband RF input signal received by antenna bypassing the analog filtering stage so that the DFE can have direct access to wideband digitized intermediate frequency signal. This would enable the DFE to select channel(s) corresponding to any communication standard depending upon the type of service. However, there are certain technological limitations which make the direct digitization of wideband RF input far from reality at present [7, 14, 15]. These limitations are elaborated below.

- If ADC is moved very close to antenna, the input signal to the ADC will be high dynamic range wideband RF signal. Also, according to the Nyquist theorem, an input signal should be sampled at a rate which is at least twice the RF bandwidth of the signal for perfect reconstruction. Considering the cellular and wireless local area network (WLAN) operating frequency range from 800 MHz to 5.8 GHz, ADCs with at least 12-bit resolution and sampling speed of more than 11 Giga samples per second (GSPS) would be required to satisfy Nyquist criteria [15]. However, for resolutions of 12 bits and 16 bits, the highest speed of operation available for commercial ADCs is 3.6 GSPS and 200 mega samples per second respectively [16, 17]. Therefore, direct digitization of wideband RF signals is beyond the scope of the existing ADCs as its dynamic range and sampling speed are known to progress at a rate much slower than Moore's law [15, 52].
- Other fundamental limitations of ADCs due to its non-ideal nature are low resolution (quantization error), non-linearity, deviation from accurate sample timing intervals (jitter error) and noise, which limit its performance [52, 53].
- 3) Also, even if perfect ADC exists, the computational capacity of the presently available computing platforms is not sufficient to process all the digital information received from ADC due to very high data rate as well as computational load [4, 5].

Thus, a partial band digitization approach is employed by introducing intermediate frequency stage which makes it possible to alleviate ADC sampling rate limitation and

computation load. In this approach, the channel selection task is shared by the analog front-end and the DFE. Taking into account of inter-standard as well as intra-standard channel bandwidth variations and limited flexibility of analog filters, "fixed digitization bandwidth" scheme has been proposed for emerging MWCRs in SDRs and CRs [7]. In this scheme, the analog front-end consists of fixed analog filters which select multiple channels in the desired frequency range (about 800 MHz to 5.8 MHz covering most of the cellular and WLAN standards) while the DFE does stringent channel selection task [7]. Various analog front-end architectures such as super-heterodyne receivers [54], zero-IF receivers [55, 56], low-IF receivers [54, 57], wideband-IF receivers [58] etc. are available in literature which can efficiently perform coarse frequency selection tasks. In addition, the analog front-end also performs signal conditioning tasks such as signal amplification, RF to intermediate frequency conversion, anti-aliasing, image rejection etc. The $\Sigma\Delta$ ADCs are preferred over Nyquist ADCs for digitizing the wideband intermediate frequency signal since the former provides high dynamic range in the channel of interest and offers lower power consumption compared to latter [59, 60]. Various $\Sigma\Delta$ ADC designs have been reported in literature for MWCRs [61-63]. The DFE is responsible for hardware and software reconfigurations needed to support existing as well as imminent communication standards. The higher sampling rate of $\Sigma\Delta$ ADCs leads to the increased computational load on the DFE. Furthermore, the computational complexity, computation time and accuracy of the DSP algorithms depend on the channel selection efficiency of the DFE. Thus, the DFE in SDRs and CRs need a significant amount of enhancement compared to existing DFE in terms of incorporating the reconfigurability with minimum overhead of area, power, delay etc. and is the focus of the research work presented in this thesis.

2.2 Digital Front-end (DFE)

The DFE is one of the most computationally intensive blocks of the MWCR [7]. In emerging SDRs and CRs, the DFE along with the DSP algorithms are required to perform two main tasks: **1) Channelization:** Extraction of individual channel(s) of distinct bandwidth and locations from the wideband input signal, **2) Spectrum sensing:** Detecting the presence and absence of channel(s) (or vacant frequency band(s)) in the wideband input signal [7, 64]. The wideband input signal to the DFE consists of multiple channels, corresponding to multiple communication standards, whose bandwidths and center frequencies may vary dynamically. For example, consider the illustrative frequency responses of wideband input signal labeled as (a), (b), (c) and (d) in Fig. 2.2, where each input consists of multiple channels shown in shaded portion. The task of the DFE is to extract desired channel(s) and frequency band(s) for further baseband processing [5, 16, 17]. For example, in channelization operation, the DFE extracts channel(s) of interest as shown in Fig. 2.2 using input-output pairs, (a)-(i) and (b)-(ii). Similarly, in case of



Fig. 2.2. Illustration of channelization and spectrum sensing tasks in the DFE of MWCRs.

spectrum sensing operation, the DFE extracts desired frequency band(s) as shown in Fig. 2.2 using input (c) – output (iii) pair. In combined spectrum sensing and channelization operation, for instance in CRs, the DFE extracts channel(s) as well as frequency band(s) as shown in Fig. 2.2 using input (d) – output (iv) pair. The DFE outputs are then passed to the respective channelization and detection DSP algorithms.

The DFE is a hardware platform representing the interface between the ADC and subsequent DSP algorithms. The DFE performs various functions such as channel(s) filtering, digital down conversion, sample rate conversion, interferer attenuation etc. [7, 20]. The input signal to the DFE is at the intermediate frequency which precludes the implementation of the DFE using digital signal processors because of their speed constraints. Hence, dedicated hardware, preferably in FPGA due to their flexibility advantage over ASICs, has to be realized for implementing the DFE in emerging SDRs and CRs. The functions of the DFE are elaborated below.

Digital down conversion [7, 19]: - A fundamental part of the many communication system is the digital down conversion. In most of the cases, the channel of interest represents a very small proportion of the wideband input signal bandwidth. The digital down conversion discards the frequency bands that are of no interest allowing more intensive processing to be performed on the bandwidth of interest. In emerging MWCRs where partial band digitization approach is employed, the basic bandwidth selection task is performed in the analog domain by converting the signal of interest to a fixed intermediate frequency. In such cases, by clever choice of intermediate frequency and sampling rate, the digital down conversion can be done using

relatively simple hardware and small look-up table.

- Sampling rate conversion [18]:- In emerging SDRs and CRs, the DFE has to handle the signals at different symbol rates or chip rates corresponding to multiple communication standards. For example, symbol rates for GSM and LTE are 270.82 K symbol per second and 14 K symbol per second, respectively. Since the sampling rate of the ADC is independent of standard-specific symbol rate and DSP algorithms such as demodulation operates at standard-specific symbol or chip rate, the sample rate conversion has been included in the DFE to convert the ADC output at the desired symbol or chip rate. The sample rate conversion factor can be either integer or fractional. In practice, it is divided into integer and fractional part. The sample rate conversion by integer part is performed using many efficient methods available in the literature [65] while the sample rate conversion by fractional part is generally performed using Farrow structure [66].
- Channel(s) filtering: Channel(s) filtering involves the extraction of desired channel(s) of interest from wideband input signal. Depending on the number of channels concurrently processed by subsequent DSP algorithms, the DFE employs either VDFs or reconfigurable filter banks.

In the DFE of emerging SDRs and CRs, channel(s) filtering is a key function since it has to take into account the inter-standard as well as intra-standard channel bandwidth variations and involves large number of multiplication and addition operations. For such scenarios, VDFs that provide variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) responses on an entire normalized frequency scale and reconfigurable filter banks that provide independent and individual control over the bandwidth and the center

frequency of subbands are desired. Realizing such architectures with the least area, delay and power on battery operated resource-constrained mobile handsets is a challenging task.

Besides spectrum sensing and channelization operations in MWCRs, VDFs and reconfigurable filter banks find applications in audio engineering tasks such as loudspeaker equalization and low power digital hearing aids [67-69]. For example, 3subband filter banks are commonly used in digital hearing aids. In emerging wireless body area networks for medical health and public safety applications, multiple sensors attached to human body perform the wireless transmission of data to the handheld device which is implemented on an embedded platform. Since the frequency range and data rate of each sensor are different, input signal to the handheld device consists of multiple channels of distinct bandwidth and location as well as interference signals from adjacent handheld devices. Thus, to receive the desired channel(s) of interest, the VDF and reconfigurable filter bank is desired [70]. Similarly, VDFs and reconfigurable filter banks are also useful for frequency domain adaptive filtering, next generation satellite based communication systems [71] etc. The area, power, speed and reconfigurable delay play an important role in choosing the type of VDFs and reconfigurable filter banks. In the next Section 2.3, the detailed literature review of digital filter banks is presented followed by the review of VDFs in the subsequent Section 2.4.

2.3 Literature Review:- Digital Filter Banks

The filter bank is a bank of filters connected in parallel to a common input such that passband of each filter is adjacent to each other with no overlap or disjointedness. The

filter bank splits the wideband digitized intermediate frequency signal into several subbands at its output. The resolution of filter bank is equal to the number of subbands in filter bank. When all subbands have identical bandwidth, the filter bank is called as uniform filter bank; otherwise called as non-uniform filter bank. Depending on whether the bandwidth and the center frequency of subbands are adjustable or fixed, the filter banks can be classified as reconfigurable filter bank and fixed-filter bank, respectively. A reconfigurable filter bank can be uniform as well as non-uniform but not vice-versa.

The uniform filter bank is commonly used in the DFE supporting single-standard operations. In emerging SDRs and CRs, the DFE must be capable of extracting desired channel(s) corresponding to multiple communication standards. When uniform filter bank is employed for such scenarios, the subband bandwidth should be smaller than or equal to the least channel bandwidth among all the supported communication standards. This is to insure that multiple channels corresponding to different communication standards do not fall in the same subband of filter bank. As a result, the minimum required resolution of the filter bank is very high compared to the number of channels concurrently processed by subsequent DSP algorithms. For example, consider the wideband input signal scenarios shown in Fig. 2.2 where the channel 2 of input (b) has the least bandwidth which is assumed to be equal to $f_s/10$ where f_s is the sampling frequency. Then, the minimum required resolution of uniform filter banks is 10 albeit the number of channels concurrently processed by subsequent DSP algorithms is only 5. Higher the resolution of the filter bank, higher is the area complexity, power consumption and delay which precludes the use of uniform filter bank for SDRs and CRs. The resolution of the filter bank should be equal to the number of channel(s) concurrently processed by the DSP

block. To achieve this, a reconfigurable filter bank which provides individual and independent control over the subband bandwidth as well as their center frequencies is desired. A detailed literature review of various filter bank architectures along with their reconfigurability penalties and complexity aspects is presented here.

2.3.1 Filter Bank using Per-Channel (PC) Approach

The per-channel (PC) approach is a straight forward method where a distinct filter is used for each subband as shown in Fig. 2.3 [7]. Here, $H_0(z)$ is a lowpass filter, $H_{N-I}(z)$ is a highpass filter and remaining filters ($H_1(z)$ to $H_{N-2}(z)$) are bandpass filters. The PC approach provides a great deal of flexibility in the design of non-uniform fixed-filter banks where subband bandwidths may not be same but fixed and known in advance.

The finite impulse response (FIR) filter of length N_{FIR} (number of filter coefficients) requires N_{FIR} multiplications and (N_{FIR} -1) additions where N_{FIR} is given by [72],



Fig. 2.3. Filter Bank using per-channel (PC) approach [7].

$$N_{FIR} = \frac{2}{3} \cdot \log_{10} \left(\frac{1}{10\delta_p \delta_s} \right) \cdot \frac{f_s}{\Delta f}$$
(2.1)

where δ_p and δ_s are the passband and stopband ripples respectively, f_s is the sampling rate and Δf is the transition bandwidth (TBW). Then, the PC approach based filter bank with N subbands requires ($N*N_{FIR}$) multiplications and ($N*(N_{FIR} - 1)$) additions which indicate that the complexity of the filter bank increases linearly with the number of subbands. Also, in case of reconfigurable filter bank designed using the PC approach, reconfiguration delay, which is the time required to reconfigure the filter bank from current frequency specifications to the desired frequency specifications, is very high. This is because, filter coefficients need to be updated every time the desired bandwidth and the center frequency of subband changes. For example, when the bandwidth of channels present in the input signal shown in Fig. 2.2 changes, coefficients of corresponding filters need to be updated. Other than high reconfiguration delay, PC approach also requires large size memories to store filter coefficients. Hence, the PC approach is not suitable for the design of low complexity reconfigurable filter banks for MWCRs where independent and individual control over the bandwidth and center frequencies of subbands are desired.

2.3.2 Modulated Filter Bank Approach

An alternative to the PC approach is the modulation approach where all the filters are derived by modulating (i.e. frequency shifting) a lowpass prototype filter [7, 20]. Since there is no need of implementing separate filter for each subband, modulated filter banks are computationally efficient (lower hardware cost and multiplication rate) than the PC approach when the resolution of filter bank is higher (≥ 2).

When discrete Fourier transform (DFT) based modulation is used, the filter bank is called as DFT filter bank (DFTFB) [7, 20]. The *N*-subband DFTFB, shown in Fig. 2.4, is a classic example of modulated filter bank approach. It consists of polyphase implementation of a lowpass prototype filter of order N_{FIR} followed by *N*-point inverse-DFT operation. The total number of multiplications and additions in the DFTFB are [N_{FIR} + $N*\log_2(N)$] and [$(N_{FIR}-1)+ 2N*\log_2(N)$] which are significantly less than that of the PC approach for a given N_{FIR} and larger *N*. Due to the down sampling operation by factor *N*, the prototype filter in the DFTFB operates at lower sampling rate i.e. 1/*N* times the input sampling rate which leads to substantial savings in dynamic power consumption [7].

Since the DFTFB is a modulated filter bank, the bandwidth of all subbands are identical and equal to the passband width of the prototype filter while the center frequencies are uniformly distributed. One way to vary the subband bandwidth is to update the filter coefficients of the prototype filter which requires large size memories and incurs large reconfiguration delay. Also, when the passband of the prototype filter is



Fig. 2.4. Discrete Fourier transform filter bank (DFTFB) [7, 20].

changed, the bandwidth of all subbands changes simultaneously which means that the independent control over each subband bandwidth is not possible in the DFTFB. Furthermore, the center frequencies of subbands are fixed. One possible way to vary center frequencies of subbands is by re-formulating the polyphase branches of the prototype filter, resolution of the inverse-DFT and down sampling factor which is a tedious and computationally intensive task. For example, the reconfiguration from 16-subband filter bank to 32-subband filter bank involves increasing the number of polyphase branches from 16 to 32, changing the down sampling factor from 16 to 32 and replacing the 16-point DFT with 32-point DFT. Despite that, only discrete control over center frequencies is possible.

The DFTFB, shown in the Fig. 2.4, is termed as an analysis filter bank because it analyses the input signal by splitting it into several subbands. In [21], an efficient filter bank called modulated perfect-reconstruction filter bank (MPRFB) is proposed which consists of synthesis filter bank followed by an analysis filter bank as shown in Fig. 2.5. An analysis section consists of a higher order narrowband prototype filter with sharp TBW (i.e. higher N_{FIR}) and a relatively large DFT (i.e. higher N) to generate many small bandwidth subbands. Then, the appropriate number of subbands are combined using synthesis section depending on the desired subband bandwidth and the center frequency. In this way, fixed channel stacking and uniform subband bandwidth limitations of the DFTFB are overcome in the MPRFB [21]. However, the inability to provide subband bandwidths which are fractional multiples of each other precludes the use of the MPRFB for channelization involving communication standards whose channel bandwidths are not related by integer factors. Also, the complexity of the MPRFB, consisting of a polyphase



Fig. 2.5. Modulated perfect-reconstruction filter bank (MPRFB) [21].

prototype filter followed by inverse-DFT and DFT sections, is almost double than that of the DFTFB [21].

In [24], coefficient decimation methods (CDM), CDM-I and CDM-II, are proposed for the design of low complexity reconfigurable FIR filters and filter banks. The CDM-II provides coarse control over the cut-off frequency of an FIR filter. In CDM-II operation by an integer decimation factor D_{II} , every D_{II} th coefficients of an FIR filter are grouped together discarding in between coefficients to obtain a decimated version of the original frequency response with the cut-off frequency and the TBW, D_{II} times that of the prototype filter [24]. Fig. 2.6 shows the variable lowpass cut-off frequency responses obtained using the CDM-II from the fixed-coefficient prototype filter for different values of D_{II} . Using CDM-II, a reconfigurable DFTFB (CDM-DFTFB) is proposed in [25] which allows on-the-fly coarse control over the subband bandwidth. In the CDM-DFTFB, the CDM-II is incorporated into the polyphase fixed-coefficient lowpass prototype filter



Fig. 2.6. Variable cut-off frequency responses obtained using the CDM-II.

of the DFTFB as shown in Fig. 2.7. By changing D_{II} , the passband of lowpass filter and hence the subband bandwidth of the CDM-DFTFB can be changed. Since D_{II} is limited to discrete integer values, the CDM-DFTFB can provide only coarse control over the subband bandwidth. Furthermore, the CDM has inherent disadvantage of deterioration in stopband attenuation as well as the TBW for higher decimation factors and hence the prototype filter needs to be over-designed [24]. As a result, the length of the prototype filter in the CDM-DFTFB is larger than that in the DFTFB.

In order to overcome the limitation of fixed center frequency subbands of the DFTFB and its modifications, a filter bank for which the response of the prototype filter can be modulated to any center frequency is needed. This can be done using the Goertzel algorithm [73] as a substitute to the DFT operation. In Goertzel filter bank (GFB) [7], a modified Goertzel algorithm is used which shifts the lowpass frequency response of the prototype filter to any desired center frequency. However, like DFTFB, the GFB cannot provide variable bandwidth subbands. Also, the GFB requires infinite impulse response (IIR) filter for the implementation of Goertzel algorithm which makes it unsuitable for several communication applications due to non-linear phase property of IIR filters [7].



Fig. 2.7. Coefficient decimation method based DFT filter bank (CDM-DFTFB) [25].

Overall, the modulated filter banks [7, 20, 21, 25] are easy to design and provide computationally efficient alternative to the PC approach when the number of subbands i.e. *N* is large. The modulated filter banks are superlative for applications such as channelization involving single communication standard where the channel bandwidth is fixed and equal. However, modulated filter bank approach fails to provide unabridged, independent and individual control over the bandwidth and the center frequency of subband. Hence, there is a need to evolve an alternative to modulated filter banks for emerging SDRs and CRs where multiple communication standards will coexist simultaneously.

2.3.3 Fast Filter Banks

When linear phase FIR filter is interpolated by a factor of N (i.e. each delay of an FIR filter is replaced by N delays), a 2N-band response is obtained. The bandwidth and the TBW of each subband are 1/N times that of the FIR filter. These subbands can be

extracted by appropriately designed interpolated masking filters. Based on this scheme, a fast filter bank (FFB) is proposed in [22] as a low complexity alternative to the DFTFB.

The *N*-subband FFB using *k*-stage tree-structured architecture is shown in Fig. 2.8 [22] where N = 16 and k = 4 (=log₂N). The FFB consists of sub-filters, $H_{ij}(z)$, where $0 \le i \le (k-1)$ and $0 \le j \le (2^i-1)$, out of which *k* sub-filters $H_{i0}(z)$, where $0 \le i \le (k-1)$, are the prototype filters. The prototype filters are even order lowpass filters with symmetrical impulse response. The remaining sub-filters, $H_{ij}(z)$, where j > 0 are modulated versions of the prototype filter [22] as shown in Fig. 2.8. All the sub-filters in the k^{th} stage are interpolated by a factor $M/2^{(k-1)}$ and each sub-filter provide original and complementary responses. In FFB, only *k* filters that have wide TBWs (lower order) are designed as prototype filters and the rest of the filters $H_{ij}(z)$, where j > 0, are realized by frequency shifting the *k* prototype filters to realize a *N*-subband FFB. The TBW and hence the order sub-filters that are located at the front-end of the tree structure is higher compared to its





successor [22]. The FFB is preferred over the DFTFB when sharp TBW response is desired since its complexity does not increase significantly with decrease in TBW compared to the linear increase in complexity for the DFTFB. However, the FFB has the same limitations as that of the DFTFB, i.e. uniform bandwidth subbands with fixed center frequencies. Also, the group delay of the FFB is larger than that of the DFTFB.

In FFB, the bandwidth and the center frequency of subbands are determined by the frequency specifications of the sub-filter, $H_{00}(z)$. If the interpolation factor of $H_{00}(z)$ can be changed with that of corresponding masking filter stages of the FFB, the resolution of filter bank can be changed without the need of hardware re-implementation. Using this approach, a multi-resolution uniform FFB is proposed in [26] which overcomes the fixed resolution constraint of the DFTFB and the FFB without any additional multiplication complexity. From *N*-subband uniform FFB, frequency responses corresponding to (*N/L*)-subband uniform FFBs, where L = 2, 4, 8 ... *N*/2, can be obtained [26]. Since the interpolation factor is limited to positive integer values, only limited and coarse control over center frequencies is possible using this multi-resolution uniform FFB. A non-uniform fixed-FFB, which consists of the FFB followed by summing and shaping sub-filters stage, is proposed in [32]. However, FFB [32] is not reconfigurable since it cannot provide on-the-fly control over the bandwidth and the center frequency of subbands.

2.3.4 Coefficient Decimation Method (CDM) Based Filter Banks

The CDM-I as well as CDM-II are widely used in the design of low complexity reconfigurable filter banks for MWCRs [24-30]. In the CDM based reconfigurable filter

bank proposed in [24], an *N*-tap lowpass FIR filter, H(z), termed as 'prototype filter' is designed. Subsequently, every D_I^{th} coefficient of the prototype filter is retained and all other coefficients are replaced with zero values. The frequency response of the resulting decimated filter, $H_{D_I}(z)$, will have replicas of the passband of the prototype filter at integer multiples of $\left(\frac{2\pi}{D_I}\right)$. This operation is termed as coefficient decimation method-I (CDM-I) [24]. The transfer function of decimated filter, $H_{D_I}(z)$, is given by

$$H_{D_{I}}(z) = \frac{1}{D_{I}} \sum_{k=0}^{D_{I}-1} H\left(e^{j\left(\omega - \left(\frac{2\pi k}{D_{I}}\right)\right)}\right)$$
(2.2)

Fig. 2.9 (b) and Fig. 2.9 (c) show the frequency responses obtained using the CDM-I from the prototype filter in Fig. 2.9 (a) for D_I of 2 and 4 respectively. Note that the bandwidth and the TBW of subbands are same as that of the prototype filter. Then, to change the subband bandwidth, the CDM-II is used. In CDM-II, every D_{II} th coefficient of the prototype filter is grouped together discarding in between coefficients to obtain a decimated frequency response in comparison to the original frequency response (i.e. a passband width of D_{II} times the original passband width) as shown in Fig. 2.9. The desired subbands can be extracted from the identical bandwidth spectrum replicas of the decimated prototype filter using one or more of the following operations – subtraction, frequency masking or complementary filtering [24]. Thus, using CDM-I and CDM-II, subbands of bandwidths D_{II} times the passband width of the prototype filter located at integer multiples of $\left(\frac{2\pi}{D_i}\right)$ can be extracted.



Fig. 2.9. (a) Frequency response of the prototype filter, (b) Frequency responses obtained using the CDM-I from prototype filter in (a) for $D_I = 2$ and $D_{II} = 1, 2, 3$, (c) Frequency responses obtained using CDM-I from prototype filter in (a) for $D_I = 4$ and $D_{II} = 1, 2, 3$.

In [27], the CDM-II is incorporated in a tree-structured filter bank and by varying D_{II} , the subband bandwidth can be changed. Since only delay line is changed, a fixed-coefficient implementation is feasible for the prototype filter, which leads to a low complexity filter bank. However, independent and individual control over the bandwidth and the center frequency of subbands cannot be achieved using both the filter banks.

A progressive decimation filter bank [28], shown in Fig. 2.10, provides independent and individual control over the bandwidth and the center frequency of subbands. In Fig. 2.10, multiple lowpass responses are obtained from fixed-coefficient lowpass prototype filter using the CDM-II. For example, the cut-off frequency of output $y_{iD_{II}}(z)$ is $f_{ciD_{II}} = D_{II} \cdot f_c$ where f_c is the cut-off frequency of the prototype filter. By subtracting the output with higher $f_{ciD_{II}}$ from the one with lower $f_{ciD_{II}}$, a bandpass response with desired bandwidth and center frequency is obtained. Recently, the modified CDM (MCDM) is proposed in [29] where the signs of alternate decimated coefficients are changed which results in fewer number of decimation factors compared to the CDM. For example, using the MCDM-II with decimation factor of D_{II} , a lowpass response with $f_{ciD_{II}} = D_{II} \cdot (1 - f_c)$ is obtained in addition to $f_{ciD_{II}} = D_{II} \cdot f_c$ obtained using the CDM-II. The progressive decimation filter bank designed using the MCDM-II [30] provides huge complexity saving compared to that in [28].

The CDM as well as the MCDM has inherent disadvantages of deterioration in



Fig. 2.10. Progressive decimation filter bank [28].

stopband attenuation and the TBW for larger decimation factors which means that the prototype filter needs to be over-designed. The other disadvantages of reconfigurable filter banks designed using the CDM and the MCDM are inability to provide an unabridged control over subband bandwidth and their center frequencies due to integer decimation factors and significant increase in complexity for sharp TBW specifications. For an easy understanding, comparison between different filter banks discussed above is summarized in Table 2.1

Filter bank	Gate Count	Group Delay	RAM/ ROM	Reconf. Delay	Control over subband's		
					Center	bandwidth	
					Frequency	Independent	Unabridged
РС	Very	Low	Yes	Very	Unabridged	Yes	Yes
approach [7]	high	Low	105	high			
DFTFB	Low	Low	No	high	No	No	No
[7, 20]	2011						
MPRFB [21]	High	Low	No	High	No	No	Coarse
CDM-	Low	Low	No	Low	No	No	Coarse
DFTFB [25]					** 1 • 1 1		
GFB [7]	Low	Low	No	Hıgh	Unabridged	No	No
FFB [22]	Very	Very	No	High	No	No	No
	Low	high					
Multi-	Very	Very high	No	Low	No	No	Coarse
resolution	Low						
FFB [26]							
CDM filter	Low	Low Low	No	Low	Coarse	No	Coarse
bank [24]							
Progressive							
decimated	High	High	No	Low	Coarse	Yes	Coarse
filter bank	0	0					
[28, 30]							

TABLE 2.1. COMPARIOSN OF DIFFERENT LINEAR PHASE FILTER BANKS

2.4 Variable Digital Filters (VDFs)

Most of the filter bank architectures discussed in the Section 2.3 incorporate reconfigurability either by using distinct structures or storing the filter coefficients corresponding to all desired specifications in memory. This is not an efficient approach from the perspective of resource utilization and hardware complexity, especially when the architecture must be area and power efficient. Though the CDM and the FRM based filter bank architectures [24-28, 30] support the set of communication standards, they provide moderate reconfigurability since the number of communication standards are limited and must be known a priori. Ideally, the filter bank is expected to provide complete reconfigurability i.e. the filter bank architecture, in addition to switching among known set of communication standards, must support imminent communication standards without the need of hardware re-implementation or the coefficient updates.

One approach to design such reconfigurable filter bank would be to replace fixedcoefficient prototype filter in the DFTFB and the FFB with the VDF. The VDF is a digital filter whose frequency specifications such as cut-off frequency can be controlled through a small number of parameters with minimum overhead on complexity [34]. By varying the cut-off frequency of the VDF, unabridged control over the subband bandwidth can be achieved. Similarly, in the case of progressive decimation filter bank [28, 30], if the CDM-VDF is replaced with another VDF which provides an unabridged control over the cut-off frequency on a wide frequency range, a reconfigurable filter bank with independent and individual control over the bandwidth and the center frequency of

subbands can be designed. For both these approaches, a lowpass VDF with an unabridged control over the cut-off frequency over entire Nyquist band is desired.

In scenarios where the number of channel(s) concurrently processed by subsequent DSP algorithms is fewer, the DFE employs the VDF instead of filter bank. For example, in serial channelization, the DSP algorithms handles single channel at a time while in combined spectrum sensing and channelization operation, the DSP algorithms concurrently handles at least two channels. To support multiple communication standards, the VDF that provides variable LP, HP, BP and BS responses from fixed-coefficient prototype filter over the entire Nyquist band is desired. Moreover, the VDF should be hardware-efficient in terms of area, speed and power consumption. Realizing such low complexity VDFs is a challenging task. A literature review on various VDF designs is presented here.

2.4.1 Programmable Filters

Programmable filters are memory based filters in which desired frequency responses are obtained by updating the coefficients of the prototype filter previously stored in memory. The various designs of programmable filters are studied, analyzed and proposed in [74-79]. In programmable filters, size of the memory depends on the discretization granularity of the cut-off frequency range as well as the prototype filter order. For the MWCR applications where filter order is relatively large due to stringent communication standard specifications and the requirement of an unabridged control over the cut-off frequency, the memory requirements are huge and updating routine becomes progressively complex and time consuming. Hence, programmable filters are preferred

only when filter order is small and the cut-off frequency changes infrequently within limited identified values.

2.4.2 Transformation Based Variable Digital Filters

The transformation based approach is the first attempt to design VDF whose cut-off frequency can be controlled using fewer parameters without the need of updating filter coefficients. In the transformation based approach [36-40, 51, 67-69], the prototype filter with certain frequency specifications is designed and then suitable transformation is applied to obtain final VDF. Depending upon the type of transformation such as allpass transformation (APT) [51, 67-69] and frequency transformation of first or second order [36-40], there are two types of VDFs:-

a) Allpass Transformation Based Variable Digital Filters (APT-VDFs)

The first APT-VDF is proposed in [51] and further extended in [67-69]. The APT-VDFs are obtained by replacing each unit delay of a digital filter with an allpass structure of an appropriate order. The frequency response of the APT-VDF is identical to the frequency response of the prototype filter on a distorted frequency scale. By changing the coefficients of an APT, the distortion of the frequency axis is varied, and the cut-off frequency of the APT-VDF can be controlled on-the-fly. The APT-VDFs are also known as warped filters since the output response is a warped version of input response.

The first and second order APTs are commonly used for the design of VDFs. Consider N^{th} order FIR filter (also called as prototype filter) with transfer function H(z) and the cut-

off frequency, f_{c0} . Let G(z) be the APT-VDF, with the cut-off frequency f_{ca} , obtained by replacing every delay of H(z) with the first order allpass structure, A(z) [51] i.e.

$$G(z) = H(A(z)) \tag{2.3}$$

where

$$A(z) = \left(\frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}}\right) \qquad |\alpha| < 1$$

The implementation of G(z) and A(z) are shown in Fig. 2.11 [51] and Fig. 2.12 [80] respectively. The G(z) consists of N^{th} order prototype filter with the cut-off frequency, f_{c0} , and coefficients h_0 , h_1 ,..., h_N in the transposed direct form. Each unit delay of G(z) is replaced with A(z) as shown in Fig. 2.11 [51]. By changing α , the cut-off frequency, $f_{c\alpha}$, of



Fig. 2.11. Allpass transformation based variable digital filter (APT-VDF), G(z) [51].



Fig. 2.12. First order allpass transformation, A(z) [80].

G(z) can be changed. For $-1 < \alpha < 0$, the transformation is backward which means $f_{c\alpha} < f_{c0}$ and for $0 < \alpha < 1$, the effect is the reverse i.e. forward transformation which means $f_{c\alpha} > f_{c0}$ [51]. When $\alpha = 0$, the APT-VDF is reduced to an FIR filter (i.e. H(z)) with unit delay and the cut-off frequency, f_{c0} . Depending upon the type of prototype filter, variable LP, HP, BP and BS responses can be obtained at the output.

In case of variable BP and BS responses, two variable parameters, the center frequency and the bandwidth, depend on a single controlling parameter, α . Hence, the APT-VDF using A(z) fails to provide variable bandwidth responses for a given center frequency since each value of α corresponds to distinct center frequency. Also, whenever the type of the response needs to be changed, the prototype filter coefficients will need to be updated, which incurs huge amount of memory read and write operations as well as large reconfiguration delay. To overcome these drawbacks, second order APT, B(z), is used [51, 69] which provides LP to BP and BS transformation, and it is given by,

$$B(z) = \left[\frac{-\left(\frac{\beta - 1}{\beta + 1}\right) + \left(\frac{2\alpha\beta}{\beta + 1}\right)z^{-1} - z^{-2}}{1 - \left(\frac{2\alpha\beta}{\beta + 1}\right)z^{-1} + \left(\frac{\beta - 1}{\beta + 1}\right)z^{-2}} \right]$$
(2.4)

where

$$\alpha = \frac{\cos\left(\frac{\omega_{c2} + \omega_{c1}}{2}\right)}{\cos\left(\frac{\omega_{c2} - \omega_{c1}}{2}\right)} \quad \text{and} \quad \beta = \cot\left(\frac{\omega_{c2} - \omega_{c1}}{2}\right) \tan\left(\frac{\omega_{c}}{2}\right)$$

Here ω_{c1} (= $2\pi f_{c1}$) and ω_{c2} (= $2\pi f_{c2}$) are upper and lower cut-off frequencies respectively. APT-VDFs are widely used for various applications such as energy

detection based spectrum sensing, linear prediction, echo cancellation, loudspeaker equalization, spectrally modifying an audio signal [51, 67-69] etc. However, APT-VDFs require separate first and second order APT to obtain variable LP, HP, BP and BS responses which make the overall filter highly complex and power inefficient [69]. Also, due to the APT, APT-VDFs are not considered as linear phase filters even if the prototype filter has linear phase [51, 80] and hence APT-VDFs are not employed extensively in communication applications that require linear phase characteristics.

b) Frequency Transformation Based Variable Digital Filters

In [36], frequency transformation based linear phase VDF is proposed and further extended in [37-40]. Consider a causal linear phase FIR filter, H(z), of order 2N with symmetric coefficients which is referred as the prototype filter. This prototype filter is implemented in Taylor form by expressing the transfer function as

$$H(z) = \sum_{n=0}^{N} a_n z^{-N} \left[\frac{z + z^{-1}}{2} \right]^n = \sum_{n=0}^{N} a_n z^{-N+n} \left[\frac{1 + z^{-2}}{2} \right]^n$$
(2.5)

where the coefficients a_n are related to the impulse response coefficients h_n of the prototype filter, through Chebyshev polynomials [36]. The P^{th} order frequency transformation is performed using the substitution

$$\frac{z+z^{-1}}{2} = \sum_{k=0}^{P} A_k \left(\frac{Z+Z^{-1}}{2}\right)^k$$
(2.6)

The transformed filter, $H_p(Z)$, obtained by substituting Eq. (2.6) into Eq. (2.5), is given by,

$$H_P(Z) = \sum_{n=0}^{N} a_n Z^{-P(N-n)} \underbrace{\left[\sum_{k=0}^{P} A_k Z^{(k-P)} \left(\frac{1+Z^{-2}}{2}\right)^k\right]}_{D_P(Z)}^n$$
(2.7)

The implementations of $H_p(Z)$ and $D_P(Z)$ are shown in Fig. 2.13 and Fig. 2.14 [36], respectively. The prototype filter coefficients a_0 , $a_1...a_n$ are fixed and hence can be hardwired. The frequency characteristics of $H_p(z)$ are varied by changing the coefficients A_0 , A_1 ,... A_P of $D_P(Z)$. In case of first order transformation i.e. P = 1, Eq. (2.7) and Eq. (2.6) reduce to

$$H_{1}(Z) = \sum_{n=0}^{N} a_{n} Z^{-(N-n)} \left[A_{0} Z^{-1} + A_{1} \left(\frac{1+Z^{-2}}{2} \right) \right]^{n}$$
(2.8)
$$\mathbf{x}(z) \longrightarrow D(Z) \longrightarrow D($$

Fig. 2.13. P^{th} order frequency transformation based VDF, $H_P(Z)$ [36].



Fig. 2.14. P^{th} order frequency transformation, $D_P(Z)$ [36].

$$\cos\omega = A_0 + A_1 \cos\Omega \tag{2.9}$$

where

$$\cos \omega = \frac{(z+z^{-1})}{2} | z = e^{j\omega}$$
 and $\cos \Omega = \frac{(Z+Z^{-1})}{2} | Z = e^{j\Omega}$

Here ω and Ω corresponds to the cut-off frequencies of the prototype filter and the transformed filter respectively. It is showed that when $A_0 + A_1 = 1$ and $0 \le A_0 < 1$, the transformation is forward i.e. Ω is always greater than or equal to ω [36, 37]. Similarly, when $A_1 = 1 + A_0$ and $-1 \le A_0 < 0$, the transformation is backward i.e. Ω is always smaller than or equal to ω [36, 37]. Hence, the frequency control on either side of prototype filter is not possible using first order frequency transformation. Also the cut-off slope i.e. the TBW of the transformed filter deteriorates compared to that of the prototype filter. To overcome these drawbacks, second order frequency transformation based VDF, $H_2(Z)$, is proposed in [40] and it is given by

$$H_2(Z) = \sum_{n=0}^{N} a_n Z^{-2(N-n)} \underbrace{\left[\sum_{k=0}^{2} A_k Z^{(k-2)} \left(\frac{1+Z^{-2}}{2}\right)^k\right]}_{D_2(Z)}^n$$
(2.10)

Corresponding second order transformation is given by,

$$\cos \omega = A_0 + A_1 \cos \Omega + A_2 \cos^2 \Omega \tag{2.11}$$

From Eq. (2.11), the cut-off frequency and the TBW of $H_2(Z)$, are given as [40]

$$\Omega = \cos^{-1}\left\{\left\{-A_1 \pm \left[A_1^2 - 4A_2(A_0 - \cos\omega)\right]^{1/2}\right\}/2A_2\right\}$$
(2.12)

$$TBW = (A_1 \sin \Omega + A_2 \sin 2\Omega) / \sin \omega$$
(2.13)

if the following constraints are met [40]:

$$A_0 + A_1 + A_2 = 1, \qquad 0 \le A_1 \le 1, \qquad A_2 \le \frac{A_1}{2}$$

 $A_2(1 - A_1 - A_2 - \cos \omega_c) \ge 0$ (2.14)

In [40], $A_1 = 1$ and $A_0 = A_2$, in order to reduce the number of multipliers and number of variable parameters. However, by restricting A_1 to unity, the range over which the cut-off frequency, Ω , can be varied is limited to approximately 12.5% of the sampling frequency through empirical observations. Also, the prototype filter needs to be updated whenever the type of response changes [36-40].

In general, all the transformation based VDFs [36-40, 51, 67-69] need to update filter coefficients or need distinct transformations to obtain variable LP, HP, BP and BS responses. Also, the TBW of the responses is not fixed and overall order of the transformed filter is higher than that of the prototype filter.

2.4.3 Spectral Parameter Approximation Based VDFs

The transformation techniques [36-40, 51, 67-69] discussed in Section 2.4.2 are applicable to VDFs with variable cut-off frequencies only while spectral parameter

Chapter 2 – Literature Review: - Variable digital filters and reconfigurable filter banks

approximation (SPA) techniques are applicable to VDFs with variable cut-off frequencies or fractional delays or both [41-50].

The block diagram of the SPA-VDF is shown in Fig. 2.15 where $H_i(z)$, $0 \le i \le L$, are sub-filters and α is the controlling parameter which controls either the cut-off frequency or the fractional delay of the SPA-VDF. This approach is known as spectral parameter approximation since the VDF is a weighted combination of fixed-coefficient FIR subfilters and the weights are directly proportional to the spectral parameter [41-50]. The SPA technique is initially proposed to design VDFs with tunable fractional delays and they employed Farrow structure [81] which provides online tuning for the phase delay of the input signal. Here, first (*L*+1) sub-filters $H_i(z)$, $0 \le i \le L$, are designed offline and optimized for a given range of delay. Then, their impulse responses are interpolated by L^{th} order polynomial using α as the variable [42]. This technique is then extended to the design of the VDF with tunable frequency specifications such as cut-off frequency. In case of the SPA-VDF with tunable cut-off frequency [41-50], $H_i(z)$, $0 \le i \le L$, are fixedcoefficient sub-filters with distinct cut-off frequencies and α is the controlling parameter which decides the cut-off frequency of the SPA-VDF. The transfer function of the SPA-



Fig. 2.15. Spectral parameter approximation based VDF (SPA-VDF) with FIR sub-

filters in transposed direct form.

VDF, $H(z, \alpha)$, shown in Fig. 2.15, can be expressed as [41]

$$H(z,\alpha) = \sum_{k=0}^{L} H_k(z) \cdot \alpha^k$$
(2.15)

where α is the tunable parameter. The transfer function of the $k^{th} N^{th}$ order fixedcoefficient linear phase sub-filter, $H_k(z)$, is given by,

$$H_k(z) = \sum_{n=0}^{N} h_k(n) z^{-n}$$
(2.16)

where $h_k(n)$ is symmetrical or non-symmetrical impulse response of $H_k(z)$. Combining Eq. (2.15) and Eq. (2.16), we get

$$H(z,\alpha) = \sum_{k=0}^{L} \sum_{n=0}^{N} h_k(n) z^{-n} \cdot \alpha^k$$
(2.17)

Different number of approaches has been proposed to determine filter coefficients, $h_k(n)$, so that the frequency response of $H(z, \alpha)$ will approximate the desired response as a function of α . In the first approach, the least squares or Parks-McClellan filter is designed for each tuning points and then polynomial curve fitting is done to obtain $h_k(n)$ where $0 \le k \le L$ and $0 \le n \le N$ [41, 42]. Subsequently, many optimization techniques such as minimax approximation, linear programming, least square, weighted least square and constrained least square are proposed [43-50]. The SPA-VDFs has advantages such as

fixed TBW, lower overall group delay, few adjustable parameters resulting in a simple updating routine, fast tuning time and high accuracy compared to frequency transformation VDFs [36-40, 51, 67-69]. From Eq. (2.17), it can be observed that additional output responses can be easily obtained from a fixed-coefficient prototype filter. Each extra output requires only *L* extra multiplications which are significantly smaller than the transformation based VDFs [36-40, 51, 67-69]. However, the complexity of the SPA-VDF is very high, almost 8-10 times that of frequency transformation based VDFs [36-40, 51, 67-69]. Also, coefficient values of sub-filters increase exponentially with their order which may impose constraints when fixed-point implementation is needed. Since the order of sub-filters depends on the cut-off frequency range, SPA-VDFs are preferred for application which requires narrower cut-off frequency range. Most of the current research on SPA-VDFs is focused on algorithms for optimizing sub-filter coefficients thereby improving the mean square error and reducing offline processing time. There is hardly any work on low complexity architectures for SPA-VDFs when a wide cut-off frequency range is desired.

2.4.4 Frequency Response Masking Based VDFs

The FRM technique is first proposed in [82] with the aim to design low complexity sharp TBW FIR filters and further extended in [31, 33, 83-86]. The block diagram of the FRM technique and corresponding frequency responses at various stages are shown in Fig. 2.16 and 2.17 respectively. The FRM filter design procedure starts with the design of a prototype lowpass filter $H_a(z)$ of odd length *N*. The corresponding complementary filter, Chapter 2 – Literature Review: - Variable digital filters and reconfigurable filter banks

 $H_c(z)$, is obtained by subtracting the output of the prototype filter from the delayed version of the input and is given by [82],

$$H_c(z) = z^{-\frac{(N-1)}{2}} - H_a(z)$$
(2.18)

Both the filters are interpolated by M to get multiband responses $H_a(z^M)$ and $H_c(z^M)$ as shown in Fig. 2.17 (b). In FRM, undesired subbands in $H_a(z^M)$ and $H_c(z^M)$ are masked



Fig. 2.16. Sharp TBW digital filter based on the FRM technique [82].



Fig. 2.17. Frequency response illustration of the FRM technique.

using two cascaded lower order masking filters, $H_{ma}(z)$ and $H_{mc}(z)$, respectively as shown in Fig. 2.17 (c). Hence the name frequency response masking. The sharp TBW lowpass response obtained using the FRM is shown in Fig. 2.17 (d) and corresponding transfer function of the overall filter, H(z), is given by,

$$H(z) = H_a(z^M)H_{ma}(z) + \left[z^{-M\frac{(N-1)}{2}} - H_a(z)\right]H_{mc}(z)$$
(2.19)

By suitable selection of the passband and stopband edges of the prototype filter and the masking filters, sharp TBW FIR filter with desired cut-off frequency can be realized. Also, the architecture in Fig. 2.16 provides LP, HP, BP and BS responses without the need of coefficient upgrades and hardware re-implementation. The multiplier complexity of an FIR filter design using the FRM technique is much lower than conventional FIR filters designed using Eq. (2.1) especially when sharp TBW is desired [82] but at the expense of larger group delay.

In [31, 33], low complexity VDFs, based on single and multi-stage FRM approaches, are proposed. The cut-off frequency of the FRM-VDF can be changed either by changing the interpolation factor, M, and by suitably selecting the subbands in $H_a(z^M)$ and $H_c(z^M)$. Though the complexity of the FRM-VDF is less compared to other VDFs, FRM-VDFs can provide only coarse control over the cut-off frequency since M is limited to positive integer values. In case of the FRM-VDF with wider cut-off frequency range, M may need to vary over large range. However, as M increases, subbands in multi-band response will be located close to each other and hence masking filters with very sharp TBWs would be

.....

Chapter 2 – Literature Review: - Variable digital filters and reconfigurable filter banks

required to extract the desired subbands from the multi-band response. Since, the order and hence the complexity of the masking filters is inversely proportional to the TBW, the overall complexity of the FRM-VDF also increases. Furthermore, only coarse control over the cut-off frequency is possible in [31, 33] which limits their operation in multistandard scenario as well as when in-field upgradeability is desired. In [86], a low complexity VDF using FFB is proposed which provides fine control over the cut-off frequency on a wide frequency range. However, due to the multi-stage architecture, it cannot be extended to the design of reconfigurable filter banks.

To provide unabridged control over the cut-off frequency and limit the range of M within small values, new VDF is proposed in [23] where each sub-filter of the FRM technique is replaced with the SPA-VDF as shown in Fig. 2.18. It is termed as SPA-FRM VDF. The interpolation factor, M and tuning parameter, α decide the cut-off frequency of the SPA-FRM VDF. The combination of the SPA-VDF and the FRM technique results in smaller range of M and hence lower group delay, fine control over the cut-off frequency compared to [31, 33] and lower implementation complexity compared to [41-50]. Though



the range of M is small which results in fewer number of masking filters (compared to [31, 33] where separate masking filters are designed for each M), the overall complexity of masking filters is still high since the separation between adjacent subband is same due to the VDF in the first stage. Furthermore, designing reconfigurable filter banks using the FRM-VDF is a tedious and complicated task since the FRM approach is itself multi-stage and difficult to incorporate into the DFTFB and the FFB architecture. Similarly, FRM-VDFs are not computationally efficient when multiple responses, each with distinct cut-off frequency, are required.

2.4.5 Coefficient Decimation Based VDFs

The CDM (CDM-I and CDM-II) are commonly used to design low complexity reconfigurable filters and filter banks [24, 25, 27-31]. They are discussed in detail in Section 2.3.2 and 2.3.4. The main advantages of CDM-VDFs are that they provide variable LP, HP, BP and BS responses from a fixed-coefficient lowpass prototype filter without any additional cost of multipliers and can vary the cut-off frequency over entire Nyquist band. In [24, 25, 27-31], applications of the CDM for channelization and spectrum sensing operation in MWCRs are discussed. However, CDM-VDFs provide only coarse control over the cut-off frequency which limits their operation in multistandard scenario as well as when in-field upgradeability is desired. For example, if the cut-off frequency and the cut-off slope of prototype filter are f_c and TBW respectively, then the relation between f_{cD} , TBW_D and integer decimation factor, D_H is given by

$$f_{cD} = f_c \cdot D_{II} \tag{2.20}$$

▶ Page 54

$$TBW_D = TBW \cdot D_{II} \tag{2.21}$$

From Eq. (2.20), it can be observed that f_c should be small to provide an unabridged control over f_{cD} since the separation between adjacent f_{cD} is f_c and D_{II} takes only positive integer values. On the other hand, smaller f_c leads to wider range of D_{II} . Since, the TBW, passband and stopband ripples of the decimated response deteriorates as D_{II} increases, the prototype filter needs to be over-designed. Thus, the CDM alone cannot be used for the design of reconfigurable filters and filter banks where an unabridged control over the subband bandwidth and the center frequency is desired. For an easy understanding, comparison between different VDFs discussed above is summarized in Table 2.2.

2.5 Summary

In this chapter, a brief review of MWCRs is presented along the various functionalities of the DFE in emerging SDRs and CRs. The limited reconfigurability of the analog frontend, sampling rate constraints of the today's ADC and extensive disparities between communication standard's specifications, e.g. channel bandwidths from 200 kHz for the GSM up to 1.25 MHz - 20 MHz in the LTE, lead to the shifting of stringent channel(s) selection task to the DFE. Thus, the DFE needs either variable digital filters (VDFs) that provide variable LP, HP, BP and BS responses, or reconfigurable filter banks that provide independent and individual control over the bandwidth and the center frequency of subbands.

	Gut	Group Delay	Reconf. Delay	Phase	RAM/	variable LP, HP, BP and		
VDFs	Gate Count					BS responses over entire		
					ROM	Nyquist band		
Programmable filter [74-79]	Low	Low	Very high	Linear	Yes	Yes		
APT-VDFs [51, 67-69]	High	NA	Low	Non- linear	No	Need of separate first and second order APTs leads to very high gate count complexity.		
Frequency transformation VDFs [36-40]	High	High	Low	Linear	No	Needofseparatetransformationsleadstoveryhighgatecountcomplexityandlimitedcut-offfrequencyrange.		
SPA-VDFs [41-50]	Very high	Very low	Low	Linear	No	Yes but preferred for short range of Nyquist band due to very high complexity.		
FRM-VDF [31, 33, 86]	Very Low	Very high	Low	Linear	No	Coarse control over bandwidth and center frequency.		
SPA-FRM VDF [23]	Very high	Very high	Low	Linear	No	Yes		
CDM-VDF [24]	Low	Low	Low	Linear	No	Coarse control over bandwidth and center frequency.		

TABLE 2.2. COMPARIOSN OF DIFFERENT VDFS

Various filter bank design approaches such as PC approach [7], modulated filter bank approach [7, 20, 21, 25], FFB approach [22, 26, 32] and CDM based approach [24, 25, 27-31] were reviewed. The PC approach provides a great deal of flexibility in the design of non-uniform fixed-filter banks when the bandwidth and the center frequency of all

subbands are fixed and known in advance. However, the complexity of the PC approach increases linearly with the number of subbands and the reconfigurability is achieved by updating the filter coefficients. The modulated filter banks, such as DFTFB [7, 20], MPRFB [21], CDM-DFTFB [25], GFB [7] etc., are computationally efficient (lower hardware cost and multiplication rate) than the PC approach when the resolution of filter bank i.e. number of subband is larger (\geq 2). However, they fail to provide an independent and individual control over the bandwidth as well as the center frequency of subbands. The FFB [22], multi-resolution FFB [26] and non-uniform FFB [32] provide low complexity alternative to modulated filter banks but they have same drawbacks as that of modulated filter banks. The CDM based reconfigurable filter banks [24, 25, 27-31] provide independent and individual control over the bandwidth and the center frequency of subbands. However, due to integer decimation factor, they provide limited and only coarse control over subband bandwidth and their center frequencies.

A detailed literature review of various VDF design such as programmable filters [74-79], frequency transformation based VDFs [36-40, 51, 67-69], SPA-VDFs [41-50], FRM-VDFs [23, 31, 33, 86] and CDM-VDFs [24, 27-30] was presented. Most of the existing VDFs have limited cut-off frequency range and need to update filter coefficients and employ parallel structures to obtain variable LP, HP, BP, BS responses etc. Realizing VDF and reconfigurable filter bank architectures with the least area complexity, power consumption, group delay as well as reconfiguration delay is a challenging task and hardly addresses in literature. In the next chapters, proposed low complexity, reduced delay VDF and reconfigurable filter bank architectures are presented.

Chapter 3 Reconfigurable Filter Bank Based on Coefficient Decimation Method and Frequency Response Masking

The digital front-end (DFE) in the multi-standard wireless receivers (MSWRs) of emerging software defined radios (SDRs) and cognitive radios (CRs) employs filter bank to simultaneously extract multiple channel(s) corresponding to distinct communication standards [20]. To perform this task efficiently using same filter bank instead of using multiple filter banks in parallel, the filter bank architecture must be dynamically reconfigurable i.e. the filter bank should provide control over the bandwidth as well as the center frequency of subbands with minimum hardware overhead. This chapter presents the first contribution of this thesis which is a low complexity and reconfigurable filter bank based on coefficient decimation method (CDM) and frequency response masking (FRM) technique. It shall be referred to as CDM-FRM filter bank. Compared to existing CDM filter banks [25, 27-30] and FRM filter banks [24, 26], proposed CDM-FRM filter bank is the first one which combines all three techniques namely CDM-I, CDM-II and FRM and offers coarse control over subband bandwidth for sharp transition bandwidth (TBW) response without compromising on implementation complexity. The applications

of the CDM-FRM filter bank in channelization and accurate estimation of frequency edges of multiple channels, corresponding to different communication standards, present in a wideband input signal for commercial as well as military wireless communication receivers are discussed in the latter part of this chapter. In the next Section, the CDM and an interpolation technique are elaborated in brief.

3.1 Review of Coefficient Decimation Methods and Interpolation Technique

In [24], two methods namely coefficient decimation method-1 (CDM-I) and coefficient decimation method-II (CDM-II) are proposed for the realization of reconfigurable filters and filter banks. In CDM-I, every D_I^{th} coefficient of the prototype filter is kept unchanged and all other coefficients are replaced by zeros to get multi-band response with identical passband width and TBW as that of original filter. The subbands in multi-band response are located at an integer multiple of $\left(\frac{2\pi}{D_I}\right)$ on normalized frequency scale (i.e. 0 to π). Fig. 3.1(b) and Fig. 3.1(c) shows the frequency responses obtained using the CDM-I from the prototype filter in Fig. 3.1(a) for D_I of 2 and 4 respectively. For example, if $\{h_0, h_1, h_2, h_3, h_4, \dots, h_{N-I}, h_N\}$ are filter coefficients of prototype filter shown in Fig. 3.1(c) are $\{h_0, 0, h_2, 0, \dots, 0, h_N\}$ and $\{h_0, 0, 0, 0, h_4, \dots, 0, 0, 0, h_N\}$, respectively.

In CDM-II, every D_{II} th coefficients of the prototype filter are grouped together discarding in between coefficients to obtain a decimated frequency response whose cut-



Fig. 3.1. (a) Frequency response of the prototype filter, (b) Frequency response obtained from filter in (a) using the CDM-I for $D_I = 2$, (c) Frequency response obtained from filter in (a) using the CDM-I for $D_I = 4$, (d) Frequency response obtained from filter in (a) using the CDM-II for $D_{II} = 2$, (e) Frequency response obtained by interpolating the filter in (a) by M = 8.

off frequency and the TBW are D_{II} times that of original filter [24]. Fig. 3.1(d) shows the frequency response obtained using the CDM-II from the prototype filter in Fig. 3.1(a) for $D_{II} = 2$ and corresponding filter coefficients of decimated filter are $\{h_0, h_2, h_4, \dots, h_N\}$. The CDM-II is used to obtain variable bandwidth frequency responses in the CDM-FRM filter bank. In CDMs, the stopband ripple and the TBW deteriorate with increase in decimation factors and hence the prototype filter needs to be over-designed.

Interpolation by *M* consists of replacing each delay of the prototype filter by *M* delays resulting in a (M+1)-band response with the passband width and the TBW of all subbands *M* times smaller than that of an FIR filter [82]. Fig. 3.1(e) shows the multi-band frequency response obtained by interpolating the filter in Fig. 3.1(a) and corresponding filter coefficients of decimated filter are { h_0 , 0, 0, 0, 0, 0, 0, 0, h_1 , 0, 0, 0, 0, 0, 0, 0, h_2 h_N }. The interpolation factor, *M*, as well as the decimation factors, D_I and D_{II} , are limited to positive integer values.

3.2 Proposed CDM-FRM Filter Bank

Existing reconfigurable filter banks [24-30] are designed using either CDM or FRM technique. The CDM based filter banks [25, 27-30] allow coarse control over subband bandwidth but their complexity is very high when sharp TBW is desired. The FRM based filter banks [24, 26] offer variable subband bandwidths by changing the interpolation factor of the prototype filter of the filter bank and have low complexity when sharp TBW is desired. However, they cannot provide coarse control over subband bandwidth for a given resolution of filter bank. The proposed CDM-FRM filter bank, obtained by combining CDM and FRM techniques, not only offers coarse control over the subband bandwidth but also have lower complexity than CDM based filter banks [25, 27-30] when sharp TBW is desired. The block diagram of the CDM-FRM filter bank is shown in Fig. 3.2. It comprises of three stages:



- 1) The first stage consists of a lowpass linear phase interpolated and decimated FIR filter (called as prototype filter) $H_a\left(z^{M/D_{II}}\right)$, and its complementary filter, $H_c\left(z^{M/D_{II}}\right)$. The first stage provides multi-band response where the (M+1)-subbands are located at integer multiples of $\left(\frac{2\pi}{M}\right)$ on normalized frequency scale (i.e. 0 to π). The bandwidth of subbands in $H_a\left(z^{M/D_{II}}\right)$ and $H_c\left(z^{M/D_{II}}\right)$ are $\left(\frac{2f_c \cdot D_{II}}{M}\right)$ and $\left(\frac{2(1-f_c \cdot D_{II})}{M}\right)$ respectively where f_c is the cut-off frequency of the prototype filter.
- 2) The multiband responses are then fed to the second stage which consists of two banks of masking filters, *Bank 1* and *Bank 2*. Each masking filter extracts the desired subband for which the masking filter is designed, by masking other subbands.
- 3) In the third stage, an adder block combines the individual subbands to provide wide bandwidth subbands, based on the final requirement of desired subband bandwidths.

The detailed design of the CDM-FRM filter bank is given below.

3.2.1 First Stage - Design of Prototype Filter

The first stage of the CDM-FRM filter bank consists of a prototype filter whose passband width can be changed using suitable decimation factor D_{II} employing the CDM-II. Then, the prototype filter is interpolated by a factor of M resulting in an (M+I)-band filter response i.e. $H_a\left(z^{M/D_{II}}\right)$ where the subband bandwidth is $\left(\frac{2D_{II}}{M}\right)$ times the cut-off frequency of the prototype filter and the TBW is $\left(\frac{D_{II}}{M}\right)$ times the TBW of the prototype filter [82]. Thus, the first stage provides variable bandwidth subbands, whose design steps are as follows:

- Determine the minimum subband bandwidth (β) and resolution (M) of the filter bank depending upon the desired filter bank specifications. Both the parameters are fixed for a given architecture. All the frequency edges mentioned here are normalized with respect to half the sampling frequency.
- 2) Depending upon *M*, the range of the CDM-II factor, $D_{IImin} \leq D_{II} \leq D_{IImax}$, and the prototype filter's passband and stopband edges, f_{pass} and f_{stop} respectively, are chosen to obtain uniform as well as non-uniform subbands and meet the bandwidth, β . There are multiple sets of D_{II} , f_{pass} and f_{stop} which results in minimum bandwidth β for a given *M*. However, f_{pass} and f_{stop} must satisfy two conditions additionally, which are:
 - a) To avoid aliasing, $D_{IImax} \cdot f_{stop} \le 1$ [24].

b) The selected f_{pass} should fall within the values obtained using Eq. (3.1) and Eq. (3.2) for a given range of D_{II} .

$$f_{pass(min)} = \left(\frac{M \times \beta}{D_{IImin} \times 2}\right)$$
(3.1)

$$f_{pass(max)} = \left[\left(\frac{1}{M} - \frac{\beta}{2} \right) \times \frac{M}{D_{IImax}} \right]$$
(3.2)

- 3) As decimation operation by D_{II} would deteriorate the stopband ripple and the TBW, the $H_a(z)$ needs to be over-designed with upper stopband attenuation and sharper TBW [24]. If the required stopband ripple of the CDM-FRM filter bank is $\delta_{s(filterbank)}$, then the stopband ripple of $H_a(z)$ is $\left(\frac{\delta_{s(filterbank)}}{D_{II}}\right)$ [24]. Similarly, if the desired TBW is $TBW_{filterbank}$, then TBW of the $H_a(z)$ is $\left(\frac{M}{D_{II}} \cdot TBW_{filterbank}\right)$ [24].
- 4) Generate an N^{th} order lowpass prototype filter, $H_a(z)$, with the specifications obtained from steps 2-3. The complementary filter response, $H_c\left(z^{M/D_{II}}\right)$, is obtained by subtracting $H_a\left(z^{M/D_{II}}\right)$ from appropriate delayed version of the input signal [82]. Due to the CDM-II by factor D_{II} and interpolation by factor M, the effective length of prototype filter is increased by $\left(\frac{M}{D_{II}}\right)$ (assuming that $M > D_{II}$) [24]. The number of delays to obtain complementary response is given as,

$$N_{Delays} = \left\{ \left(\left\lfloor \frac{N-1}{2} \right\rfloor + \left(\left\lfloor \frac{N-1}{D_{II}} \right\rfloor mod2 \right) \right) \frac{M}{2} \right\}$$
(3.3)

The dependence of the subband bandwidth on D_{II} is demonstrated using frequency responses shown in Fig. 3.3. Fig. 3.3 (a) shows the frequency response of the prototype filter, $H_a(z)$, and its complementary filter, $H_c(z)$. In Fig. 3.3 (b), the frequency responses of decimated and interpolated prototype filter, $H_a\left(z^{M/D_{II}}\right)$ and its complementary, $H_c\left(z^{M/D_{II}}\right)$ when $D_{II} = D_{IImin}$ are shown. Fig. 3.3 (c) shows the frequency responses of $H_a\left(z^{M/D_{II}}\right)$ and $H_c\left(z^{M/D_{II}}\right)$ when $D_{II} = D_{IImax}$. As the value of D_{II} is increased from D_{IImin} to D_{IImax} , the bandwidth of the subbands in $H_a\left(z^{M/D_{II}}\right)$ increases while the bandwidth of subbands in $H_c\left(z^{M/D_{II}}\right)$ decreases and vice versa. Fig. 3.4 (a) and Fig. 3.4 (b) show the variation of bandwidth of the subbands in $H_a\left(z^{M/D_{II}}\right)$ and $H_c\left(z^{M/D_{II}}\right)$ as D_{II} is varied. When $D_{II} = D_{IImin}$, the bandwidth of the subbands in $H_a\left(z^{M/D_{II}}\right)$ and $H_c\left(z^{M/D_{II}}\right)$ as (smallest bandwidth) and when $D_{II} = D_{IImax}$, bandwidth of subbands in $H_c\left(z^{M/D_{II}}\right)$ is β .



Fig. 3.3. Multi-band responses obtained using first stage of the CDM-FRM filter bank.

Since the factor D_{II} for $H_a(z^{M/D_{II}})$ and $H_c(z^{M/D_{II}})$ is controlled independently, all the subbands can have bandwidth β (narrowband) or $(\frac{2}{M} - \beta)$ (wideband) simultaneously.

3.2.2 Second Stage - Design of Masking Filter

The CDM-FRM filter bank consists of two banks of masking filters, 1) *Bank 1* for $H_a(z^{M/D_{II}})$, and 2) *Bank 2* for $H_c(z^{M/D_{II}})$ as shown in Fig. 3.2. These two masking filter banks are designed independently and consist of fixed-coefficient masking filters to extract variable bandwidth subbands obtained from the first stage. It is not required to reconfigure the masking filters unlike in existing FRM technique where the masking filters need to be reconfigured to match with the specifications of multiple communication standards [87]. The passband and stopband frequencies of masking filters of *Bank 1* are obtained using the frequency plot of $H_a(z^{M/D_{II}})$ for $D_{II} = D_{IImax}$ shown in Fig. 3.5 where all subbands have largest bandwidth. Similarly, the passband and stopband



Fig. 3.4. Frequency responses of prototype and complementary filters of the CDM-FRM filter bank for different values of D_{II} .

frequencies of masking filters of *Bank 2* can be obtained using frequency plot of $H_c(z^{M/D_{II}})$ for $D_{II} = D_{IImin}$. The design equations for masking filters (as can be observed from Fig. 3.5) are specified below:

1) The passband frequencies of masking filter $(f_{p(mask)})$ are given as,

$$f_{p1(mask)} = f_{center1} - \left(TBW_{filterbank} \cdot \frac{D_{IImax}}{M}\right) + \frac{\beta}{2}$$
(3.4 a)

$$f_{p2(mask)} = f_{center2} - \left(TBW_{filterbank} \cdot \frac{D_{IImax}}{M}\right) - \frac{\beta}{2}$$
(3.4 b)

2) Similarly, the stopband frequencies of masking filter ($f_{s(mask)}$) are given as,

$$f_{s1(mask)} = f_{center1} + \left(TBW_{filterbank} \cdot \frac{D_{IImax}}{M}\right) - \frac{\beta}{2}$$
(3.5 a)

$$f_{s2(mask)} = f_{center2} - \left(TBW_{filterbank} \cdot \frac{D_{IImax}}{M}\right) + \frac{\beta}{2}$$
(3.5 b)



Fig. 3.5. Frequency plot indicating the passband and stopband frequencies of masking filters when $D_{II} = D_{IImax}$.

where β is the minimum subband bandwidth, (*fcenter1*, *fcenter2*) are the center frequencies of adjacent subbands as shown in Fig. 3.5. Since the frequency edge specifications of the masking filter, given by Eq. (3.4) and Eq. (3.5), are fixed and independent of the prototype filter, fixed-coefficient masking filters can be used. The implementation complexity of fixed-coefficient filters can be reduced further by replacing coefficient multiplication operation with shift and addition operations [88, 89] and incorporating the multiplier block technique to reduce the number of adders [90]. In the CDM-FRM filter bank, *M* is fixed depending on the desired resolution and masking filters are designed for a given interpolation factor, *M*. When *M* is changed, number of subbands and their center frequencies changes and hence, different set of masking filters will be required.

For (M+1)-subband filter bank, conventional approach [87, 91] is to use one masking filter for each subband. Though this approach reduces the design effort significantly, it leads to larger hardware complexity and power consumption. In the CDM-FRM filter bank, the CDM-I is employed to reduce the number of masking filters, which is explained later in Section 3.3.

3.2.3 Third Stage - Adder Block

The third stage of the CDM-FRM filter bank consists of an adder block. The purpose of the Adder block is to combine adjacent subbands to provide wider bandwidth subbands and overcome the fixed channel stacking problem in existing filter banks such as DFTFB [7] and FFB [22]. The detailed design of Adder block is explained in Section 3.3.

3.3 Architecture of CDM-FRM Filter Bank

This section presents the reconfigurable architecture of the CDM-FRM filter bank. The Simulink diagram of the filter bank architecture is shown in Fig. 3.6. It consists of three blocks: Lyrtech signal master controller [92], input signal and Xilinx hardware co-simulation (hwcosim) block along with the Simulink representation of the architecture [103]. The Lyrtech signal master controller consists of three components, (1) Board configuration for configuring the field programmable gate array (FPGA) and for



Fig. 3.6. Simulink diagram of the CDM-FRM filter bank Architecture.

downloading the bit-stream to FPGA, (2) Xilinx's system generator for generating the bit stream to be downloaded to the FPGA, and (3) Log viewer which gives implementation information about area and delay of the architecture used.

The input signal block provides the real time input to the architecture. For illustrative purpose, the values chosen are $\beta = 0.075$ and M = 8 so that a 9-subband filter bank is obtained. The stopband ripple of the filter bank is taken as -30 dB. The f_{pass} and f_{stop} of the prototype filter are selected as 0.083 and 0.115 respectively. The decimation factor D_{II} is varied from 3 to 7. For $D_{II} = 6$, all the subbands are of uniform bandwidth (identical to that of the DFTFB). The length of the prototype filter obtained using Bellanger's formula [72] is 276. The sub-blocks of the CDM-FRM filter bank are shown in Fig. 3.7



Fig. 3.7. Simulink diagram of the three stages of the CDM-FRM filter bank.

representing the inputs and outputs of the three stages. Next, the design of each sub-block is discussed in detail.

The first stage consists of prototype filter with the CDM-II, interpolation and complementary delays to get multiband responses. The detailed architecture of the prototype filter is shown in Fig. 3.8. All the filters in the CDM-FRM filter bank are implemented in transposed direct form to make the critical path delay independent of the filter length. Since M = 8, each unit delay in the prototype filter is replaced by 8 delays. The multiplexer control signals, *Sel_D_{II}* and *Sel_comp*, select the suitable values of *D_{II}* for the prototype filter response and the complementary filter response respectively. Both the signals, *Sel_D_{II}* and *Sel_comp*, are 5 bit wide i.e. 1 bit for each *D_{II}*. For example, 00001, 00010 indicate that *D_{II}* is 3 and 4 respectively and so on. When *Sel* input for multiplexer is '0', it passes the *d0* input and when *Sel* value is '1', the multiplexer passes the *d1* input. For *D_{II}* = 3, filter coefficients *h*(1), *h*(4), *h*(7), *h*(10).. are selected and for *D_{II}* = 6, filter coefficients *h*(1), *h*(7), *h*(13).. are selected. Here, an *OR* gate is used which selects filter



coefficient h(7) in both cases. The upper part of Fig. 3.8, denoted by label A, gives the prototype filter response. The output of the lower part of Fig. 3.8, denoted by label B, is subtracted from an appropriate delayed version of input signal to get the complementary filter response.

Both the outputs of prototype filter and complementary filter are passed to the second stage which consists of banks of masking filters as shown in Fig. 3.7. The masking filters are used to individually extract all the subbands obtained from first stage and their frequency edge specifications are given by Eq. (3.4) and Eq. (3.5). Using conventional masking techniques [87, 91], 9 masking filters are required to separate 9 subbands (band-0 to *band*-8). However, the CDM-I can be used to reduce the number of masking filters from 9 to 4. The architectures of masking filter banks, Bank 1 and Bank 2, are shown in Fig. 3.9 and Fig. 3.10 respectively. In *Bank* 1, masking filter $H_1(z)$ is designed to extract band-0 i.e. $Y_0(z)$. Then, using the CDM-I with value of D_I as 2 on $H_1(z)$, frequency response, $Y_{08}(z)$, containing band-0 and band-8 is obtained (according to Fig. 3.1(b)). By subtracting $Y_0(z)$ from $Y_{08}(z)$, response with band-8 i.e. $Y_8(z)$ is obtained. Similarly, using the CDM-I with value of D_I as 4 on $H_I(z)$, frequency response, $Y_{0.48}(z)$, containing band-0, band-4, band-8 together (according to Fig. 3.1(c)) is obtained and then by subtracting $Y_{08}(z)$ from $Y_{048}(z)$, the response, $Y_4(z)$ i.e. band-4 is obtained. Thus, using a single masking filter, $H_1(z)$, and the CDM-I, 3 bands are extracted. Finally, the complementary response of $Y_{048}(z)$ i.e. $Y_{26}(z)$ is passed through the lower order lowpass masking filter, $H_2(z)$, to obtain the response $Y_2(z)$ i.e. band-2 while the complementary response of $H_2(z)$ provides the response $Y_6(z)$ i.e. band-6.



Fig. 3.9. Architecture of masking filter bank (Bank 1)



Fig. 3.10. Architecture of masking filter bank (Bank 2)

In *Bank* 2, the complementary response of the prototype filter is passed through the bandpass masking filter, $H_3(z)$, to obtain the response $Y_3(z)$ i.e. *band*-3 while the CDM-I with value of D_I as 2 on $H_3(z)$ provides the response $Y_{35}(z)$. Then by subtracting the response $Y_3(z)$ from $Y_{35}(z)$, the response $Y_5(z)$ i.e. *band*-5 is obtained as shown in Fig.

3.10. Finally, the complementary response of $Y_{35}(z)$ i.e. $Y_{17}(z)$, is passed through a lower order masking filter, $H_4(z)$, to obtain the response $Y_1(z)$ i.e. *band*-1 and the CDM-I with $D_{II} = 2$ on $H_4(z)$ provides the response $Y_7(z)$ i.e. *band*-7. In this way, all the subbands are obtained at the output of the second stage and by changing D_{II} , the subband bandwidth can be changed. Thus, the CDM reduces the number of masking filters from 9 to 4 which in turn reduces the complexity of the architecture. The extracted subbands are delayed by an appropriate delay value before passing to the third stage. The value of delay depends on the order of masking filters and is selected such that the group delays of all extracted subbands at the input of third stage (i.e. Adder block) are same.

The Adder block architecture shown in Fig. 3.11 combines the adjacent subbands in order to obtain subbands of wider bandwidths. The number of subbands that can be combined are limited to 4 for the design example considered here. However, it is possible to combine more than 4 subbands using additional adders and multiplexers. The Adder block consists of two stages. The inputs to this block are the subbands (i.e. band-0 - band-8) extracted from the masking filter stage and the multiplexer control signal Sel_band. The signal Sel_band is 6-bit wide and can be used to extract any subband of interest. In the first stage of the Adder block, non-adjacent subbands (such as band-0 and band-8 or band-1 and band-7 and so on) are given to the 2-input multiplexers. This is because band-0 and *band*-8 together are seldom required as output in most practical scenarios since they are located apart from each other in frequency domain. The outputs of multiplexers are combined combinational outputs COMB UP1, COMB DOWN2, to obtain COMB_DOWN3 as shown in Fig. 3.11. For example, the output COMB_UP1 consists of



Fig. 3.11. Architecture of the Adder block.

either *band*-0 and *band*-1 together or *band*-7 and *band*-8 together depending on the value of *Sel_band*. The second output *COMB_UP2* is complementary to *COMB_UP1* such that when the output *COMB_UP1* consists of addition of *band*-0 and *band*-1, *COMB_UP2* consists of addition of *band*-7 and *band*-8 and vice versa. Similarly, the outputs *COMB_DOWN2*, *COMB_DOWN3* contain addition of either *band*-2 and *band*-3 or *band*-5 and *band*-6.

In the second stage of the Adder block, outputs of first stage are given to 2-input multiplexer. The outputs of multiplexers are combined to obtain *COMB_DOWN1*, *COMB* and *COMB1*. Table 3.1 shows the bands obtained for some of the combinations of *Sel_band*. For example, the output *COMP_UP1* is given by,

$$COMB_UP1 = \{Sel_band(0)[band - 7 + band - 8]\} + \{\overline{Sel_band(0)}[band - 0 + band - 1]\}$$
(3.6)

When $Sel_band(0) = 0$, $COMB_UP1 = band-0 + band-1$ and when $Sel_band(0) = 1$, $COMB_UP1 = band-7 + band-8$. Thus, at the output of third stage of the CDM-FRM filter bank, non-uniform subbands are obtained from combinations of adjacent subbands along with original subbands extracted by second stage. This makes the CDM-FRM filter bank architecture suitable for non-uniform channelization.

The decimation factor, D_{II} , of the prototype filter and the complementary filter is TABLE 3.1. SPECIFICATION OF CHANNELS EXTRACTED BY ADDER BLOCK FOR DIFFERENT

VALUES OF SEL_BAND

Sel_band	COMB	COMB1	COMB	COMB	COMB_	COMB_	COMB_
			_UP1	_UP2	DOWN1	DOWN2	DOWN3
1000000	0+1+2	5+6+7+	0+1	7+8	2	2+3	5+6
		8					
0100000	0+1+2+	5+6+7+	0+1	7+8	2+3+4	2+3	5+6
	3+4	8					
0111111	4+5+6+	0+1+2+	7+8	0+1	4+5+6	5+6	2+3
	7	3					
0101000	1+2+4	5+6+7+	0+1	7+8	2+3	2+3	5+6
		8					

controlled individually using Sel_D_{II} and Sel_comp respectively. Depending upon Sel_D_{II} and Sel_comp , there are two modes of operations of the CDM-FRM filter bank:

- 1) In the first mode, D_{II} is chosen such that the bandwidth of all the subbands is same and equal to $\left(\frac{2D_{II}}{M}\right)$ times the cut-off frequency of the prototype filter. For example, if *Sel_* $D_{II} = 00001$ ($D_{II} = 3$ for prototype filter) and *Sel_comp* = 10000 ($D_{II} = 7$ for complementary filter), the bandwidth of all subbands, using prototype filter with $f_{pass} =$ 0.083, $f_{stop} = 0.115$, M = 8, is 0.075 (narrowband). Similarly, when $D_{II} = 7$ for prototype filter and $D_{II} = 3$ for complementary filter, the bandwidth of all subbands is 0.2 (wideband). In this way, proposed filter bank allows extraction of extremely narrowband as well as wideband channels from wideband input signal. This is identical to the subband bandwidth variations obtained using recently proposed CDM-DFTFB [25]. This mode of operation is selected when bandwidth of all channels in wideband input signal is equal and changes in chorus while channels locations are fixed and known in advance.
- 2) The main drawback of first mode and the CDM-DFTFB [25] is that all subbands are either disjoint (narrowband case) or overlapped (wideband case) which happens when decimation factor D_{II} is different for prototype and complementary filters. This is not favorable in spectrum sensing operation where entire bandwidth need to be searched and in non-uniform channelization where individual channel bandwidth and location varies dynamically. For such cases, decimation factor D_{II} for prototype and

complementary filter is kept same and adjacent subbands of filter bank can be combined using adder stage.

Overall, the CDM-FRM filter bank overcomes the fixed subband bandwidth limitation of the DFTFB, the FFB and their modifications and provides the subband bandwidths which are fractional multiples of each other. By combining adjacent subbands and changing D_{II} , the problem of fixed channel stacking in the DFTFB and the FFB is overcome in the CDM-FRM filter bank.

3.4 Implementation Complexity Comparison

The implementation complexity of the CDM-FRM filter bank is compared with that of other filter banks in terms of total estimated gate count. A 16x16 bit multiplier, a 2:1 multiplexer, 16 bits of memory and 32 bit adder were synthesized on a TSMC 0.18µm process. The Synopsys Design Compiler was used to estimate the cell area. The area in terms of gate count is obtained by normalizing the cell area values by that of a two input NAND gate from the same library. The total estimated gate count in Table 3.2 is the sum of gate counts of all the components in the filter bank. The values " $\pm x$ %" in last column of Table 3.2 indicates the difference in percentage gate counts when compared with the CDM-FRM filter bank.

In the specific design example of the CDM-FRM filter bank presented in Section 3.3, the length of prototype filter is 276. Similarly, the length of masking filters, $H_1(z)$ and $H_3(z)$ is 65 and that of $H_2(z)$ and $H_4(z)$ is 21 using Bellanger's formula [72]. As the

TABLE 3.2 GATE COUNT COMPLEXITY COMPARISON OF CDM-FRM FILTER BANK WITH

Filter banks	No. of multiplications	No. of adders	No. of MUXs	Total delay in samples	Total gate count
PC approach [7]	459	900	0	51	936900 (+151%)
DFTFB [7]	161	320	0	97	329600 (-11%)
CDM-DFTFB [25]	265	528	400	201	556800 (+49%)
FFB [22]	111	151	0	169	211575 (-43%)
CDM filter bank [24]	305	610	500	283	642750 (+72%)
CDM-FRM filter bank	179	358	157	772	372445

OTHER FILTER BANKS

prototype filter and all masking filters have symmetrical coefficients and transposed direct form filter structure is employed, the number of coefficient multiplications is reduced by half. Also, as the CDM-II is employed with $3 \le D_{II} \le 7$, 48 out of 139 prototype filter coefficients are discarded.

For a fair comparison, 9 filters employed in the PC approach and they are designed with same magnitude response specifications as that obtained by the CDM-FRM filter bank with $f_{pass} = 0.083$, $f_{stop} = 0.115$, M = 8 and D = 7. The total number of multiplications for the PC approach is 459 (9 filters corresponding to 9 subbands each of length 101 with symmetric coefficients). The PC approach requires 151% higher gate count compared to the CDM-FRM filter bank. Moreover, in the CDM-FRM filter bank, the bandwidth of subbands can be varied by changing D_{II} as discussed in Section 3.2. In the PC approach,

the filter coefficients need to be updated to meet the desired specifications which require large memories and larger reconfiguration delay compared to the CDM-FRM filter bank.

As mentioned in Section 3.2, the CDM-FRM filter bank produces output similar to the uniform DFTFB [7] and uniform FFB [22] when $D_{II} = 6$. Though the gate counts of the CDM-FRM filter bank are larger than the DFTFB and the FFB, it provides on-the-fly control over subband bandwidth compared to the DFTFB and the FFB where the subband bandwidth is fixed and equal. The CDM-DFTFB [25] and the CDM based filter bank [24] are designed to provide identical control over the subband bandwidth as that of design example presented in Section 3.3. The CDM-FRM filter bank provides 49% and 72% of reductions in total gate count compared to these two filter banks respectively. As discussed in Section 3.3, in case of the CDM-DFTFB [25], variation of subband bandwidth results in disjointedness or overlapping of subbands which may not be favorable in applications such as spectrum sensing or channelization. The CDM-FRM filter bank avoids disjointedness or overlapping of subbands by selecting same value of D_{II} for the prototype filter and the complementary filter. However, the CDM-FRM filter bank has higher group delay compared to other filter banks.

The CDM-FRM filter bank, the CDM-DFTFB and the PC approach architecture are implemented on Xilinx Virtex-2 FPGA associated with the dual DSP-FPGA Signal master kit provided by Lyrtech [92]. The CDM-FRM filter bank is implemented with 16bit precision while the PC approach and the CDM-DFTFB are implemented with 14-bit precision. This is because the requirement of the number of taps (and hence number of

slices and area) in the CDM-FRM filter bank is low compared to other approaches. A model based design using Matlab's Simulink and Xilinx's System generator was employed for the implementation purpose [103]. The system generator provides the hwcosim interface that makes it possible to directly incorporate a design running on signal master FPGA in a Simulink simulation [103]. The bit stream of the proposed simulation architecture, generated using the Xilinx system generator, can be downloaded to FPGA using the board configuration block. The performance of the bit stream and the simulation architecture were checked to ensure that they are identical. The power consumption figures were calculated using timing and power analysis tool of Xilinx system generator [103]. The area results are obtained using log viewer block provided by Lyrtech. The implementation results are summarized in Table 3.3. Table 3.3 shows that the PC approach [7] and the DFTFB [25] require 41% and 23% higher slices respectively, 134% and 8.6% higher power consumption respectively compared to the CDM-FRM filter bank. However, the total delay of the PC approach and DFTFB are less than that of CDM-FRM filter bank by 38% and 12% respectively.

Filter Banks	PC Approach [7]	CDM-DFTFB [25]	CDM-FRM filter bank
Total slices	14334	12475	10157
Total power (mW)	1473	750	690
Total delay (ns)	11.533	26.549	30.12

 TABLE 3.3 IMPLEMENTATION COMPLEXITY COMPARISON FOR CDM-FRM FILTER BANK

3.5 Application: Non-uniform Channelization

The functionality of the CDM-FRM filter bank for non-uniform channelization operation is validated for different input signal spectrum scenarios. Wideband input

signals consisting of channels of distinct bandwidth, as shown in Fig. 3.12(a), Fig. 3.13(a), Fig. 3.14(a) and Fig. 3.15(a), are given to the CDM-FRM filter bank. The bandwidths of different channels are given in Table 3.4. All the channels are successfully extracted using the CDM-FRM filter bank architecture by selecting appropriate value of *Sel_D_{II}*, *Sel_comp* and *Sel_band*. For example, all the channels shown in Fig. 3.12(a) are extracted by choosing *Sel_D_{II}* = 1, *Sel_comp* = 1 and *Sel_band* = 34. The individual extracted channels are shown in Fig. 3.12(b)–3.12(f). Similarly, individual extracted channels corresponding to inputs in Fig. 3.13(a), Fig. 3.14(a) and Fig. 3.15(a) are shown in Fig. 3.13(b) - (e), Fig. 3.14(b) - (e) and Fig. 3.15(b) - (d) respectively. Other filter bank architectures such as PC approach, DFTFB and FFB needed to reconfigure their prototype filter to extract channels corresponding to different inputs. To insure that CDM-FRM filter bank does not cause amplitude distortion, the mean square error (MSE) is calculated and shown in Table 3.4 where $MSE = E\{(S_{ec} - S_{in})^2\}$ where *E* is an expectation operator, *S_{in}* and *S_{ec}* are the samples of extracted channels and corresponding input signal, respectively. Smaller MSE values indicate good channelization performance.

BW	(Fig. 3.12)		(Fig. 3.13)		(Fig. 3.14)		(Fig. 3.15)	
Channels	BW	MSE	BW	MSE	BW	MSE	BW	MSE
Channel 1	0.14	0.1014	0.16	0.1004	0.19	0.1054	0.37	0.1090
Channel 2	0.061	0.0324	0.06	0.0366	0.204	0.0494	0.091	0.0992
Channel 3	0.28	0.0632	0.13	0.0197	0.09	0.0278	0.28	0.0623
Channel 4	0.045	0.0732	0.19	0.0992	0.05	0.0614	-	-
Channel 5	0.11	0.0123	-	-	-	-	-	-

TABLE 3.4. BANDWIDTH AND MSE FOR DIFFERENT CHANNELS


Fig. 3.12. (a) Input signal, (b) – (f) Channels extracted using the CDM-FRM filter bank.



Fig. 3.13. (a) Input signal, (b) – (e) Channels extracted using the CDM-FRM filter bank.



Fig. 3.14. (a) Input signal, (b) – (e) Channels extracted using the CDM-FRM filter bank.



Fig. 3.15. (a) Input signal, (b) – (d) Channels extracted using the CDM-FRM filter bank.

▶ Page 84

3.6 Application: Detection of Frequency Band Edges

In a multi-standard military communication receiver (MMCR), it is required to sense the wideband input signal consisting of multiple channels of distinct bandwidths and unknown center frequencies. When compared to commercial MWCRs such as CRs, MMCRs have only little priory information about the input signal [13]. The key task of the MMCR is to sense the entire spectrum as fast as possible in order to accurately detect the frequency edges of multiple channels present in a wideband input signal. Due to the channel fading, interference and hidden terminal problems, a reliable, low complexity and fast spectrum sensing is one of the most vital requirements in MMCRs.

There are various filter bank based spectrum sensing approaches in the literature such as single-stage sensing using matched filtering [93], energy based detection [93], cyclostationary feature based detection (CFD) [93] as well as more accurate two-stage sensing techniques such as coarse detection followed by serial detection [94] or energy detection followed by CFD [95]. Matched filtering is the optimum method for signal detection since it maximizes the signal-to-noise ratio (SNR). But match filtering requires prior knowledge of the input signal which makes it non-suitable for MMCRs. The energy detection is the most common method for signal detection because it does not require a priori knowledge of input signal and low implementation complexity [93]. But it suffers from poor performance at low SNR. The CFD takes advantage of cyclostationary properties of the input signal and have better performance than the energy detection at low SNR [93]. But the computation of spectral correlation function in the CFD is a highly complex task. Hence, to meet the complexity, time and reliability requirements of

MMCRs, two-stage spectrum sensing has been proposed in [94, 95]. It consists of coarse detection stage followed by the fine detection stage. For example in [94, 95], the energy detection is employed in the coarse detection stage where detection time is more important. Then, if necessary, either energy detection [94] or CFD [95] is performed in the second stage. The advantage of employing the CFD in second stage is the complexity reduction because the CFD is performed only when the energy detection fails to identify the signal. In MMCRs, the channel bandwidth and their edge frequencies vary over time and these two parameters are often not governed by a fixed rule as opposed to commercial communication receivers. Hence, accurate estimation of edge frequencies of multiple channels present in the wideband input spectrum is a key task in MMCRs.

In this application of the CDM-FRM filter bank, the focus is on coarse detection part of the two-stage spectrum sensing which detects multiple channels using energy detectors and an algorithm to accurately estimate the edges of the channels present in the wideband input spectrum is presented.

3.6.1 CDM-FRM Filter Bank Based Energy Detector

The block diagram of the proposed scheme is shown in Fig. 3.16. It consists of the (M+1)-band CDM-FRM filter bank followed by energy detectors for each subband. The outputs of each detector are fed to the edge detection algorithm which calculates the edge frequencies of all the channels present in the wideband input signal.



Fig. 3.16. The CDM-FRM filter bank based spectrum sensing scheme.

The aim of the energy detector is to calculate the energy of the signal in each subbands. Consider the received input signal, y(n), as

$$y(n) = s(n) + w(n)$$
 (3.7)

where s(n) is the primary user signal and w(n) is the addictive white Gaussian noise (AWGN). The decision metric for the energy detection is given by,

$$P = \sum_{n=0}^{N} |y(n)|^2$$
(3.8)

The decision metric, P, is compared with a threshold, T_0 , to determine the presence of a primary signal. The threshold, T_0 , is determined based on the noise level in the signal and stopband ripple of the filter bank [93]. In the proposed method, (M + 1) energy detectors

determine the decision metric, P, for each value of D_{II} and pass it to the edge detection algorithm. The matrix P has (M + 1) columns and one row for each value of D_{II} . Thus, for the CDM-FRM filter bank, matrix P has 9 columns and 5 rows. The comparison of $P_{D.M}$ (where $P_{D.M}$ corresponds to the decision metric for subband M and decimation factor D_{II}) with T_0 is done in the edge detection algorithm stage. For the analysis, following assumptions about the input signal spectrum are made:

- The number of channels, their bandwidths and locations are unknown to the MMCR. This information may change over time but assumed to be unchanged during one cycle of sensing.
- The range of frequencies over which sensing needs to be performed (bandwidth of wideband input signal) is known to the MMCR.
- 3) The power spectral density within each subband is assumed to be almost flat.
- 4) The input noise is the AWGN with zero mean and unit variance.

One cycle of spectrum sensing corresponds to the maximum time required to scan through the entire frequency range with the required frequency resolution. In the proposed method, one cycle of spectrum sensing consists of following steps:

- 1) Set D_{II} to its middle value. For the design example considered here, D_{II} takes integer values from 3 to 7 and hence D_{II} is set to 5.
- 2) Run the simulation to obtain *N* samples at the input of each detector and update the decision metric, $P_{D.M}$, using Eq. (3.8) for each of the (*M*+1) i.e. 9 subbands.

- Run the edge detection algorithm to calculate the edge frequencies of all channels present in the input.
- 4) Repeat step 2 for next higher and lower values of D_{II} and then go to step 3 i.e. for $D_{II} = 4$ and $D_{II} = 6$ and run the edge detection algorithm using $P_{4.M}$, $P_{5.M}$ and $P_{6.M}$.
- 5) Repeat step 4 for all values of D_{II} .

3.6.2 Edge Detection Algorithm

The effect of D_{II} on the subband bandwidth is shown in Fig. 3.17 using different colors. Fig. 3.17(a) shows the prototype filter response where subband bandwidth increases with D_{II} and Fig. 3.17 (b) shows the complementary filter response where subband bandwidth decreases with increase in D_{II} . The input to the algorithm is a matrix, *P*.



Fig. 3.17. Illustrative frequency responses of filter bank, (a) Prototype filter response (b)

Complementary filter response.

The first step in edge detection algorithm is to divide the sensing bandwidth into smaller bands and calculate the energies, E_0 , E_1 , present in these bands. This is done serially from band-0 to band-9. For example, E_0 is equal to $P_{3.0}$, E_1 is equal to difference between $P_{4.0}$ and $P_{3.0}$ and so on. Here, it is assumed that $P_{D.M}$ is available for all $D_{II} = 3$, 4, 5, 6, 7. If $P_{D.M}$ is available only for $D_{II} = 4$, 5, 6, then E_0 is equal to $P_{4.0}$, E_1 is equal to difference between $P_{5.0}$ and $P_{4.0}$ and so on.

Once E_0 to E_4 are calculated, next values are obtained using simple subtraction. For example, E_6 is obtained by subtracting E_4 and $P_{7.1}$ from $P_{6.1}$. Also, note that E_0 , E_5 , E_{10} ,... are equal to the respective $P_{D.M}$ values i.e. $P_{3.0}$, $P_{7.1}$ and $P_{3.2}$ respectively.

The next step is to find whether the primary signal is present in these subbands or not. This is done by comparing the band energies, E_x , with the threshold, T_0 . If the energy is greater than T_0 , then signal is present. Otherwise, signal is not present.

In the next step, bands containing the edges of the channels are identified based on the comparison between the energy present in that band and its adjacent bands. For example, if E_0 is less than T_o and E_1 is greater than T_0 , then it is concluded that the rising edge is present in the band with energy, E_1 . Similarly, if E_5 is less than T_0 and E_4 is greater than T_0 , then it is concluded that the falling edge is present in the band with energy, E_4 . In this way, bands containing either rising or falling edges of the channels are identified.

After identifying the bands containing the edges, next step is to find the approximate edge frequency, f_{approx} . The simplest approach is to set the edge frequency equal to the center frequency of the band in which edge is identified. In this approach, the maximum error in calculating the edge frequency is half of the bandwidth. In order to reduce the error further in this work, the edge frequencies are calculated using prediction method which is based on the comparison between the energies present in that band and its adjacent band. This is in accordance with our assumption that power spectral density in each channel is almost flat. For example, if E_2 is much less than E_3 , then it is likely that the rising edge is present at the end of the band rather than at the center of the band. Similarly, if E_2 and E_3 are almost same, then it is likely that the rising edge is present at the center of the band. The prediction method helps in further improving the accuracy of edge detection algorithm.

3.6.3 Simulation Results and Complexity Analysis

The CDM-FRM based scheme is tested under two input signal spectral scenarios where wideband input signal consists of multiple channels whose specifications are given in Table 3.5. Note that all the frequencies are normalized with respect to half the sampling frequency, f_s (= 2π). The 9-subband CDM-FRM filter bank with D_{II} = 3, 4, 5, 6, 7 is considered here. The prototype filter has passband and stopband frequencies as 0.1 and 0.115 respectively with -30 dB stopband ripple. The objective is to find the edge frequencies of all the channels present in input. The energy detectors are assumed to be ideal i.e. probability of miss detection and probability of false alarm is zero. The edge frequencies obtained using our algorithm, f_{approx} , and corresponding error with respect to

actual edge frequencies, f_{actual} , are given in Table 3.5. The percentage error in the edge frequency is given by Eq. (3.9). Note that the errors are low.

$$Error = \frac{\left| \left(f_{actual} - f_{approx} \right) \right|}{\left(\frac{f_s}{2} \right)} \cdot 100$$
(3.9)

Input	Frequency	Channel	factual	fannrox	Error
	bands	frequency	Jucinar	Juppiox	-
Input 1	Channel 1	frising	0	0	0 %
		$f_{falling}$	0.13	0.128	0.2 %
	Channel 2	frising	0.3	0.299	0.1 %
		$f_{falling}$	0.65	0.642	0.8~%
	Channel 3	frising	0.78	0.781	0.1 %
		$f_{falling}$	0.89	0.881	0.9 %
Input 2	Channel 1	frising	0.06	0.058	0.2 %
		$f_{falling}$	0.16	0.165	0.5 %
	Channel 2	frising	0.34	0.339	0.5 %
	2	$f_{falling}$	0.49	0.5	1 %
	Channel 3	frising	0.65	0.663	1.3 %
		$f_{falling}$	0.77	0.76	1 %
	Channel 4	frising	0.89	0.892	0.2 %
		f _{falling}	1	1	0 %

TABLE 3.5. CHANNEL EDGE FREQUENCIES

a) Error vs. Complexity

The relation between error and number of multipliers for the CDM-FRM filter bank, DFTFB, tree-structured quadrature mirror filter bank (TQMFB) [96] and tree structure DFTFB (TDFTFB) [97], for different resolutions of filter banks, is plotted in Fig. 3.18. It can be observed that, the CDM-FRM filter bank requires fewer number of multipliers (and hence less computational complexity) than the other methods for a given error.



Fig. 3.18. Percentage error vs. complexity comparison.

b) Error vs. Detection Time

The dependence of performance (error and time) on different values of D_{II} for the CDM-FRM filter bank and the DFTFB is shown in Fig. 3.19. The number of samples at the input of the energy detector is kept constant. It can be observed that the proposed method requires slightly longer detection time than the DFTFB. This is because the CDM-FRM filter bank has higher group delay than the DFTFB as shown in Table 3.3. However, due to the reconfigurable architecture of the CDM-FRM filter bank, error decreases with time as $P_{D.M}$ is available for more values of D_{II} as shown in Fig. 3.19. On the contrary, the error is fixed in the case of DFTFB because it is incapable of providing multiple subband bandwidths and it needs to be re-designed to further reduce the error.



Fig. 3.19. Percentage error vs. detection time comparison.

The CDM-FRM filter bank provides low complexity alternative to DFTFB when input signal spectrum is varying slowly. However, in scenarios where input signal spectrum is varying dynamically, reconfigurable filter banks with low group delay discussed later in Chapter 5 are necessary.

3.7 Summary

In this chapter, a new low complexity reconfigurable filter bank architecture based on the CDM and the FRM (termed as CDM-FRM filter bank) is presented. In the CDM-FRM filter bank, the subband bandwidth is changed by changing the decimation factor D_{II} and it provides uniform as well as non-uniform bandwidth subbands along with fractional control over the bandwidth and the center frequency of subbands. Two different modes of

operation of the CDM-FRM filter bank depending on the values of D_{II} are explained. The gate count and implementation results indicate that the CDM-FRM filter bank offers substantial savings in area and power consumption compared to other filter banks. The functionality of the CDM-FRM filter bank is validated for different input signal spectrum scenario and smaller mean square error values between the samples of the extracted channels and the respective samples of input signal indicates good channelization performance. The application of the CDM-FRM filter bank for accurately detecting the frequency edges of multiple channels in wideband input signal for multi-standard military communication receivers is presented. Simulation results shows that the CDM-FRM filter bank based edge detection approach is computationally more efficient than other edge detection approaches for a given error in channel edge frequency.

The CDM-FRM filter bank uses CDM-VDF in the first stage. Since CDM has an inherent drawback of coarse control over the cut-off frequency, the CDM-FRM filter bank cannot provide an unabridged control over subband bandwidth as well as their center frequencies. To provide an unabridged control over subband bandwidth as well as their center frequencies, a low complexity lowpass VDF which can provide an unabridged control over the cut-off frequency range is required. In the next chapters, the design of such VDFs and reconfigurable filter bank architectures using these VDFs are presented.

Chapter 4 Low Complexity Reconfigurable Fast Filter Bank (RFFB)

The motivation behind the work presented in this chapter is to design a low complexity reconfigurable filter bank with an unabridged control over the bandwidth as well as the center frequency of subbands. The coefficient decimation method (CDM) and frequency response masking (FRM) based filter bank (termed as CDM-FRM filter bank) presented in Chapter 3 provides coarse control over the subband bandwidth and the center frequency. In order to improve it further to achieve an unabridged control over subband bandwidth and their center frequency, the CDM based variable digital filter (VDF) should be replaced with a lowpass VDF that provides an unabridged control over the cut-off frequency on a wide frequency range. In this chapter, a brief literature review of various VDFs is presented complementing the comprehensive literature review in Section 2.4 of Chapter 2 followed by two key contributions on the design of low complexity VDFs. The latter part of this chapter presents a new low complexity reconfigurable fast filter bank (RFFB) architecture and comparison of its gate count complexity with other reconfigurable filter banks in literature.

4.1 Review of Variable Digital Filters (VDFs)

A VDF is a filter which allows on-the-fly control of one or more frequency specifications such as cut-off frequency, f_c , phase delay, group delay etc. via fewer number of input parameters with minimum overhead on complexity [36, 51]. A VDF can be designed either using finite impulse response (FIR) filters [24-33, 36-50] or infinite impulse response (IIR) filters [51, 67-69]. For a linear phase filter bank, FIR VDFs are preferred over IIR counterparts because the former can have exact linear phase with guaranteed stability and low coefficient sensitivity.

A number of linear phase VDFs are available in literature and reviewed in detail in Chapter 2. They include programmable filters [74-79], frequency transformation based VDFs [36-40], spectral parameter approximation (SPA) based VDFs [41-50], CDM-VDFs [24, 30] and FRM-VDFs [23, 31, 33, 86]. To design a reconfigurable filter bank, the requirement on lowpass VDF is that it should provide an unabridged control over f_c on a wide frequency range with low complexity and small reconfiguration delay. The programmable filters [74-79] cannot provide an efficient solution due to the large memory and reconfiguration time required. CDM-VDFs [24, 30] and FRM-VDFs [23, 31, 33, 86] provide only coarse control over f_c as decimation and interpolation factors are limited to positive integer values. SPA-VDFs [41-50] and frequency transformation based VDFs [36-40] provide an unabridged control over f_c but they are preferred only when f_c needs to be varied on a smaller frequency range due to huge area complexity and power consumption requirements for wider frequency ranges. Thus, most of the existing linear phase VDFs do not satisfy the requirement of wide f_c range for the design of a reconfigurable filter bank. Furthermore, the analysis on non-linear phase allpass transformation (APT) based VDFs [51] and CDM-VDFs [24, 30] in Chapter 2 give insinuation that unabridged control over the cut-off frequency could be achieved if unit delays in an FIR filter are replaced with fractional delays (FD). Based on the study on various FD structures, a new approach of linear phase VDF design using Lagrange interpolation based modified Farrow FD filters (termed as MF-VDF) is proposed which is presented in the next section.

4.2 Modified Farrow Structure Based Variable Digital Filter (MF-VDF)

The design of VDFs is based on the basic principle that f_c and transition bandwidth (TBW) of an FIR filter can be changed by modifying its impulse response. The f_c of an FIR filter is obtained from the impulse response sample that has the largest magnitude value which in turn depends on the filter coefficients values [98]. Also, the TBW of an FIR filter depends on the length of an FIR filter (i.e. length of an impulse response) which in turn depends on the total number of delays in an FIR filter [98]. The VDF structures in [41-50, 74-79] are based on modifying the filter coefficients or expressing the filter coefficients in some polynomial forms. However, if each delay of an FIR filter is replaced by the FD, the f_c and the TBW will change with the value of FD [51] similar to that of APT-VDFs. The proposed VDF, shown in Fig. 4.1, is obtained by replacing each unit delay of an N^{th} order transposed-direct form FIR filter, H(z), with the FIR FD structure which provides online control over the FD value D. The order and type of the FD



Fig. 4.1. Proposed fractional delay based variable digital filter (VDF).

structure, N_{fd} , decides the range of D which can be either { $(N_{fd} -1)$ to $(N_{fd} +1)$ } or { $(N_{fd} -1)/2$ to $(N_{fd} +1)/2$ } [35]. The change in D changes the length and amplitude of the impulse response of an FIR filter. This in turn results in the VDF whose filter coefficients are fixed while f_c and the TBW decrease as the value of D increases. Since FIR FD filters have linear phase unlike APT-VDFs, the proposed VDF retains the linear phase property which is essential for most of the communication and signal processing applications. In the next section, the mathematical equations relating the f_c and the TBW of the proposed VDF with the FD value D, is derived.

4.2.1 Relation Between Cut-off Frequency, Fractional Delay (FD) and Transition Bandwidth (TBW)

The delay, D, can be represented as a sum of integer and fractional part.

$$D = \lfloor D \rfloor + d \tag{4.1}$$

where [.] denotes the floor function and *d* is the value of the FD ($0 \le d < 1$). Consider the canonical implementation of N^{th} order fixed-coefficient lowpass filter (referred to as the prototype filter). Then, the order of prototype filter is equal to total number of unit delay elements in the filter. In the proposed VDF, each delay of the prototype filter is replaced with FIR FD filter of an appropriate order as shown in Fig. 4.1. Hence, the order of an FIR filter can be varied by varying *D*, i.e. *d* and the resulting filter order is termed as the 'effective order' of an FIR filter. Initially when D = 1 (i.e. d = 0), the effective order of an FIR filter is N_1 (where $N_1 = N$). When *D* is changed by varying *d*, the effective order of an FIR filter changes according to the equation,

$$N_D = [N_1, D] \tag{4.2}$$

where N_D is the effective order of an FIR filter corresponding to D. For the window design based fixed-coefficients FIR filter, the product of TBW_D and effective order of an FIR filter (N_D) is always constant [98].

$$N_D.TBW_D = C \tag{4.3}$$

where TBW_D is the TBW of the proposed VDF corresponding to D and constant C is calculated as,

$$C = N_1 \cdot TBW_1 \tag{4.4}$$

In [24, 30, 36], the prototype filter needs to be over-designed to meet the final required

▶ Page 100

specifications in order to compensate for the deterioration in the TBW and stopband ripple due to operations such as frequency transformation, CDM etc. From Eq. (4.2) and Eq. (4.3), it can be observed that as *D* increases, N_D increases and TBW_D decreases which means that $TBW_D \leq TBW_I$ i.e. there is no deterioration in the TBW. Since the filter coefficients in the proposed VDF are fixed and equal to that of prototype filter, the stopband ripple of the proposed VDF is same as that of prototype filter. Hence, such overdesign of the prototype filter is not required in the proposed VDF. Mathematically, if f_{cD} is the cut-off frequency corresponding to *D*, then

$$f_{cD} = \frac{f_c}{D} \tag{4.5}$$

From Eq. (4.5), it can be noted that f_{cD} decreases with the increase in D. To avoid multiband response, D should be less than 2. Also, when D is less than 1, $f_{cD} > f_c$ and $TBW_D > TBW$. Similar results can be obtained by incorporating the CDM [24] with the proposed VDF. Hence, the desired range of delay for the proposed VDF is $1 \le D < 2$. Next step is to select a computationally efficient FD structure which provides on-the-fly control over FD, $1 \le D < 2$.

4.2.2 Selection of Fractional Delay (FD) Structure

A number of FD filter designs such as Least squares based design, Maximally flat design, Equiripple design, multi-rate based design and FIR delay control based design are reported in literature [35]. In order to obtain the linear phase response, only FIR FD structures are taken into consideration for the design of the proposed VDF. The implementation complexity and the range of FD values, D, of the FIR FD structure depends on its order, N_{fd} . For $1 \le D < 2$, second order FD structure is required. The third or higher order FD structure will lead to multiband response as D > 2 and hence, cannot be used. Furthermore, the FIR FD structure must allow online tuning of the FD as opposed to the offline control where coefficients are updated every time the FD needs to be changed.

Lagrange interpolation (i.e. Maximally flat design) is the most commonly used technique to design an FIR filter approximating a given FD. This is because, Lagrange interpolation has the advantages of smooth magnitude response, easy to calculate filter coefficients, better response at low frequencies and preferable for applications where a lower order (\leq 3) FIR FD filter is needed [35]. The direct form implementation of Lagrange interpolation needs computationally intensive coefficient update when FD is changed. Hence, it is not suitable for the proposed VDF where FD must be changed in real time in order to vary f_c .

The Farrow structure proposed in [81] as an alternative technique for implementing the Lagrange interpolation has the advantages of using fixed-coefficient filters for a given order and real time control over the FD. However, the complexity of the Farrow structure grows with the square of the interpolation order. The design of the Farrow structure using Vandermonde matrix results in fewer number of multiplications than the direct from structure plus coefficient update, at the cost of extra adders [99]. Hence, the Farrow structure is computationally efficient than the direct form implementation of Lagrange

interpolation plus coefficient update overhead when frequent change in the FD is required. The complexity of the Farrow structure is further reduced in [99] and FD value D is replaced by its fractional part, d. The structure is called as modified Farrow structure [99].

Another computationally efficient structure for the Lagrange interpolation based on discrete time Taylor series expansion is proposed in [100]. The structure in [100] has linearly growing computational complexity with the interpolation order and less complex than the modified Farrow structure [99] for higher order, N_{fd} . Also, the structure in [100] has the advantage of real time order update. However, since the order of FIR FD filter, N_{fd} , is fixed for the proposed VDF, the advantage of order update of the structure in [100] is not significant in the context of the proposed VDF. Also, the multiplication complexity of the modified Farrow structure [99] and the structure in [100] for second order FD filter is same. Therefore, both these structures are equivalent.

The design of the proposed VDF using modified Farrow structure is presented in this thesis and it is termed as modified Farrow structure based VDF (MF-VDF). The modified second order Farrow structure [99], as shown in Fig. 4.2(a), requires only two multipliers shown as d because the multiplication with 0.5 can be replaced with hardwired shift operation which incurs negligible hardware cost. The MF-VDF structure, shown in Fig. 4.2 (b), is obtained by replacing each unit delay of a transposed-direct form FIR filter with the modified Farrow structure in Fig. 4.2 (a).





Fig. 4.2. (a) Second order modified Farrow structure of Lagrange Interpolation [99], (b) Proposed MF-VDF.

4.2.3 Design Example

In this example, a linear phase lowpass VDF with tunable f_{cD} is designed. In the conventional VDF design, first step is to set the lower and upper cut-off frequencies i.e. f_{cD1} and f_{cD2} . However, in the MF-VDF, either f_{cD1} or f_{cD2} can be set and the other can be controlled by maximum value of D i.e. D_{max} , as shown in Eq. (4.5). Note that all the

frequency edges mentioned here are normalized with respect to half the sampling frequency.

Let the desired f_{cD2} , TBW, passband and stopband ripple be 0.07, 0.02, 0.05 dB and -57 dB respectively. For the desired specifications, a prototype filter of order 300 is designed with the cut-off frequency, TBW, passband and stopband ripple specifications of 0.07, 0.02, 0.05 dB and -57 dB respectively. Fig. 4.3 (a) shows the variable frequency responses of the MF-VDF as f_{cD} varies between 0.035 and 0.07. Note that the cropped version of frequency axis up to normalized frequency of 0.1π is shown. Though the frequency responses in Fig. 4.3 (a) are discrete due to finite resolution of *D*, the MF-VDF provides an unabridged control over f_{cD} by selecting the appropriate value of *D*. The stopband attenuation of the MF-VDF is fixed and equal to that of prototype filter. The phase is linear in the passband as indicated by flat phase delay in Fig. 4.3 (b).

4.2.4 Conclusion

A new MF-VDF using second order modified Farrow structure of Lagrange interpolation is proposed. In most of the VDF structures [36-50], the TBW of the VDF is equal to or greater than the TBW of the prototype filter. To the best of our knowledge, the proposed MF-VDF is the first one where the TBW of the VDF is narrower than the TBW of the prototype filter. Also, Eq. (4.5) indicates that the MF-VDF along with the CDM would provide fine control over the cut-off frequency on wide frequency range provided that FIR FD structure has flat magnitude and phase/group delay response. However, all existing lower order FD structures have flat magnitude and phase/group delay responses

up to lower frequencies only [35, 99, 100]. Beyond this frequency range, magnitude and phase response of the FD structure start deviating from the desired values leading to magnitude and phase distortion. Hence, the MF-VDF, which employs second order FD structure, is suitable for applications where fine control over f_c on a lower frequency range is desired.



Fig. 4.3. (a) Variable cut-off frequency responses obtained using the MF-VDF,

(b) Phase delay responses of the MF-VDF.

▶ Page 106

In the next Section, a modification to VDFs designed using second order frequency transformation is proposed. It is shown that the proposed modified second order transformation based VDF (MFT-VDF) has wider range over which f_c can be varied compared to the original VDF in [40].

4.3 Frequency Transformation Based Variable Digital Filters

The first method to design a linear phase VDF using frequency transformation is proposed in [36] and further extended in [37-40]. The VDF in [36] is obtained by replacing sub-networks in the Taylor structure of a prototype filter by a sub-network which performs a first order frequency transformation of the original network. By changing the parameters of sub-networks, the cut-off frequency of VDFs can be changed. In [40], second order frequency transformations are used and VDFs have sharper TBW characteristics and reduced cut-off frequency range for the same multiplication complexity and same number of variable parameters compared to VDFs in [36]. A detailed review of frequency transformation based VDF has been presented in Chapter 2. Here, second order frequency transformation based VDFs are reviewed in brief.

Consider a causal linear phase FIR filter, H(z), of order 2N with symmetric coefficients implemented in Taylor form which will be referred to as prototype filter. The transfer function of the second order frequency transformation based VDF, $H_2(Z)$, is given as,

$$H_2(Z) = \sum_{n=0}^{N} a_n Z^{-2(N-n)} \underbrace{\left[A_0 Z^{-2} + A_1 Z^{-1} \left(\frac{1+Z^{-2}}{2} \right) + A_2 \left(\frac{1+Z^{-2}}{2} \right)^2 \right]^n}_{D(Z)}$$
(4.6)

where coefficients a_n are related to the impulse response coefficients h_n of the prototype filter, through the Chebyshev polynomials [36]. The second order frequency transformation is performed using D(Z) where A_0 , A_1 , A_2 are the transformation coefficients which control the relationship between the prototype and transformed frequency responses [40]. Let the cut-off frequencies of the prototype and transformed filters be ω_c and Ω_c respectively. From D(Z), the Ω_c and the cut-off slope (i.e. TBW) are given by [40],

$$\Omega_c = \cos^{-1} \left\{ \frac{\left\{ -A_1 \pm \left[A_1^2 - 4A_2(A_0 - \cos \omega_c) \right]^{1/2} \right\}}{2A_2} \right\}$$
(4.7)

$$TBW = \frac{A_1 \sin \Omega_c + A_2 \sin 2\Omega_c}{\sin \omega_c} \tag{4.8}$$

where

$$\cos \omega = \frac{z + z^{-1}}{2} | z = e^{j\omega}$$
 and $\cos \Omega = \frac{Z + Z^{-1}}{2} | Z = e^{j\Omega}$

if the following constraints are met [40],

$$A_0 + A_1 + A_2 = 1, \qquad 0 \le A_1 \le 1$$

$$A_1^2 - 4A_2(1 - A_1 - A_2 - \cos \omega_c) \ge 0$$
(4.9)

The implementation of $H_2(Z)$ is shown in Fig. 4.4 (a) [36] where second order frequency transformation is realized through D(Z) shown in Fig. 4.4 (b). The coefficients $a_0, a_1...a_n$ are fixed and hence can be hardwired. The cut-off frequency and the TBW of $H_2(Z)$ are controlled through the parameters A_0 , A_1 and A_2 . In [40], A_1 is set to unity in



Fig. 4.4. (a) Second order frequency transformation based VDF, $H_2(Z)$, (b) Second order frequency transformation, D(Z).

order to reduce the number of multipliers and number of variable parameters. However, by restricting A_1 to unity, the range over which the cut-off frequency can be varied is limited to approximately 12.5% of the sampling frequency through empirical observations. However, Eq. (4.7) and Eq. (4.9) indicate that all the three parameters A_0 , A_1 and A_2 should be adjustable to have wider range of cut-off frequency. In the proposed MFT-VDF, A_1 is fixed to sum of reciprocal of power-of-two values between 0 and 1 instead of unity. Therefore, multiplication with A_1 can be done using hardwired shifts which incurs negligible hardware cost. By not restricting the value of A_1 to unity, the MFT-VDF allows a much wider range of cut-off frequencies. Next, the efficacy of the

MFT-VDF in the design of VDF with variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) responses and the reconfigurable fast filter bank (RFFB) is presented in the Section 4.4 and Section 4.5 respectively.

4.4 Modified Frequency Transformation Based Variable Digital Filter (MFT-VDF)

A digital filter with variable LP, HP, BP and BS responses are useful in communication applications such as serial channelization, serial two-stage spectrum sensing etc. The literature review of various VDFs presented in Chapter 2 indicates that most of the existing VDFs need to update their filter coefficients or employ distinct structures to provide different types of responses. In this section, application of the MFT-VDF to design linear phase fixed-coefficient VDF which provides variable LP, HP, BP and BS responses using the fixed architecture is presented.

4.4.1 Architecture of the MFT-VDF

The architecture of the MFT-VDF which provides variable LP, HP, BP and BS responses is shown in Fig. 4.5. It is obtained from Fig. 4.4 with two extra outputs and an output logic unit (OLU). The coefficients of lowpass prototype filter, a_0 , $a_1...a_n$, are fixed and hence can be hardwired. First input to the OLU, $y_1(n)$, is the LP response and the cut-off frequency of $y_1(n)$ can be controlled via input A_2 . Second input to the OLU, $y_2(n)$, is the BP response obtained from the prototype filter using the CDM-I with $D_I = 2$ and third input, $y_c(n)$, is a delayed version of input signal, x(n), such that group delay of all signals



Fig. 4.5. Architecture of the MFT-VDF.

at the input of the OLU is equal. The OLU consists of three multiplexers (one for each input, $y_1(n)$, $y_2(n)$ and $y_c(n)$) followed by two adder/subtractor blocks. The *Sel* signal decides the type of the output response, y(n). The variable frequency responses are obtained as follows:-

$$LP \rightarrow y(n) \text{ or } [y(n) + y_c(n) - y_1(n)]$$
$$HP \rightarrow [y_c(n) - y(n)] \text{ or } [y_1(n) - y(n)]$$
$$BP \rightarrow [y_c(n) - y_1(n)]$$
$$BS \rightarrow y_1(n)$$

4.4.2 Design Example

The performance of the MFT-VDF is evaluated in this section with the help of a suitable design example. In this design example, the cut-off frequency range of the VDF in [40] and the MFT-VDF is compared for a prototype filter with the cut-off frequency, f_c , and the TBW of 0.295 and 0.07 respectively. All the frequency edges mentioned here are

normalized with respect to half the sampling frequency. Let the desired passband and stopband ripple specifications be 0.06 dB and -50 dB respectively. The CDM-I has an inherent disadvantage of deterioration of the stopband attenuation and the TBW. Hence, the prototype filter needs to be over-designed. Thus, the order of the prototype filter for the MFT-VDF is 88 (=2N) compared to 80 for the VDF in [40].

For the lowpass VDF, the range of cut-off frequencies in the MFT-VDF and the VDF in [40] for a given prototype filter are shown in Fig. 4.6. The largest cut-off frequency range obtained using the MFT-VDF is 0.18 to 0.87 and corresponding A_1 and A_2 , calculated using Eq. (4.9), are 0.875 and 0.4375 $\leq A_2 \leq$ -0.9 respectively. On the other hand, the f_c of the VDF in [40] ($A_1 = 1$ and -0.5 $\leq A_2 \leq$ 0.5) has the limited range from 0.21 to 0.47. Thus, the range of f_c for the MFT-VDF is 173% wider than that of VDF in [40]. Similarly, variable HP responses at different cut-off frequencies can be obtained by complementing corresponding LP responses. The variable BP responses for center frequency of 0.63, obtained using the MFT-VDF, are shown in Fig. 4.7. Similarly, variable BP and BS responses at different center frequencies can be obtained.



▶ Page 112



Fig. 4.7. Variable bandpass responses obtained using the MFT-VDF.

4.4.3 Implementation Complexity Comparison

In this section, the complexity comparison in terms of total number of gate counts is presented. A 16x16 bit multiplier, a 2:1 multiplexer and 32 bit adder were synthesized on a TSMC 0.18µm process. The Synopsys Design Compiler was used to estimate the cell area. The area in terms of gate count, as shown in Table 4.1, was obtained by normalizing the above area values by the cell area of a two input NAND gate from the same library.

TABLE 4.1. GATE COUNT	COMPLEXITY	COMPARISON OF	MFT-VDF WITH	OTHER VDFS
-----------------------	------------	---------------	--------------	------------

VDFs No. of	MFT-VDF	MFT-VDF (<i>A</i> ₁ = 0.875)	VDF in [40] $0.16 \le f_{pass} \le 0.83$	VDF in [48]
Multipliers	133	89	162	196
Adders	378	422	640	172
Multiplexers	2	1	0	0
Total gate Count	311603	247193	420040	372072

For the design example discussed in Section 4.4.2 and for the range of f_c from 0.16 to 0.83, the MFT-VDF (with $A_1 = 0.875$ and hence multiplication with A_1 is replaced with hardwired shifts) offers a total gate count reductions of 33% and 41% over the VDF in [48] and [40] respectively. For the MFT-VDF and the VDF in [40], TBW is not fixed over the entire frequency range and it varies from 0.04 to 0.12. Hence, for a fair comparison, the VDF in [48] is designed with the TBW of 0.12. Even when multiplication with A_1 is done using general multipliers, the complexity of the MFT-VDF is significantly less than other VDFs. Moreover, other VDFs need to update filter coefficients or filter architecture to obtain BP and BS responses.

4.5 Proposed Reconfigurable Fast Filter Bank (RFFB)

The fast filter bank (FFB) is a low complexity filter bank, proposed as an alternative to the discrete Fourier transform filter bank (DFTFB) [22]. The FFB follows a tree structure and is suitable for filter banks requiring sharp TBWs. However, the FFB in [22] has the same drawbacks as that of the DFTFB, i.e., the inability to provide non-uniform bandwidth subbands and the constraint of fixed center frequency for each subband. Further extensions and improvements of the FFB have been proposed in [26, 32]. In particular, a multi-resolution FFB that is capable of adjusting subband bandwidths by changing the filter bank resolution without the need of hardware re-implementation is proposed in [26]. However, all the existing FFBs [22, 26, 32] fail to provide an unabridged control over the bandwidth as well as the center frequency of subbands. The aim of the proposed RFFB presented in this section is to provide an unabridged control over the bandwidth and the center frequency of the subbands over a desired range. Let the design specifications of the RFFB with 2*M* subbands are as follows: Minimum and maximum subband bandwidth are BW_{min} and BW_{max} respectively, TBW is TBW_d , passband ripple is δ_p , stopband ripple is δ_s . The structure of the proposed *k*-stage RFFB ($k = \log_2(2M)$) is shown in Fig. 4.8 where k = 4. The RFFB consists of the MFT-VDF in the first stage replacing the fixed-coefficient filter in uniform FFB [22]. Also, the fixedcoefficient sub-filters in the remaining (k - 1) stages of the RFFB have narrow TBWs and hence higher order than the sub-filters of uniform FFB in [22]. The RFFB design is described in detail below.



Fig. 4.8. Proposed reconfigurable fast filter bank (RFFB).

4.5.1 First Stage – Variable Digital filter

The lowpass VDF in the first stage of the RFFB is the MFT-VDF with transfer function $H_2(Z)$ in the form given by Eq. (4.6). The range over which the cut-off frequency

of $H_2(Z)$ can be varied is controlled by parameters A_1 and A_2 while the order of the prototype filter of $H_2(Z)$ depends on the desired TBW, passband and stopband ripple specifications. The D(Z) in Eq. (4.6) is given by,

$$D(Z) = A_0 Z^{-2} + A_1 Z^{-1} \left(\frac{1+Z^{-2}}{2}\right) + A_2 \left(\frac{1+Z^{-2}}{2}\right)^2$$
(4.10)

From the constraints given by Eq. (4.9), substituting $A_0 = 1 - A_1 - A_2$, into Eq. (4.10) and simplifying, Eq. (4.10) can be re-written as

$$D(Z) = A_1 \left[\left(\frac{Z^{-1} + Z^{-3}}{2} \right) - Z^{-2} \right] + Z^{-2} - A_2 \left[Z^{-2} - \left(\frac{1 + Z^{-2}}{2} \right)^2 \right]$$
(4.11)

In this way, only two multipliers are needed instead of three to implement D(Z). In [40], A_I is fixed to unity. For the RFFB, the restriction that $A_I = 1$ needs to be relaxed so that the $H_2(Z)$ allows a much wider range of the cut-off frequencies. The design steps for the first stage of the RFFB are:

- 1) Based on desired filter bank specifications, the lower and upper cut-off frequencies of the $H_2(Z)$, f_{c1} and f_{c2} , are given as $\left(\frac{M}{2} \cdot BW_{min}\right)$ and $\left(\frac{M}{2} \cdot BW_{max}\right)$ respectively.
- 2) For a desired range from $\Omega_{c1} = (2\pi f_{c1})$ to $\Omega_{c2} = (2\pi f_{c2})$, corresponding value of A_1 and range of A_2 are calculated using Eq. (4.7) and Eq. (4.9). This is an iterative procedure where for a given A_1 ($0 \le A_1 \le 1$) and ω_c , corresponding range of A_2 and Ω_c is obtained

using Eq. (4.9) and Eq. (4.7) respectively. Note that A_1 is fixed and restricted to sum of reciprocals of power-of-two values between 0 and 1 to keep the multiplier complexity same as [40].

- 3) The worst case passband and stopband ripple specifications of the prototype filter of $H_2(Z)$ are equal to δ_p and δ_s respectively.
- 4) Since the *TBW* of the $H_2(Z)$ is not constant over the frequency range from f_{c1} to f_{c2} as shown in Eq. (4.8), the *TBW*₀ of the prototype filter of $H_2(Z)$ is chosen such that the maximum *TBW* over the range f_{c1} to f_{c2} is equal to or narrower than $M \cdot TBW_d$.
- 5) Based on these parameters, $H_2(Z)$ is designed and interpolated by factor *M* to get the multi-band original (O_1) and complementary (C_1) responses.

4.5.2 Remaining (k-1) Stages – Fixed-Coefficient Sub-filters

The remaining (*k*-1) stages of the RFFB consist of fixed-coefficient FIR sub-filters, $H_{ij}(z)$, where $1 \le i \le (k-1)$ and $0 < j \le (2^i-1)$, arranged in a tree-structure similar to the FFB [22] as shown in Fig. 4.8. The design steps for remaining stages are:

- The (k-1) sub-filters, H_{ij}(z), 1 ≤ i ≤ (k-1) and j = 0 are fixed-coefficients even order lowpass filters which shall be known as sub-prototype filters. The cut-off frequency of all these sub-prototype filters is fixed and equal to 0.5 in the normalized frequency scale. The δ_p and δ_s of the filter bank and all sub-prototype filters are kept same.
- 2) The transition bandwidth TBW_i of the sub-prototype filter $H_{i0}(z)$, $1 \le i \le (k-1)$ is not same as that in FFB and is given by Eq. (4.12).

$$TBW_i = 1 - \left(f_{c2} + \frac{TBW_d}{2}\right)2^{(1-i)}$$
(4.12)

where f_{c2} is maximum cut-off frequency of $H_2(Z)$.

- 3) Based on these parameters, $H_{i0}(Z)$ are designed and then interpolated by the factor $\left(\frac{M}{2^{i}}\right)$ where $1 \le i \le (k-1)$.
- 4) The remaining sub-filters, $H_{ij}(z)$ where $1 \le i \le (k-1)$ and $1 \le j \le (2^i-1)$, are obtained by modulating the corresponding interpolated sub-prototype filters, $H_{i0}\left(z^{\binom{M}{2^i}}\right)$ [22].

Consider the illustrative lowpass frequency responses similar to that of $H_2(Z)$ as shown in Fig. 4.9 (a). When the $H_2(Z)$ is interpolated by M, the multi-band responses O_1 and C_1 with the TBW smaller by a factor of M are obtained as shown in Fig. 4.9 (b) and (c) respectively. All subbands are individually extracted using the sub-filters in remaining (k-1) stages. When the cut-off frequency of $H_2(Z)$ is $f_{c1} \leq f_c \leq f_{c2}$, all subbands in the original response, O_1 , and complementary response, C_1 , have bandwidth BW_{o1} and BW_{c1} respectively where



Fig. 4.9. Illustrative frequency responses of the first stage (a) Response of the MFT-VDF,(b) Original response, O₁, (c) Complementary response, C₁.
.....

$$BW_{o1} = \frac{2}{M} f_c$$
 (4.13)

$$BW_{c1} = \frac{2}{M}(1 - f_c) \tag{4.14}$$

Note that $BW_{ol} = BW_{cl}$ only when $f_c = 0.5$ i.e. uniform FFB case. When $f_c = f_{c2}$, $BW_{ol} = BW_{max}$ and $BW_{cl} = BW_{min}$. Similarly, when $f_c = f_{c1}$, $BW_{ol} = BW_{min}$ and $BW_{cl} = BW_{max}$. In this way, by controlling the f_c of $H_2(Z)$ using A_2 , an unabridged control over the subband bandwidth from BW_{min} to BW_{max} is achieved. Furthermore, by combining adjacent subbands and varying A_2 , the RFFB provides fine control over the center frequency of subbands having fixed bandwidth as explained in detail in Section 4.5.3 using suitable design example. Since $H_2(Z)$ in the first stage of RFFB is a linear phase VDF and all sub-filters in remaining (k-1) stages are linear phase FIR filters, the RFFB retains the linear phase property of the FFB in [22].

4.5.3 Design Example

Let the desired filter bank specifications are: $-BW_{min} = 0.06$, $BW_{max} = 0.2$, $TBW_d = 0.03$, $\delta_p = 0.1$ dB and $\delta_s = -50$ dB respectively. Then, for M = 8 and $k = \log_2(2M) = 4$, the required values of f_{c1} and f_{c2} are $0.24 \left(=\frac{8}{2} \cdot 0.06\right)$ and $0.8 \left(=\frac{8}{2} \cdot 0.2\right)$ respectively. Note that the chosen bandwidth range allows the subband bandwidth to be varied to the resolution of 32-subband uniform filter bank i.e. normalized subband bandwidth of 0.0625 using 16subband RFFB. For desired values of f_{c1} and f_{c2} , the value of A_1 is 0.4375, range of A_2 is from -0.2 to 1.5 and $\omega_c = 0.4\pi$. Note that multiplication with A_1 can be performed using only addition and shift operations. $H_2(Z)$ consists of the prototype filter of order 80 with $\omega_c = 0.4\pi$, $TBW_0 = 0.065$, $\delta_p = 0.1$ dB and $\delta_s = -50$ dB respectively. The order of the subfilters $H_{10}(Z)$, $H_{20}(Z)$ and $H_{30}(Z)$ with the cut-off frequency of 0.5, TBWs obtained using Eq. (4.12), maximum passband ripple of 0.1 dB and minimum stopband ripple of -50 dB are 40, 16 and 6 respectively.

The RFFB provides unabridged control over the subband bandwidth by varying A_2 from -0.2 to 1.5. Fig. 4.10 shows the frequency responses of subband 9 as the bandwidth varies between 0.06 and 0.2 with the center frequency of 0.125. Note that cropped version of frequency axis up to frequency of 0.5 is shown to have better view of adjacent bandpass responses. Though the responses shown in Fig. 4.10 are discrete, the RFFB provides unabridged control over the subband bandwidth from 0.06 and 0.2 by selecting appropriate value of A_2 . Similar responses can be obtained for all the 16 subbands having center frequencies $\pm l/M$ where $0 \le l \le M$. When $A_2 = 0.255$, all the subbands have uniform bandwidth as shown in Fig. 4.11, similar to uniform FFB [22].



Fig. 4.10. Variable bandwidth responses for subband 9 obtained using the RFFB.



Fig. 4.11. Uniform bandwidth responses using the RFFB.

The RFFB also provides high resolution control over the center frequency by combining adjacent subbands. For example, consider the subband, S_{9-10} , obtained by combining subbands 9, 10. By varying A_2 , the center frequency of S_{9-10} can be set anywhere from 0.15 to 0.22, as shown in Fig. 4.12 using different colors. Note that the bandwidth of S_{9-10} is fixed to 0.26 (= $BW_{min} + BW_{max}$). At the same time, adjacent



Fig. 4.12. Variable center frequency responses using the RFFB.

subbands S_{7-8} and S_{11-12} , each of bandwidth 0.26 have center frequency 0.26 lower and higher respectively compared to that of S_{9-10} . This makes the RFFB useful for the channelization and spectrum sensing scenario where the channel bandwidth is fixed but their locations may vary dynamically.

4.5.4 Implementation Complexity

The implementation complexity of the RFFB shall now be compared with other nonuniform filter banks in terms of total gate count for the design example considered in Section 4.5.3. A 16x16 bit multiplier, a 2:1 multiplexer, 16 bits of memory and 32 bit adder were synthesized on a TSMC 0.18 μ m process. The Synopsys Design Compiler was used to estimate the cell area. The area in terms of gate count is obtained by normalizing the cell area values by that of a two input NAND gate from the same library. The total gate count in Table 4.2 is the sum of gate counts of all the components. The "±x" values in Table 4.2 indicate the percentage increase of total gate count in respective filter banks when compared with the RFFB.

The CDM-DFTFB [25], consisting of the prototype filter of order 1000 ($f_c = 0.0225$, TBW= 0.003, the CDM factor range of 5 to 10) followed by 16-point fast Fourier transform (FFT), has a gate count 99% higher than the RFFB. The orders of filters in 4 stages of uniform FFB [22] are 36, 16, 10 and 6 respectively. In uniform FFB [22], $f_{c2} = f_{c2} = 0.5$ which is always smaller than f_{c2} in the RFFB. It can be observed from Eq. (4.12) that the *TBW_i* of all sub-filters in uniform FFB [22] are wider compared to those in RFFB. Thus, the order of the all sub-filters and hence corresponding number of multipliers, adders

	CDM-	Uniform	Reconfigu			
	DFTFB		Programmable	VDF in	SPA-VDF	RFFB
No. of	[25]	ГГ D [22]	filter [79]	[40]	[48]	
Multipliers	461	93	129	327	371	191
Multiplexers	429	0	0	26	0	0
Adders	492	171	243	406	719	526
Words of	0	0	> 1000	0	0	0
memory						
Delay in samples	500	189	243	499	323	739
Total gate count	863315 (+99%)	187275 (-56%)	321075 (-26%)	615460 (+42%)	755375 (+74%)	423950

TABLE 4.2. GATE COUNT COMPLEXITY COMPARISON OF RFFB WITH OTHER FILTER BANKS

and total delay are higher in the RFFB than FFB [22] for a given TBW_d , δ_p and δ_s . Since the RFFB bank can be used as a uniform and non-uniform filter bank, its complexity is higher than uniform FFB [22] due to VDF instead of fixed filter in the first stage and higher order fixed-coefficient sub-filters in remaining (k -1) stages. The higher gate counts of RFFB compared to FFB can be considered as penalty paid to achieve unabridged control over subband bandwidth.

The RFFBs can also be designed using either one of the following VDFs in the first stage of the FFB: 1) Programmable filter [79] of order 36, 2) Two VDFs in [40] each of order 50, 3) The SPA-VDF [48] consisting of 9 sub-filters each of order 56. The remaining stages in all three approaches consist of $H_{10}(Z)$, $H_{20}(Z)$ and $H_{30}(Z)$ of order 40, 16 and 6 respectively. Note that all three approaches are based on proposed idea of employing VDF in the first stage of FFB. Although the performances of all these filter

banks are identical, the RFFB based on VDFs in [40] and [48] require higher gate counts of 42% and 74% respectively compared to the RFFB using proposed MFT-VDF. Though the gate count requirement of the programmable filter based RFFB [79] is 26% less than the proposed MFT-VDF based RFFB, the former requires changes to the filter coefficients whenever the subband bandwidth needs to be changed. This involves huge amount of memory to store filter coefficients and incurs large reconfiguration delay compared to the proposed MFT-VDF based RFFB. The drawback of the RFFB is higher group delay compared to other approaches.

4.6 Summary

In this chapter, a new design of VDF using second order modified Farrow structure of Lagrange interpolation (MF-VDF) is presented. To the best of knowledge, the MF-VDF is the first linear phase VDF where the TBW of the responses is narrower than the TBW of prototype filter and it provides an unabridged control over the cut-off frequency on either side of the cut-off frequency of the prototype filter. Due to deterioration of magnitude response and phase or group delay response of the FIR FD structure at higher frequencies [35], the MF-VDF is suitable for applications where fine control over f_c on a lower frequency range is desired. Then, the modified VDF based on second order frequency transformation (MFT-VDF) is presented. The MFT-VDF has wider range over which f_c can be varied when compared to original VDF. The MFT-VDF when combined with the CDM provides variable LP, HP, BP and BS responses from a fixed-coefficient prototype filter without the need of hardware re-implementation. This makes the MFT-

VDF suitable for communication applications such as serial channelization, serial twostage spectrum sensing etc.

The proposed RFFB using the MFT-VDF is presented at the latter part of chapter. The RFFB allows an unabridged control over the bandwidth and the center frequency of subbands over the desired range without the need of hardware re-implementation. The implementation results showed that the methods in [25], [40] and [41] requires 135%, 45% and 78% higher gate counts respectively when compared with the RFFB. The possible applications of the RFFB includes area and power efficient two-stage spectrum sensing as well as channelization operation involving channels of distinct bandwidths corresponding to multiple communication standards. For example, in two-stage spectrum sensing, the advanced sensing stage dominates the area and power requirements when compared to the basic sensing stage. Here, the RFFB could be used to minimize dynamic power consumption by reducing the rate of activation of the advanced sensing stage. In RFFB, when adjacent subbands are combined, then bandwidth of all subbands is equal and by varying A_2 , the center frequency of subbands can be varied. This unique property makes RFFB useful for the channelization and spectrum sensing scenario where channel bandwidth is fixed but their locations may vary dynamically.

The proposed MFT-VDF has limited cut-off frequency range in case of variable LP and HP responses for a given prototype filter. Similarly, in case of BP and BS responses, there is upper and lower limit on the bandwidth of the response for a given prototype filter. For example, in the design example discussed in Section 4.4.3, to obtain the LP and HP

response with f_c of 0.95 or to obtain BP and BS response with bandwidth of 0.1, the prototype filter coefficients need to be updated in the MFT-VDF. Furthermore, most of the existing filter banks [7, 20-22, 25, 26, 32, 91] as well as the CDM-FRM filter bank and the RFFB cannot provide independent and individual control over the bandwidth and the center frequency of subbands. This is because, the subband bandwidth of all the subbands changes simultaneously when the cut-off frequency of the prototype filter is changed. In the next chapter, low complexity and reduced delay VDF architectures which provides variable LP, HP, BP and BS responses anywhere over the entire normalized frequency scale are presented. The proposed VDF is then extended to the design of a new low complexity reconfigurable filter bank which provides independent and individual control over the bandwidth as well as center frequency of subbands.

Chapter 5 Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

In existing modulated filter banks [7, 20, 21, 25], interpolation based filter banks [22, 26, 32, 91] including the proposed CDM-FRM filter bank and the RFFB, the bandwidth of all subbands depends on a single parameter i.e. cut-off frequency of the prototype filter which means that when the cut-off frequency of the prototype filter is changed, the bandwidth of all subbands changes simultaneously. Thus, independent and individual control over the bandwidth and the center frequency of subbands is difficult to achieve in these filter banks. Furthermore, the subband bandwidth of these filter banks should be equal to the bandwidth of narrowest channel in the wideband input signal. This is to insure that multiple channels corresponding to different communication standards do not fall in the same subband of the filter bank. In multi-standard wireless communication receivers (MWCRs), the wideband input signal consists of channels of distinct communication standard whose bandwidths may vary over a wide range as shown in Table 1.1 of Chapter 1. As a result, the minimum required resolution of the filter bank is very high compared to the number of channels concurrently processed by subsequent DSP algorithms. The higher the resolution of the filter bank, the higher is the area complexity, power consumption and delay. In order to reduce the complexity and the

group delay of the filter bank, its resolution must be equal to the number of channels concurrently handled by the subsequent DSP algorithms and the resolution should be independent of the channel bandwidth. To achieve this, a filter bank which provides independent and individual control over the bandwidth and the center frequency of subbands is desired.

In this chapter, new low complexity variable digital filter (VDF) and reconfigurable filter bank based on recently proposed modified coefficient decimation method-I (MCDM-I) in [29] are presented. The proposed VDF provides variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) responses over entire normalized frequency scale. The reconfigurable filter bank designed using the proposed VDF provide independent and individual control over the bandwidth and the center frequency of subbands. The applications of the proposed architectures such as combined channelization and spectrum sensing for cognitive radios (CRs) and filter banks for digital hearing aids are presented in the latter part of the chapter.

5.1 Proposed Modified CDM Based Variable Digital Filter and Reconfigurable Filter Bank

In most of the VDF applications, desired frequency specifications such as cut-off frequency (f_c or ω_c) range, type of response etc. are specified and then the type of the VDF is decided based on the permissible implementation complexity, delay, linear or non-linear phase requirement etc. This approach works well when the range of f_c is

narrow and a specific response such as LP, HP, BP and BS is required. However, most of the existing VDFs are not computationally efficient when f_c needs to be varied over wide frequency range and all types of variable responses (i.e. LP, HP, BP and BS responses) are desired from a lowpass prototype filter. For such applications, an alternative low complexity VDF design based on the combination of lowpass prototype VDF that has narrow range of f_c (hence lower complexity) and the MCDM-I, is proposed in this chapter. The proposed VDF is then extended to the design of reconfigurable filter bank. In the next sub-section, the detail review of the MCDM-I is provided.

5.1.1 Modified Coefficient Decimation Method-I (MCDM-I)

The coefficient decimation methods (CDM-I and CDM-II) are widely used for the design of reconfigurable filters and filter banks for MWCRs [24, 25, 27-31]. Both the methods are reviewed in Chapter 2. In the CDM-I with decimation factor D_I , every D_I^{th} coefficient of the prototype filter is retained and the others are replaced with zeros. If $H(e^{j\omega})$ denotes the Fourier transform of the prototype filter, then the Fourier transform of the decimated prototype filter, $H_{D_I}(e^{j\omega})$, is given by [24],

$$H_{D_I}(e^{j\omega}) = \frac{1}{D_I} \sum_{k=0}^{D_I - 1} H\left(e^{i\left(\omega - \frac{2\pi k}{D_I}\right)}\right)$$
(5.1)

where D_I is limited to positive integer values. The $H_{D_I}(e^{j\omega})$ is a multi-band frequency response with subbands located at multiples of $\left(\frac{2\pi}{D_I}\right)$. The bandwidth and the TBW of all

Chapter 5 – Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

subbands in $H_{D_I}(e^{j\omega})$ are identical and equal to the passband width and the TBW of the prototype filter, $H(e^{j\omega})$, respectively. Recently, the CDM-I is extended where the sign of every alternate retained coefficients in the CDM-I operation is reversed. This is known as modified CDM-I (MCDM-I) [29]. For example, if { h_0 , h_1 , h_2 , h_3 , h_4, h_N } are coefficients of prototype filter, then coefficients after MCDM-I with $D_I = 1$ and $D_I = 2$ are { h_0 , $-h_1$, h_2 , $-h_3$, h_4, h_N } and { h_0 , 0, $-h_2$, 0, h_4, h_N } respectively. The Fourier transform of the decimated prototype filter, $H_{D_I}^m(e^{j\omega})$, is given by [29],

$$H_{D_{I}}^{m}(e^{j\omega}) = \frac{1}{D_{I}} \sum_{k=0}^{D_{I}-1} H\left(e^{i\left(\omega - \frac{\pi(2k+1)}{D_{I}}\right)}\right)$$
(5.2)

The multiband responses obtained using the MCDM-I are same as that obtained using the CDM-I except they are circularly shifted by frequency of $\left(\frac{\pi}{D_I}\right)$ on the normalized Nyquist band [29]. From Eq. (5.1) and Eq. (5.2), it can be observed that the MCDM-I provide multi-band responses with a center frequency resolution of $\left(\frac{\pi}{D_I}\right)$ compared to the resolution of $\left(\frac{2\pi}{D_I}\right)$ obtained using the CDM-I. For example, consider the prototype filter with cut-off frequency of ω_c as shown in Fig. 5.1 (a). The prototype filter response using the CDM-I with $D_I = 1$ is same as that of original response as shown in Fig. 5.1 (a). The HP and its complementary LP frequency responses obtained using the MCDM-I with $D_I =$ 1 are shown in Fig. 5.1 (b) in blue (solid line) and green (dashed line) colors respectively. The frequency responses obtained using the CDM-I and the MCDM-I for $D_I = 2$ are shown in Fig. 5.1 (c) and Fig. 5.1(d) respectively where prototype and its complementary Chapter 5 – Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

frequency responses are shown in blue (solid line) and green (dashed line) colors respectively.



Fig. 5.1 (a). Frequency response of lowpass prototype filter.



Fig. 5.1 (b). Original and complementary frequency responses using MCDM-I with $D_I = 1$.



Fig. 5.1 (c). Original and complementary frequency responses using CDM-I with $D_I = 2$.



Fig. 5.1 (d). Original and complementary frequency responses using MCDM-I with $D_I = 2$.

Consider the case where the CDM-I is used to obtain variable lowpass responses. From Fig. 5.1 (c), it can be observed that, to obtain lowpass responses with the cut-off frequency of ($\pi - \omega_c$), the CDM-I needs very narrow TBW (and hence higher order) masking filter, indicated in red color (dotted line), to mask higher frequency subband and $D_I = 2$. On the other hand, lowpass response with cut-off frequency of ($\pi - \omega_c$) is easily obtained using the MCDM-I with $D_I = 1$ without the need of masking filter. Note that for larger decimation factor, D_I , prototype filter needs to be over-designed to compensate the deterioration in stopband attenuation due to decimation operation. Furthermore, the MCDM-I with $D_I = 2$, provides additional lowpass responses (with cut-off frequencies of ($0.5\pi - \omega_c$) and ($0.5\pi + \omega_c$)) using wide TBW (and hence lower order) masking filter shown in Fig. 5.1 (d) in red color (dotted line). The CDM-I needs to update prototype filter coefficients to obtain lowpass responses with cut-off frequencies of ($0.5\pi - \omega_c$) and ($0.5\pi + \omega_c$).

Overall, when compared to the CDM-I, the MCDM-I has advantages such as lower order prototype filter, lower range of D_l , additional lowpass responses and lower order masking filters. The implementation results show that the MCDM-I provides substantial reduction in area complexity and power consumption over the CDM-I [29]. Though the MCDM-I improves the flexibility of the CDM-I, both methods fail to provide an unabridged control over the cut-off frequency due to integer decimation factors. The basic principle of the proposed VDF and reconfigurable filter bank design is discussed in the next sub-section.

5.1.2 Basic Principle

Consider the prototype filter with the cut-off frequency f_c (or ω_c). The MCDM-I with $D_I = 1, 2$ provides lowpass responses with cut-off frequencies of ω_c , $(\pi - \omega_c)$, $(0.5\pi + \omega_c)$ and $(0.5\pi - \omega_c)$ as shown in Fig. 5.1(a)-(d). The LP response with cut-off frequency of $(\pi - \omega_c)$ is obtained by complementing the HP response obtained using the MCDM-I with $D_I = 1$. The LP response with cut-off frequency of $(0.5\pi - \omega_c)$ is obtained by masking the higher frequency subband of multi-band response obtained using the MCDM-I with $D_I = 2$. Finally, the LP response with cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the LP response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ is obtained by combining the the response with the cut-off frequency of $(0.5\pi + \omega_c)$ with the complementary of the response obtained using the MCDM-I with $D_I = 2$.

Assume that the normalized Nyquist band is divided into four quarters of bandwidth 0.25π each i.e. $(0 - 0.25\pi)$, $(0.25\pi - 0.5\pi)$, $(0.5\pi - 0.75\pi)$ and $(0.75\pi - \pi)$. When N^{th} order prototype filter in the MCDM-I is replaced with N^{th} order prototype VDF, $H_a(z)$, that provides LP responses with an unabridged control over the cut-off frequency, ω_{cpa} , in second quarter i.e. $0.25\pi \le \omega_{cpa} \le 0.5\pi$ with fixed TBW of TBW_d , then LP responses with ω_c anywhere on normalized frequency range from $\left\{ \left(\frac{TBW_d}{2}\right)\pi \le \omega_c \le \left[1 - \left(\frac{TBW_d}{2}\right)\right] \right\}\pi$ can be obtained as follows:

1) The prototype VDF, $H_{\alpha}(z)$, provides variable LP responses in second quarter as shown in Fig. 5.2 (a) where α is the parameter which controls the cut-off frequency. The response in second quarter is represented using the notation $H_{\alpha02}^m(z)$ where the subscript '0' denotes $D_I = 0$ and the subscript '2' denotes second quarter.



Fig. 5.2. (a) Frequency response of lowpass prototype VDF, $H_{\alpha}(z)$, (b) Frequency response, $H_{\alpha 1}^{m}(z)$, obtained using MCDM-I with $D_{I} = 1$, (c) Complementary response, $H_{\alpha c1}^{m}(z)$, (d) Frequency response, $H_{\alpha 2}^{m}(z)$, obtained using MCDM-I with $D_{I} = 2$, (e) Complementary response, $H_{\alpha c2}^{m}(z)$, (f) Frequency response of masking filter, $H_{m}(z)$, (g) Frequency response of, $[H_{\alpha c2}^{m}(z)H_{m}(z)]$, (h) Frequency response of $[H_{\alpha c2}^{m}(z)H_{m}(z) + H_{\alpha 2}^{m}(z)]$.

Chapter 5 – Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

Using the MCDM-I with D_I=1, HP response, H^m_{α1}(z), with 0.5π ≤ ω_c ≤ 0.75π (third quarter) are obtained as shown in Fig. 5.2 (b). Then, by complementing, H^m_{α1}(z), LP response, H^m_{α13}(z) with 0.5π ≤ ω_c ≤ 0.75π (third quarter) are obtained as shown in Fig. 5.2 (c). Mathematically, above operations can be represented as

$$H_{\alpha 13}^{m}(e^{j\omega_{c}}) = 1 - H_{\alpha 1}^{m}(e^{i\omega_{c}}) = 1 - H_{\alpha}(e^{i(\omega_{cp\alpha} - \pi)})$$
(5.3)

where the subscript 'c' denotes complementary response.

3) Using the MCDM-I with $D_I = 2$ and fixed-coefficient masking filter, $H_m(z)$, LP responses with $\left(\frac{TBW_d}{2}\right)\pi \leq \omega_c \leq 0.25\pi$ (first quarter) are obtained. In this case, using the MCDM-I with $D_I = 2$, we have bandpass response, $H_{\alpha 2}^m(z)$, and its complementary bandstop response, $H_{\alpha c2}^m(z)$, as shown in Fig. 5.2 (d) and Fig. 5.2 (e) respectively. Then the higher frequency subband of $H_{\alpha c2}^m(z)$, is masked using N_m th order masking filter $H_m(z)$ whose response is shown in Fig. 5.2 (f). This results in LP responses, $H_{\alpha 21}^m(z)$, with $\omega_c = (0.5^*\pi - \omega_{cp\alpha})$ i.e. $\left(\frac{TBW_d}{2}\right)\pi \leq \omega_c \leq 0.25\pi$ as shown in Fig. 5.2 (g). Mathematically, above operations can be represented as

$$H^m_{\alpha 21}(e^{j\omega_c}) = H^m_{\alpha c2}(e^{i\omega_c})H_m(e^{i0.5\pi})$$
(5.4)

where

$$H^{m}_{\alpha c2}(e^{i\omega_{c}}) = \left\{ \left(e^{-i\omega_{cp\alpha}\left(\frac{N-1}{2}\right)} \right) - \left[\frac{1}{2} \sum_{k=0}^{1} H_{\alpha} \left(e^{i\left(\omega_{cp\alpha}-\frac{\pi(2k+1)}{2}\right)} \right) \right] \right\}$$

▶ Page 135

The cut-off frequency and the TBW of the masking filter $H_m(z)$ are 0.5 and $(0.5 - 2*TBW_d)$ respectively.

4) Finally, adding the bandpass response, $H_{\alpha 2}^m(z)$, to $H_{\alpha 21}^m(z)$, lowpass responses with $\omega_c = (0.5^*\pi + \omega_{cp\alpha})$ i.e. $0.75\pi \le \omega_c \le \left[1 - \left(\frac{TBW_d}{2}\right)\right]\pi$, can be obtained as shown in Fig. 2(h). Mathematically, above operations can be represented as

$$H^m_{\alpha 24}(e^{j\omega_c}) = H^m_{\alpha 21}(e^{j\omega_c}) + H^m_{\alpha 2}(e^{i\omega_c}) \left[e^{-i\omega_{cp\alpha}\left(\frac{N_m-1}{2}\right)} \right]$$
(5.5)

where

$$H^{m}_{\alpha 2}(e^{i\omega_{c}}) = \left\{ \left[\frac{1}{2} \sum_{k=0}^{1} H_{\alpha} \left(e^{i \left(\omega_{cp\alpha} - \frac{\pi(2k+1)}{2} \right)} \right) \right] \right\}$$

In the same way, HP responses with variable f_c can be obtained by complementing the corresponding LP responses. Furthermore, the BP response with rising and falling edge cut-off frequencies of f_{c1} and f_{c2} respectively is obtained by subtracting the LP response with cut-off frequency f_{c1} from another LP response with cut-off frequency f_{c2} . Likewise, the BS response with desired frequency specifications can also be obtained. The complexity of existing VDFs increases linearly with the cut-off frequency range. The proposed method overcomes this drawback by combining existing VDFs with smaller cut-off frequency range (and hence lower complexity) with the MCDM-I and offers wider cut-off frequency range.

The proposed method can be extended to the design of reconfigurable filter bank which provides independent and individual control over the bandwidth as well as the center

frequency of subbands. In case of *M*-subband filter bank, cut-off frequencies, f_{c1} , f_{c2} ... f_{cM-1} corresponding to falling frequency band edges of subbands are calculated. Then, individual LP responses with the cut-off frequencies, f_{c1} , f_{c2} f_{cM-1} are simultaneously obtained using the proposed VDF and parallel branches of α . For example, branch with α_1 , α_2 α_{cM-1} provides lowpass response with the cut-off frequency f_{c1} , f_{c2} f_{cM-1} respectively. Finally, by subtracting the LP response whose cut-off frequency is equal to the rising edge cut-off frequency of subband from the LP response whose cut-off frequency response of a 4-subband proposed filter bank is shown in Fig. 5.3 where three LP responses with cut-off frequency of three subbands are obtained as shown in Fig. 5.3 (a)-(c) respectively.



Fig. 5.3. Frequency response illustration of a 4-subband reconfigurable filter bank.

The advantages of the filter bank designed using proposed method are:

- 1) The bandwidth and the center frequency of each subband can be controlled independently by controlling the cut-off frequencies of corresponding LP responses using control parameters, $\alpha_1, \alpha_2, \dots, \alpha_{cM-1}$.
- 2) Since the proposed VDF provides an unabridged control over the cut-off frequency on entire normalized frequency range, the bandwidth as well as the center frequency of subbands are not limited to any specific range or set of discrete values.
- 3) The resolution of the proposed filter bank, *M*, depends on the number of LP responses and hence it is not limited to any range or discrete values unlike fast filter bank [22] where *M* is constrained to the power-of-two values.
- 4) Using *M*-subband filter bank architecture, the resolution of the filter bank can be changed anywhere from 1 to *M* by selecting the subset of LP responses. Thus, the proposed filter bank can be easily reconfigured to a desired resolution compared to interpolation and modulation based filter banks where complex and time consuming hardware reconfiguration and coefficient updates are needed to change resolution, *M*.
- 5) Since all the LP responses are obtained in parallel, total group delay of the filter bank is independent of the resolution of the filter bank and is equal to the total group delay of the prototype VDF.

5.1.3 Selection of Prototype Variable Digital Filter

The successful realization of the proposed VDF as well as filter bank and the overall implementation complexity essentially depends on the choice of the prototype VDF. A comprehensive literature review of various VDFs such as frequency response masking (FRM) based VDFs [23, 31, 33, 86], CDM-VDF [24, 29], frequency transformation based VDFs [36-40, 51, 67-69] and spectral parameter approximation (SPA) based VDFs [41-50] has been provided in the Section 2.4 of Chapter 2. Most of the VDFs are preferred when desired f_c range is narrow complementing the narrow cut-off frequency range (0.25π - 0.5π) requirement of the prototype VDF in the proposed method. However, for successful realization of the proposed method, the prototype VDF should satisfy following conditions:

- 1) The prototype VDF architecture should support MCDM-I.
- 2) Provide lowpass response with an unabridged control over ω_c from 0.25π to 0.5π .
- 3) Provide multiple lowpass responses, each with distinct f_c , at the minimum cost of multipliers and adders. This is a necessary requirement for obtaining BP and BS responses as well as designing low complexity reconfigurable filter bank.
- 4) The TBW of the VDF should be less than or equal to desired TBW specifications.
- 5) The group delay should be as low as possible.

▶ Page 139

The FRM-VDFs and the CDM-VDF can be realized with low complexity when coarse control over f_c on wide frequency range is desired. However, FRM-VDFs [23, 31, 33, 86] are not suitable for the proposed method because of two reasons. First, the FRM VDFs can provide only coarse control over f_c due to integer interpolation factor. Second, the multi-stage architecture of FRM-VDFs makes the MCDM-I difficult to integrate. In addition, the group delay of FRM-VDFs is very large. Similarly, the CDM-VDF [24] provides only coarse control over the cut-off frequency because of integer decimation factor and hence it is not considered for the proposed MCDM based method of VDF and filter bank design.

On the other hand, frequency transformation based VDFs [36-40, 51, 67-69] and SPA-VDFs [41-50] can be implemented with low complexity while providing an unabridged control over f_c on narrow frequency range. Frequency transformation based VDFs include VDFs designed using first order frequency transformation [36-39], second order frequency transformation [40], first order allpass transformation (APT) [51] and second order APT [51, 67-69]. The first and second order frequency transformation based VDFs are implemented using Taylor structure which makes them incompatible for integrating with the MCDM-I. The second order APT-VDFs provide LP to BP transformation and hence not considered for the proposed method. Thus, the search for lowpass prototype VDF narrows down to two VDFs namely, first order APT-VDF [51] and the SPA-VDF [41-50], since both are compatible with MCDM-I and provide multiple LP responses of fixed TBW and ω_c anywhere from 0.25π to 0.5π from a fixed-coefficient prototype filter. Both VDFs are reviewed in brief below.

a) First Order Allpass Transformation Based Variable Digital Filters

The APT-VDF was first proposed in [51] and further extended in [67-69]. The detailed literature review of the APT-VDF is provided in Section 2.4.2 of Chapter 2. They are realized by replacing each unit delay of a digital filter with first order allpass structure. The frequency response of the transformed filter is then identical to the frequency response of the prototype filter on a distorted frequency scale. By changing the coefficient of an allpass structure, the distortion of the frequency axis and hence the cut-off frequency of the VDF is varied. They are also known as warped filters since the output response is warped version of the input response.

Consider an N^{th} order FIR filter (also called as prototype filter) with transfer function H(z) and cut-off frequency, f_{c0} . Let $H_{\alpha}(z)$ be the VDF, with cut-off frequency $f_{c\alpha}$, obtained by replacing every delay of H(z) with first order allpass structure, A(z) [51] i.e.

$$H_{\alpha}(z) = H(A(z)) \tag{5.6}$$

where

$$A(z) = \left(\frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}}\right) \qquad |\alpha| < 1$$

The implementation of $H_{\alpha}(z)$ and A(z) are shown in Fig. 5.4 [51] and Fig. 5.5 [80] respectively. The coefficients of the prototype filter h_0 , h_1 ,..., h_N are fixed and can be hardwired. By changing α , the cut-off frequency, $f_{c\alpha}$, of $H_{\alpha}(z)$ changes. For $-1 < \alpha < 0$, the transformation is backward which means $f_{c\alpha} < f_{c0}$ and for $0 < \alpha < 1$, the effect is the





Fig. 5.5. First order allpass transformation, A(z) [80].

reverse i.e. forward transformation which means $f_{c\alpha} > f_{c0}$ [51]. When $\alpha = 0$, the APT-VDF is reduced to the prototype filter (i.e. H(z)) with unit delay and the cut-off frequency, f_{c0} . The complementary response is obtained by subtracting the output from appropriately delayed version of the input signal. The APT-VDF requires (2.5*N + 1) multipliers and (5*N + 1) adders to obtained LP response and its complementary response. For each additional LP response, extra N multipliers and (3*N+1) adders are required. Though the prototype filter is an FIR filter, $H_{\alpha}(z)$ is a non-linear phase filter due to the APT [51, 36].

▶ Page 142

b) Spectral Parameter Approximation Based Variable Digital Filters

SPA-VDFs can be designed to provide variable cut-off frequencies or fractional delays or both [41-50]. The details of SPA-VDFs are provided in Section 2.4.3 of Chapter 2. The block diagram of SPA-VDF, $H(z, \alpha)$, is shown in Fig. 5.6 where $H_i(z)$, $0 \le i \le L$, are N^{th} order fixed-coefficient FIR sub-filters and α is the variable parameter which controls the cut-off frequency of $H(z, \alpha)$ [41-50]. The transfer function, $H(z, \alpha)$ can be expressed as

$$H(z,\alpha) = \sum_{k=0}^{L} H_k(z) \,\alpha^k \tag{5.7}$$

The transfer function of $k^{th} N^{th}$ order fixed-coefficient sub-filter, $H_k(z)$, is given by,

$$H_k(z) = \sum_{n=0}^{N} h_k(n) z^{-n}$$
(5.8)

where $h_k(n)$ is symmetrical impulse response of $H_k(z)$. Then, Eq. (5.7) can be re-written as



Fig. 5.6. The SPA-VDF with FIR sub-filters in transposed direct form.

$$H(z,\alpha) = \sum_{k=0}^{L} \sum_{n=0}^{N} h_k(n) z^{-n} \alpha^k$$
(5.9)

A number of optimization techniques such as minimax approximation [47, 48], linear programming [41, 46], least square [44], weighted least square [42, 43, 45, 49, 50] and constrained least square [45] have been proposed in literature to determine sub-filter coefficients, $h_k(n)$ so that the frequency response of $H(z, \alpha)$ will approximate the desired response as a function of α [41-50]. SPA-VDFs have advantages such as linear phase, fixed TBW, smaller overall group delay, fewer number of variable multipliers and improved accuracy over APT-VDFs. From Fig. 5.9, it can be observed that additional LP responses can be easily obtained from fixed sub-filters by adding extra branches and the cut-off frequency of each response can be controlled individually using distinct control parameter α . The SPA-VDF requires only L extra multipliers and L adders for each additional output compared to the ATP-VDF [51] which requires N and 3*N (N is generally much higher than L) multipliers and adders respectively. Also, complementary response can be easily obtained in SPA-VDFs using fewer number of delays and a subtractor compared N multipliers and (2*N+1) adders required in APT-VDFs. However, the overall complexity of SPA-VDFs [41-50] is still high compared to ATP-VDFs [51]. Also, coefficient values of sub-filters in SPA-VDFs increase exponentially with their order which is problematical when fixed-point implementation is needed. Since the subfilter order depends on cut-off frequency range, SPA-VDFs are preferred for the applications which require narrow cut-off frequency range analogous to the requirement of the prototype VDF in the proposed MCDM based VDF and filter bank design.

5.1.4 Proposed Variable Digital Filter Architectures

The architectures of the proposed VDF using the SPA-VDF (termed as the SPA-MCDM VDF) and using the APT-VDF (termed as the APT-MCDM VDF) are shown in Fig. 5.7 and Fig. 5.8 respectively. The SPA-MCDM VDF consists of (L+1) fixedcoefficient sub-filters, $H_k(z)$ where $0 \le k \le L$, each of order N. The detailed architecture of k^{th} sub-filter is shown in Fig. 5.7 (b). The filter coefficients of these sub-filters corresponding to the cut-off frequency range from 0.25π to 0.5π , desired TBW of TBW_d, passband and stopband ripples of δ_p and δ_s respectively are obtained using one of optimization procedures discussed in Section 5.1.3. The sub-filter coefficients are fixed and can be hardwired. The control signals, sell D_l and sel2 D_l , select the MCDM-I factor D_I for the two branches of these sub-filters [29]. Two fixed-coefficient masking filters, $H_{m1}(z)$ and $H_{m2}(z)$, each with the cut-off frequency and the TBW of 0.5 and (0.5 – $2*TBW_d$) respectively are used to mask the higher frequency subband of multiband response obtained using the MCDM-I as discussed before. The sub-filters along with controlling parameters, α_1 , α_2 , $(0 \le (\alpha_1, \alpha_2) \le 1)$ and output logic unit (OLU) provide LP and HP responses with desired cut-off frequencies. The second branch with controlling parameter α_2 is used to provide BP response, $y_3(z)$, by subtracting $y_2(z)$ from $y_1(z)$ where cut-off frequencies of $y_2(z)$ and $y_1(z)$ are equal to rising and falling edge cut-off frequency of desired BP response respectively. Similarly, variable BS responses can be obtained. The architecture of the ATP-MCDM VDF is shown in Fig. 5.8 where A(z) is first order APT as shown in Fig. 5.5. It can be observed that complementary response in the APT-MCDM VDF needs N multipliers compared to only delays required in the SPA-MCDM VDF.



Fig. 5.7. (a) Architecture of the SPA-MCDM VDF, (b) Architecture of sub-filter, $H_k(z)$.

Z-1

(b)

SUB

¥

ADD/

SUB

SUB

Ŧ

ADD/

SUB

Z-1

SUB

¥

ADD/

SUB

 Z^{-1}

sel2_D_{II}

The architectures shown in Fig. 5.7 and 5.8 also correspond to a 3-subband reconfigurable filter bank. In this case, $y_1(z)$ and $y_2(z)$ provide LP and BP responses respectively while complementary of $y_3(z)$ provides HP response. Using control signals, *sel1_D₁*, *sel2_D₁*, α_1 , α_2 , the bandwidth and location of each subband can be controlled. For *M*-subband filter banks, the architecture consists of (*M*-1) branches and (*M*-1) OLU.



Fig. 5.8. Architecture of the APT-MCDM VDF.

In the next section, the complexity comparison of the proposed architectures with other architectures is presented.

5.2 Complexity Comparison For Variable Digital Filters

Consider the design of the VDF with TBW_d of 0.2π , passband and stopband ripple of 0.1 dB and -50 dB respectively. The VDF is expected to provide variable LP, HP, BP and BS responses anywhere over entire Nyquist band. A 16x16 bit multiplier, a 2:1 multiplexer, and 32 bit adder were synthesized on a TSMC 0.18µm process. The Synopsys Design Compiler was used to estimate the cell area. The area in terms of gate count is obtained by normalizing the cell area values by that of a two input NAND gate from the same library. The total gate count in Table 5.1 is the sum of gate counts of all the components. The "±x" values in Table 5.1 indicate the percentage increase of total gate count in respective VDF realization methods when compared with the SPA-MCDM VDF.

No. of VDFs	Multipliers	Multiplexers	Adders	Total gate count	Delay in samples
SPA-VDF [41-50]	542	0	1023	1097375 (+247%)	31
APT-VDF [51]	146	92	288	301620 (-4 %)	NA
MCDM-VDF [29]	503	2000	2001	1325025 (+318%)	≤ 501
MFT-VDF	163	43	301	330030 (+4%)	80
APT-MCDM VDF	126	38	251	258955 (-18%)	NA
SPA-MCDM VDF	132	210	435	316425	25

TABLE 5.1. GATE COUNT COMPLEXITY COMPARISON OF VARIABLE DIGITAL FILTERS

The term "NA" in Table 5.1 indicates that group delay is not constant i.e. non-linear phase VDF. All the VDFs in Table 5.1 are designed to provide variable LP, HP, BP and BS responses anywhere on normalized frequency scale with TBW_d of 0.2π , passband and stopband ripple of 0.1 dB and -50 dB respectively. The gate count calculations of each VDF are explained in detail below:

- SPA-VDF [41-50]: The SPA-VDF, shown in Fig. 5.6, consists of L sub-filters each of order N. To obtain BP and BS response, two branches are used similar to the proposed architecture in Fig. 5.7. For the design example considered here, the order of sub-filters, N = 62 and the order of polynomial, L = 15. Then,
 - a) Total number of multiplications = 32*16 (sub-filter coefficients) + 2*15 (multiplications with α) = 542.
 - b) Total number of additions = 62*16 (sub-filter coefficients additions) + 2*15(additions for α) + 1 (output logic unit) = 1023.

- APT-VDF [51]: The APT-VDF requires first order APT to obtain variable LP and HP responses and second order APT to obtain variable BP and BS responses. For the desired specifications, the order of the prototype filter is 36. Then,
 - a) Total number of multiplications = 19*2 (corresponds to prototype filter coefficients) + 36 (first order APT) + 72 (second order APT) = 146.
 - b) Total number of additions = 3*36 (first order APT branch) + 5*36 (second order APT branch) = 288.
 - c) Total number of 2-input multiplexers = 19 (selecting prototype filter coefficients)
 + 36 (selecting between LP or HP response) + 36 (selecting between BP or BS response) + 1 (output selection) = 92.
- 3) **MCDM-VDF [30]:** Since MCDM-VDF [30] provides only coarse control over the cut-off frequency, the resolution between cut-off frequencies is fixed to 0.02π compared to other VDFs which provide an unabridged control over the cut-off frequency. Then, for the design example considered here, the order of the prototype filter is 1000 and the range of D_{II} is 1 to 25.
- 4) Modified frequency transform (MFT) based VDF (MFT-VDF): The linear phase MFT-VDF presented in Chapter 4 provides variable LP, HP, BP and BS responses and has wider cut-off frequency range than previous frequency transform based VDFs. For the design example considered here, order of the prototype filter is 40.

- 5) **APT-MCDM VDF:** For the desired specifications, the APT-MCDM VDF consists of the prototype filter order 30 and 2 masking filters each of order 18. Then,
 - a) Total number of multiplications = 16 (prototype filter coefficients) + 2*10 (2 masking filters) + 3*30 (first order APT) = 126.
 - b) Total number of additions = 30*2 (prototype filter coefficients additions, 2 factor is due to MCDM-I) + 2*18 (2 masking filters) + 3*2*30 (first order APT) + 5 (output logic unit) = 251.
 - c) Total number of 2-input multiplexers = 2*16 (MCDM-I) + 6 = 38.
- 6) **SPA-MCDM VDF:** For the desired specifications, proposed SPA-MCDM VDF, consists of 6 sub-filters each of order 32 and 2 masking filters each of order 18. Then,
 - a) Total number of multiplications = 17*6 (sub-filter coefficients) + 2*10 (2 masking filters) + 2*5 (multiplications with α) = 132.
 - b) Total number of additions = 32*6*2 (sub-filter coefficients additions, 2 factor is due to MCDM-I) + 2*18 (2 masking filters) + 2*5 (additions for α) + 5 (output logic unit) = 435.
 - c) Total number of 2-input multiplexers = 2*17*6 (MCDM-I) + 6 = 210.

The gate count complexity comparisons in Table 5.1 show that the SPA-MCDM VDF provides low complexity alternative to previous SPA-VDFs [41-50] when desired cut-off frequency range is wide. The complexity of the SPA-VDF increases steeply with the cut-

off frequency range and hence they are preferred when desired cut-off frequency range is narrow. In the SPA-MCDM VDFs, MCDM-I allows the prototype VDF to have narrow cut-off frequency range even if desired cut-off frequency range is wide and hence the SPA-MCDM VDF needs 247% less gate count than SPA-VDFs [41-50]. Since the MCDM-VDF [29] is preferred when coarse control over wide range of cut-off frequency is desired, its complexity is huge compared to the SPA-MCDM VDF for the design example considered here. Also, the SPA-MCDM VDF requires 4% less gate count compared the MFT-VDF. For narrow cut-off frequency range, SPA-VDFs [41-50] have much higher complexity and higher delay than the MFT-VDF. However, for wide cut-off frequency range, the SPA-MCDM VDF have less complexity and reduced delay than the MFT-VDF since latter is incompatible with the MCDM-I due to Taylor structure. The group delay of the SPA-MCDM VDF is lowest among all other linear phase VDFs.

The APT-MCDM VDF requires 16% less gate counts than the APT-VDF [51]. The APT-VDF, despite non-linear phase, is widely used for energy detection based spectrum sensing and various audio signal processing applications [67-69]. Though the complexity of the APT-MCDM VDF is lower than the linear phase SPA-MCDM VDF, the SPA-MCDM VDF is preferred over the APT-MCDM VDF for communication applications such as channelization, cyclostationary or higher order statistics based spectrum sensing where phase of input signal affects the performance of DSP algorithms and hence linear phase VDFs are required.

The variable LP responses obtained using the SPA-MCDM VDF are shown in Fig. 5.9.



Fig. 5.9. Variable LP responses obtained using the SPA-MCDM VDF.

The passband and stopband ripple are 0.1 dB and -50 dB respectively. The range of the cut-off frequency for $TBW_d = 0.2\pi$ is 0.1π to 0.9π . In Fig. 5.9, responses in blue, green, red and black colors are obtained using the procedures 1-4 in Section 5.1.2 respectively. Similarly, variable HP, BP and BS responses can be obtained. In the next section, the complexity comparison of the filter banks is presented.

5.3 Complexity Comparison For Filter Banks

A reconfigurable *M*-subband filter bank with TBW_d of 0.2π , passband and stopband ripple of 0.1 dB and -50 dB respectively is designed which provides independent and individual control over the subband bandwidth as well as their center frequency. The architectures of the SPA-MCDM filter bank and the APT-MCDM filter bank are similar to that shown in Fig. 5.7 and Fig. 5.8 respectively where *M*-subband filter bank has (*M*-1) branches and (*M*-1) OLUs. The gate count comparisons of 4-subband and 8-subband reconfigurable filter banks designed using various VDFs are shown in Table 5.2. The

		No. of Subband	ds = 4	No. of Subbands = 8	
Filter Bank using		Total gate count	Delay in samples	Total gate count	Delay in samples
SPA -VDF [41-50]	Α	1125010 (+222%)	31	1235550 (+156%)	31
APT-VDF [51]	B	525575 (+50%)	NA	1421395 (+195%)	NA
MCDM-VDF [29]	С	1582050 (+353%)	≤ 501	2622950 (+445%)	≤501
MFT-VDF	D	529385 (+51%)	38	1328905 (+176%)	38
APT-MCDM VDF	E	349120	NA	709780 (+47.5%)	NA
SPA-MCDM VDF	F	348980	25	481000	25

TABLE 5.2. GATE COUNT COMPLEXITY COMPARISON OF FILTER BANKS ($TBW_d = 0.2$)

"±x" values in Table 5.2 indicate the percentage increase of total gate count in respective filter bank realization methods when compared with the SPA-MCDM filter bank. The term "NA" in Table 5.2 indicates that group delay is not constant i.e. non-linear phase filter bank. It can be observed that the proposed linear phase SPA-MCDM filter bank (F) provides substantial reductions in gate counts over other filter banks. Also, the group delay of the SPA-MCDM filter bank is lowest among all filter banks.

In Fig. 5.10, the plot of percentage difference in gate count for filter banks 'A', 'B', 'C', 'D', 'E' with respect to the SPA-MCDM filter bank (F) for different number of subbands is shown. Though both the filter banks 'A' and 'F' are designed using SPA-VDFs, gate count complexity of proposed filter bank 'F' is much lower than that of 'A'. Likewise, in case of filter banks 'B' and 'E' designed using ATP-VDFs, gate count complexity of 'E' is much lower compared to that of 'B'. For the design example considered here, each extra output branch in case of 'E' requires total gate count of 90165

(multiplications = 40, adders = 101, multiplexers = 34) compared to 33005 (multiplications = 15, adders = 23, multiplexers = 103) in case of 'F'. Hence, even if the APT-MCDM VDF requires less gate count than the SPA-MCDM VDF as shown in Table 5.1, the SPA-MCDM filter bank 'F' is computationally efficient than 'E' and 'B' especially when number of subbands are more (> 4). Additionally, 'F' is a linear phase filter bank while 'E' and 'B' are non-linear phase filter banks. The complexity of filter bank designed using the MFT-VDF (D) increases rapidly with the number of subbands due to Taylor structure which requires separate prototype filter for each output response. For the design example considered here where $TBW_d = 0.2\pi$, $\delta_p = 0.1$ dB and $\delta_s = -50$ dB, selected frequency responses obtained using the proposed 3-subband SPA-MCDM filter bank are shown in Fig. 5.11 (a)-(d) along with the values of parameters α_l , α_2 . It can be observed that the bandwidth and the center frequency of each subband can be controlled individually using the SPA-MCDM filter bank. Furthermore, the bandwidth and the center frequency of subbands are not constrained to any fixed range or set of values.



Fig. 5.10. Complexity comparison of filter banks for different number of subbands.


Fig. 5.11. Frequency responses of the 3-subband SPA-MCDM filter bank,

(a) $\alpha_1 = 0.2$, $\alpha_2 = 0.2$, $LP = H_{1\alpha02}^m(z)$, $BP = H_{2\alpha13}^m(z) - H_{1\alpha02}^m(z)$, $HP = 1 - H_{2\alpha13}^m(z)$, (b) $\alpha_1 = 0.2$, $\alpha_2 = 0.7$, $LP = H_{1\alpha02}^m(z)$, $BP = H_{2\alpha13}^m(z) - H_{1\alpha02}^m(z)$, $HP = 1 - H_{2\alpha13}^m(z)$, (c) $\alpha_1 = 0.1$, $\alpha_2 = 0.55$, $LP = H_{1\alpha11}^m(z)$, $BP = H_{2\alpha14}^m(z) - H_{1\alpha11}^m(z)$, $HP = 1 - H_{2\alpha14}^m(z)$, (d) $\alpha_1 = 0.01$, $\alpha_2 = 0.99$, $LP = H_{1\alpha13}^m(z)$, $BP = H_{2\alpha13}^m(z) - H_{1\alpha13}^m(z)$, $HP = 1 - H_{2\alpha13}^m(z)$.

5.4 Combined Channelization and Spectrum Sensing

Cognitive radio (CR) has been proposed as an effective solution for mitigating the imbalance between the spectrum scarcity because of the rapid development of various radio access technologies and poor spectrum utilization mainly due to spectrum management strategies [8, 12, 13, 64]. In the CR network, the secondary (unlicensed) user needs to perform spectrum sensing along with channelization. In spectrum sensing, CR senses the environment over huge swaths of spectrum to search for vacant band and ensure adaptive transmission within vacant band without causing interference to primary (licensed) user [12, 13, 64]. In channelization, CR receives the data transmitted by another CR by extracting the desired channel of interest. In either operations, filter or filter bank plays an important role to select the desired channel(s) of interest.

A variety of emerging applications such as public safety networks, smart grid networks, wireless medical networks and cellular networks need CRs to access unlicensed vacant bands ultimately improving overall spectrum utilization [93]. The area complexity and power consumption of wireless devices must be low to make it handy to use and lasts for a longer period in emergencies. Also, faster spectrum sensing increases the time available for useful communication which in turn increases the achievable throughput. Additionally, in order to extend the capabilities of existing public safety, cellular and wireless medical networks beyond voice to video, data, and visualized location-based services that require distinct bandwidths, CRs must be able to search the vacant band and extract the channel of required bandwidths. Hence, reconfigurable filters and filter banks with individual and independent control over the bandwidth and the center frequency of subbands are desired.

Consider a typical practical scenario where the wideband input signal of 12 MHz bandwidth consists of multiple radio channels of bandwidths ranging from 200 kHz to 5 MHz. The locations and bandwidth of channel may vary dynamically. The DFE extracts the channel of interest and passed it to the demodulator block for further baseband processing. In addition, the DFE also selects the desired frequency band and passed it to the detector block to check whether the frequency band is vacant or not. Using conventional filter bank such as DFTFB [7, 20], 64-subband filter bank is required since the resolution of filter bank is decided by smallest channel bandwidth (i.e. 200 kHz) rather than total number of detectors and demodulators which is 2 for the design example considered here. Out of these 64-subbands, single or combination of multiple adjacent subbands is passed to the demodulator. Similarly, another single subband or combination of multiple adjacent subbands is passed to the detector. The proposed architecture for combined serial channelization and spectrum sensing is shown in Fig. 5.12 where number of subbands are decided by the total number of demodulators and detectors. For the scenario considered here, 5-subband SPA-MCDM filter bank which provides 2 bandpass responses, one for channelization and other for spectrum sensing is used. The bandwidth and the center frequency of each bandpass response can be controlled independently.



Fig. 5.12. Combined channelization and spectrum sensing approach.

Chapter 5 – Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

The gate count complexity comparisons in Table 5.3 show that the DFTFB approach requires 118% higher gate counts than the proposed approach.

TABLE 5.3. GATE COUNT COMPLEXITY COMPARISON OF COMBINED CHANNELIZATION AND SPECTRUM SENSING APPROACHES

No. of Filter Bank	Multipliers	Multiplexers	Adders	Total gate count
DFTFB [7, 20]	400	0	798	819550 (+118%)
SPA-MCDM filter bank	162	216	485	374845

In some cases, CR is required to keep track of multiple vacant bands, e.g. shift to other frequency band when primary user arrives or optional shift to suitable vacant band of wider bandwidth, preferred frequency range or less interference to enable better communication. In Fig. 5.13, the relation between gate count complexities vs. number of subbands processed is plotted. It can be observed that proposed approach is a low complexity alternative to conventional filter bank approach when fewer number of frequency bands need to be processed i.e. upto 18 subbands for the design example



Fig. 5.13. Gate count of filter bank vs. number of subbands processed.

considered here. Here the gate count complexities of other VDFs are not shown since the comparisons in Table 5.1 and Table 5.2 indicated that the SPA-MCDM VDFs has lower gate count complexity than other VDFs.

5.5 Filter Bank for Digital Hearing Aids

In [69], a 3-subband filter bank designed using the APT-VDF is proposed for low power digital hearing aids. It consists of variable LP, BP and HP filters in parallel. However, the complexity of the BP filter, which uses second order APT, almost doubles than that of filters where first order APT is used. In Table 5.4, the gate count comparisons for 3-subband filter banks with $TBW_d = 0.2\pi$, passband and stopband ripple of 0.1 dB and -50 dB respectively is shown. Both the filter banks provide individual and independent control over the bandwidth and the center frequency of each subband. It can be observed that the filter bank in [69] requires 35% higher gate counts compared to the APT-MCDM filter bank.

	No. of subbands = 3			
No. of	[69]	APT-MCDM Filter bank		
Multipliers	181	126		
Multiplexers	0	66		
Adders	440	370		
Total gate count	388600 (+35%)	287160		

TABLE 5.4. GATE COUNT COMPLEXITY COMPARISON FOR 3-SUBBAND FILTER BANKS

▶ Page 159

5.6 Summary

In this chapter, a low complexity and reduced delay VDFs (SPA-MCDM VDF and APT-MCDM VDF) with an unabridged control over the cut-off frequency on entire normalized frequency scale is presented. The proposed VDFs also provide variable LP, HP, BP and BS responses without the need of complex hardware reconfiguration and time consuming coefficient updates. The gate count complexity comparison results show that the SPA-MCDM VDF provides substantial savings in gate counts over other linear phase VDFs. The complexity of the APT-MCDM VDF, designed using APTs, is less than the SPA-MCDM VDF but APT-MCDM VDF no longer exhibits linear phase property which limits its utility in various communication applications.

The proposed VDFs are then extended to the design of reconfigurable filter banks. The linear phase SPA-MCDM filter bank and non-linear phase APT-MCDM filter bank provide independent and individual control over the bandwidth and the center frequency of subbands. The complexity comparison shows that the proposed filter banks provide substantial savings in gate counts and has reduced group delay compared to other filter banks. The usefulness of the proposed filter bank for area efficient combined channelization and spectrum sensing in CRs and digital hearing aids are also elaborated.

Though the APT-MCDM VDF is a non-linear phase VDF, it can be useful for energy detection based spectrum sensing as well as various audio signal processing applications and is computationally efficient than linear phase SPA-MCDM VDF. However, the complexity of the APT-MCDM VDF increases at a faster rate than that of the SPA-

▶ Chapter 5 – Modified CDM Based Variable Digital Filters and Reconfigurable Filter Banks

MCDM VDF when number of VDF outputs increases. This is because, each output of the APT-MCDM VDF requires N multipliers and (3*N+1) adders compared to L multipliers and L adders in case of the SPA-MCDM VDF where N is prototype filter order, L is polynomial order and N > L. Furthermore, to obtain complementary response, the APT-MCDM VDF requires N multipliers and (2*N+1) adders whereas the SPA-MCDM VDF needs fewer number of delays and a subtractor. In the next chapter, a new architecture for efficient implementation of the APT-VDF by combining first and second order APT with the CDM is proposed to further reduce the complexity of the APT-VDF.

Chapter 6 Reduced Second Order Allpass Transformation Based Variable Digital Filters

In resource-constrained battery operated multi-standard wireless communication receivers (MWCRs) for cognitive radios (CRs), energy detection is the first choice for spectrum sensing since it is simple, very low complex and easy to implement compared to cyclostationary and higher order statistics based detection [93, 94, 101]. In the energy detection, an energy of the signal in a given frequency band is calculated and compared with certain threshold to detect whether the frequency band is vacant or not [93, 94, 101]. Since the decision taken by the energy detector is solely based on the energy of input signal and independent of phase of input signal, non-linear phase allpass transformation (APT) based variable digital filters (VDFs) [51, 67-69] can be used due to their lower complexity instead of linear phase VDFs. In this Chapter, a new design of low complexity VDF by integrating reduced second order transformation based APT-VDFs with coefficient decimation-II (CDM-II) is proposed. It shall be referred to as APT-CDM VDF. In the next Section, brief review of APT-VDFs is done.

6.1 Allpass Transformation Based Variable Digital Filters

The APT-VDF is obtained by replacing each unit delay of a digital filter with the allpass structure of an appropriate order [51]. The comprehensive review of APT-VDFs is provided in Section 2.4.2 (a) of Chapter 2. When first order APT is used, the type of the prototype filter decides the type of response of the APT-VDF [51]. For example, lowpass (LP) and bandpass (BP) prototype filters provide variable LP and variable BP responses, respectively. Note that, in case of variable BP and bandstop (BS) responses, the two variable parameters, the center frequency and the bandwidth, depend on a single controlling parameter i.e. APT coefficient, α , where $|\alpha| < 1$. For example, variable BP responses obtained using the APT-VDF with the bandpass prototype filter and first order APT are shown in Fig. 6.1. It can be observed that APT-VDFs using first order APT fail to provide variable bandwidth responses for a given center frequency since each value of α corresponds to distinct center frequency.



Fig. 6.1. Variable bandpass responses using the APT-VDF where $|\alpha| < 1$.

Alternatively, when the APT-VDF with bandpass prototype filter and first order APT is combined with the CDM-II [24], variable BP responses can be obtained as shown in Fig.



Fig. 6.2. Variable bandpass responses using the APT-VDF with bandpass prototype filter, first order APT and the CDM-II.

6.2. By changing α and D_{II} , the center frequency and the bandwidth can be varied respectively. Similarly, variable BS responses can be obtained using bandstop prototype filter. However, whenever the type of the response needs to be changed, the prototype filter coefficients will need to be updated, which incurs large number of memory read and write operations as well as larger reconfiguration delay. Furthermore, it can be observed from BP responses in Fig. 6.1 and Fig. 6.2 that they are not symmetrical about their center frequencies. Hence, to obtain variable bandwidth responses from lowpass prototype filter with symmetry about center frequency, second order APT is proposed in [51]. This means that the APT-VDF would require separate first and second order APT branches to obtain variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) responses making the overall filter highly complex and power inefficient.

The reduced second order APT, $B_r(z)$, provides fixed bandwidth BP and BS responses from LP prototype filter [51]. The APT-VDF, G(z), obtained from lowpass prototype

filter, H(z), by replacing each unit delay with $B_r(z)$ is given by,

$$G(z) = H(B_r(z)) \tag{6.1}$$

where

$$B_r(z) = \mp z^{-1} \left(\frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}} \right) = -z^{-1} A(z) \qquad |\alpha| < 1$$

Here, A(z) is first order APT and α is the APT coefficient. The '-' sign indicates LP to BP transformation while '+' sign indicates LP to BS transformation. The multiplier complexity of $B_r(z)$ and A(z) is same. Thus, APT-VDFs with LP prototype filter and $B_r(z)$ provide variable LP, HP, fixed bandwidth BP and fixed bandwidth BS responses. But, the prototype filter coefficients need to be updated whenever a change in bandwidth is required. Thus, existing APT-VDFs, cannot provide variable LP, HP, BP and BS responses from fixed-coefficient lowpass prototype filter.

In Chapter 5, low complexity VDF using modified coefficient decimation method (MCDM) and first order APT based VDF is proposed and it is termed as APT-MCDM VDF. The APT-MCDM VDF provides variable LP, HP, BP and BS responses on entire Nyquist band. The complexity comparison showed that APT-MCDM VDF requires lower gate counts than existing VDFs.

The APT-MCDM VDF, with N^{th} order prototype filter, needs two parallel branches of first order APTs (i.e. 2N multipliers and 6N adders) to obtain BP and BS responses. Furthermore, the APT-MCDM VDF needs an additional branch of APTs (i.e. N

multipliers and 2*N* adders) to obtain complementary response for the MCDM. In the next Section, a new APT-CDM VDF is presented which offers further reduction in total gate count compared to the APT-MCDM VDF.

6.2 Proposed Variable Digital Filter

In the proposed APT-CDM VDF, a fixed-coefficient lowpass prototype filter, H(z), is used and reduced second order APT, $B_r(z)$, is combined with the CDM-II to obtain variable LP, HP, BP and BS responses. In the APT-CDM VDF, fixed bandwidth BP and BS responses at an arbitrary center frequency are obtained using $B_r(z)$ and then the CDM-II is employed to change the bandwidth. The variable LP and HP responses are obtained by bypassing one delay element of $B_r(z)$ using multiplexers to obtain A(z) which provides LP-LP and LP-HP transformations.

In some cases, finite impulse response (FIR) filters are preferred over infinite impulse response (IIR) filters because IIR techniques do not directly address the design of a filter with an arbitrary cut-off frequency and requires high precision in the design and actual operation [102]. Furthermore, the round-off error of an FIR filter is easier to analyze and to control than that of IIR filter. In this thesis, the APT-CDM VDF design using FIR prototype filter is considered. The proposed approach can also be extended to the design of the APT-CDM VDF using IIR prototype filter. Note that even if FIR prototype filter is used, the APT-CDM VDF has non-linear phase characteristics as a result of the APT [51].

6.2.1 Design of the APT-CDM VDF

Consider an Nth order lowpass prototype filter, H(z), with the cut-off frequency, ω_{c0} $(= 2\pi f_{c0})$ and coefficients h_0, h_1, \dots, h_N . The APT-CDM VDF architecture is shown in Fig. 6.3. The filter coefficients are fixed and hence can be hardwired. The CDM-II is implemented using the multiplexers controlled by N-bit signal, sel_D_{II} . For example, when $D_{II} = 1, 2, 3$, the values of sel_D_{II} will be "00...0", "10101...0", "110110....0" respectively. The multiplexers select signals, sel_{f_1} (1 bit) and sel_{f_2} (1 bit), decide the type of the output response. The values of sel_{f_1} and sel_{f_2} to obtain LP, HP, BP and BS responses are $\{1, 1\}, \{0, 1\}, \{1, 0\}$ and $\{0, 0\}$ respectively. The different variable frequency responses are obtained as follows:-

a) Variable LP responses are obtained using the transformation given by Eq. (6.2) [51].

$$G(z) = H(A(z)) \tag{6.2}$$

where



 $A(z) = \left(\frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}}\right)$

Chapter 6 – Reduced Second Order Allpass Transformation Based Variable Digital Filter

b) Variable HP responses are obtained using the transformation given as [51],

$$G(z) = H(-A(z))$$
(6.3)

c) Fixed bandwidth BP responses at an arbitrary center frequency are obtained using the reduced second order APT, $B_r(z)$ in Eq. (6.1) and given by [51],

$$G(z) = H(B_r(z)) \tag{6.4}$$

where

$$B_r(z) = -z^{-1} \left(\frac{-\alpha + z^{-1}}{1 - \alpha z^{-1}} \right) = -z^{-1} A(z) \qquad |\alpha| < 1$$

d) Fixed bandwidth BS responses at an arbitrary center frequency are obtained using the reduced second order APT, $B_r(z)$ in Eq. (6.1) and given by [51],

$$G(z) = H(-B_r(z)) \tag{6.5}$$

In the APT-CDM VDF, there are two controlling parameters, APT coefficient, α and decimation factor, D_{II} where $|\alpha| < 1$ and D_{II} can be any positive integer. In cases (a) and (b), both the parameters control the cut-off frequency of LP and HP responses respectively. In cases (c) and (d), α controls the center frequency and D_{II} controls the bandwidth of BP and BS responses respectively. In this way, different types of variable responses can be obtained using fixed-coefficient lowpass prototype filter.

6.2.2 Mathematical Derivation

The mathematical relation between desired cut-off frequency, $\omega_{c\alpha}$ (= $2\pi f_{c\alpha}$), prototype filter cut-off frequency, ω_{c0} (= $2\pi f_{c0}$) and APT coefficient α derived in [51] is modified in this section by introducing new term of decimation factor, D_{II} . The frequency and phase responses of first order causal stable real-coefficient allpass filter are given by [51]

$$A(e^{j\omega}) = \frac{-\alpha + e^{-j\omega}}{1 - \alpha e^{-j\omega}}$$
(6.6)

$$\theta_c(\omega) = -\omega - 2\tan^{-1}\left[\frac{\alpha\sin\omega}{1 - \alpha\cos\omega}\right]$$
(6.7)

The phase delay, $\tau_p(\omega)$, of the $A(e^{j\omega})$ in Eq. (6.6) is given by [51]

$$\tau_p(\omega) = -\frac{\theta_c(\omega)}{\omega} = 1 + \frac{2}{\omega} \tan^{-1} \left[\frac{\alpha \sin \omega}{1 - \alpha \cos \omega} \right]$$
(6.8)

The relation between ω_{c0} and $\omega_{c\alpha}$ for given α and D_{II} is given by,

$$\omega_{c\alpha} = \frac{\omega_{c0}}{\tau_p(\omega_{c\alpha})} \cdot D_{II} \tag{6.9}$$

$$\therefore \ \omega_{c0} = \frac{\omega_{c\alpha}}{D_{II}} + \frac{2}{D_{II}} \tan^{-1} \left[\frac{\alpha \sin \omega_{c\alpha}}{1 - \alpha \cos \omega_{c\alpha}} \right]$$
(6.10)

Using algebraic simplification, it can be shown that

▶ Page 169

$$\alpha = \left[\frac{\tan x}{\sin \omega_{c\alpha} + \tan x \cdot \cos \omega_{c\alpha}}\right] \tag{6.11}$$

where

$$x = \frac{(D_{II} \cdot \omega_{c0}) - \omega_{c\alpha}}{2}$$

Using Eq. (6.11), the value of α required to obtain the desired $\omega_{c\alpha}$ (= $2\pi f_{c\alpha}$) can be calculated. In case of BP and BS responses, where reduced second order APT is used, the value of α for the desired value of center frequency, *f_{center}*, is given as [51],

$$\alpha = -\cos(f_{center} \cdot \pi) \tag{6.12}$$

The bandwidth of BP responses is D_{II} times the passband width of the prototype filter.

6.3 Design Example

The performance of the APT-CDM VDF is illustrated with the help of a suitable design example. All the frequency edges mentioned here are normalized with respect to half of the sampling frequency. Let the desired peak passband and stopband ripple specifications are 0.02 dB and -80 dB respectively. The cut-off frequency, f_c , and the TBW of the prototype filter are 0.06 and 0.02 respectively. The variable LP responses obtained using the APT-CDM VDF and zoomed passband ripples are shown in Fig. 6.4 using different colors. f_c can be changed anywhere from 0.01 to 0.99 i.e. an unabridged control over entire Nyquist band. The TBW depends on α and D_{II} and varies between 0.002 and 0.1.



Fig. 6.4. Variable lowpass responses using the APT-CDM VDF.

The variable BP responses with $f_{center} = 0.548$ for $\alpha = 0.15$ are shown in Fig. 6.5. As the value of D_{II} increases, the bandwidth increases. By changing α , the center frequency can be varied as shown in Fig. 6.6 where variable BP responses with $f_{center} = 0.452$ for $\alpha =$ -0.15 are shown. Similarly, variable HP and variable BS responses can be obtained. In Fig. 6.7, variable BP responses with $f_{center} = 0.548$ for $\alpha = -0.55$, using another prototype filter with f_c and TBW of 0.015 and 0.02 respectively, are shown. The relation between



Fig. 6.5. Variable bandpass responses using the APT-CDM VDF for $\alpha = 0.15$.

desired center frequency of bandpass response, f_{center} , and corresponding value of APT coefficient, α , is shown in Fig. 6.8. The wider bandwidths can be obtained by using higher values of D_{II} . Since the APT-CDM VDF and the APT-VDF [51] use same APT and the CDM affects only magnitude response, phase or group delay characteristics of the APT-CDM VDF are identical to that of the APT-VDF [51].



Fig. 6.6. Variable bandpass responses using the APT-CDM VDF for $\alpha = -0.15$.



Fig. 6.7. Variable bandpass responses using second design example for $\alpha = -0.55$.



Fig. 6.8. Relation between APT coefficient, α and desired center frequency of bandpass

response (f_{center}).

6.4 Implementation Complexity

In this section, the complexity comparison of the APT-CDM VDF with that of APT-VDFs [51, 68] in terms of total number of gate counts is presented. A 16x16 bit multiplier, a 2:1 multiplexer and a word of memory and 32 bit adder were synthesized on a TSMC 0.18 μ m process. The Synopsys Design Compiler was used to estimate the cell area. The area in terms of gate count, as shown in Table 6.1, was obtained by normalizing the above area values by the cell area of a 2-input NAND gate from the same library. The values "±x%" in last row of Table 6.1 indicates the difference in percentage gate counts when compared with the APT-CDM VDF.

The CDM-II has an inherent disadvantage that the stopband attenuation deteriorates as the decimation factor is increased [24]. Hence, the prototype filter needs to be overdesigned. Thus, the order of the prototype filter for the APT-CDM VDF is 600 compared

	(A)	(B)	(C)	(D)	
VDFs No. of	APT-VDF [51] $0.013 \le f_c \le 0.93$	APT-VDF with memory [68]	APT-VDF without memory [68]	VDF with 1 st and 2 nd order APT	APT-CDM VDF
Multipliers	827	827	2750	1928	901
Multiplexers	0	1100	1650	1101	1800
Adders	1375	1650	1650	3850	1800
Words of memory	2208	2200	0	0	0
Total gate count	1803595 (-11%)	1945650 (-2.7%)	5121875 (+61%)	4184587 (+52%)	1999735

TABLE 6.1. GATE COUNT COMPLEXITY COMPARISON OF APT-VDFs

to 550 for the APT-VDFs in [51, 68]. The TBW varies between 0.002 and 0.1 in all the cases. The results can be summarized as follows.

The APT-VDF in [51] (A) uses first order APT. Though the complexity of the APT-CDM VDF is higher than 'A', the latter needs a large number of memory read and write operations to update the prototype filter coefficients each time the type of response or the bandwidth needs to be changed. Also, the range over which f_c can be varied is larger in the APT-CDM VDF than 'A' by 6.4%. The APT-VDF in [68] is similar to the APT-CDM VDF except filter coefficients corresponding to each bandwidth are either stored in memory (B) or implemented in parallel (C). Though, the total gate count complexity of the APT-CDM VDF is slightly higher than 'B', the latter requires a large number of memory read and write operations and hence larger reconfiguration delay whenever the bandwidth of the BP response needs to be changed. The performance of the APT-CDM VDF and 'C' are identical. Furthermore, the APT-CDM VDF offers a total gate count saving of 61% over 'C'. The VDF (D), designed using first and second order APTs, provides complete control over the bandwidth and f_c . However, the gate count

requirement of 'D' is 52% more than the APT-CDM VDF.

The APT-CDM VDF, filters 'C' and 'D' are implemented on Xilinx Virtex 4vsx35-10ff668 FPGA for functionality verification and power consumption analysis. The filters 'A' and 'B' are not implemented because they need to update filter coefficients whenever type or bandwidth of response need to be changed. The prototype filter order is reduced to 75 for the APT-CDM VDF and 60 for 'C', 'D' respectively due to limited FPGA resources. The order of the prototype filter is chosen high (75) in the APT-CDM VDF compared to orders of prototype filter in 'C' and 'D' (60) taking into account of stopband attenuation deterioration due to the CDM-II. The stopband performance of the APT-CDM VDF is same as that of 60th order filters, 'C' and 'D'. The power consumption values for the APT-CDM VDF, 'C' and 'D' are 558mW, 752mW and 830mW respectively. The APT-CDM VDF offers power saving of 26% and 33% over 'C' and 'D' respectively.

6.5 Applications

In this section, applications of the APT-CDM VDF are elaborated in detail.

6.5.1 Application 1: Energy Detection Based Spectrum Sensing

The APT-CDM VDF finds applications in the energy detection based serial spectrum sensing in battery operated area and power constrained CRs. In serial spectrum sensing, input signal from the desired frequency bands is extracted using VDF and passed to the energy detector one by one to determine whether band is vacant or not [93]. The gate count complexity comparison between SPA-MCDM VDF, APT-MCDM VDF and APT-

CDM VDF is shown in Table 6.2 for TBW_d of 0.2π , passband and stopband ripple of 0.1 dB and -50 dB respectively. It can be observed that the SPA-MCDM VDF and the APT-MCDM VDF require 104% and 67% higher gate count compared to the APT-CDM VDF.

TABLE 6.2. GATE COUNT COMPARISON OF APT-CDM VDF, APT-MCDM VDF AND SPA-MCDM-VDF

VDFs No. of	SPA-MCDM VDF	APT-MCDM VDF	APT-CDM VDF	
Multipliers	132	126	73	
Multiplexers	210	38	144	
Adders	433	249	144	
Total gate count	315975	258955	154240	
	(+104%)	(+67%)		

In spectrum sensing scenarios such as 1) Switch to other frequency band when primary user arrives, 2) Find a vacant band with wider bandwidth, desired frequency range or less interference to improve the performance etc., CRs may need information about multiple vacant bands. This approach is known as block serial spectrum sensing. In block serial spectrum sensing, the number of VDF outputs as well as the number of energy detectors are more than one but fewer compared to total number of channels present in the wideband input signal. In Fig. 6.9, the plot of total gate count vs. number of VDF output branches is shown which indicates that the APT-CDM VDF is favorable for block serial spectrum sensing compared to the APT-MCDM VDF.

6.5.2 Application 2: Audio Signal Processing

In addition to spectrum sensing, APT-VDFs are widely used for various audio applications such as linear prediction, echo cancellation, loudspeaker equalization, spectrally modifying an audio signal, detection of bandpass signals in a broadband signals



Fig. 6.9. Total gate count vs. number of VDF outputs (number of energy detectors).

etc. [67-69, 102]. In [67], the APT-VDF is used for audio equalizer applications and the results showed that the APT-VDF with FIR prototype filters are better than traditional FIR filters. In [68], adaptive filters are designed using the APT to detect bandpass signals in a broadband signal. These adaptive filters are reduced second order APT based APT-VDFs that provide fixed bandwidth BP responses at an arbitrary center frequency. However, whenever the bandwidth needs to be changed, the filter coefficients are updated, which incurs a large number of memory read and write operations and larger reconfiguration delay. Thus, adaptive filters in [68] perform poorly when input signals are dynamically varying. The APT-CDM VDF provides alternative solution to [68] where the subband bandwidth can be changed via *sel_D_{II}* and the complexity comparisons in Table 6.1 showed that the gate count overhead in APT-CDM VDF is only 2.7% compared to that of VDF in [68].

6.6 Filter Bank Complexity Comparisons

Consider the design of reconfigurable filter bank with independent and individual control over the subband bandwidth and the center frequency using SPA-MCDM VDF, APT-MCDM VDF and APT-CDM VDF. The SPA-MCDM VDF and APT-MCDM VDF provide two LP responses and they are combined to obtain BP and BS responses i.e. 3-subband filter bank while the APT-CDM VDF provides only one response which may be LP, HP, BP or BS i.e. 1-channel filter bank. Hence, when reconfigurable filter bank is designed using these VDFs, the SPA-MCDM filter bank is more computationally efficient especially when the number of subbands are more (≥ 4) as shown in Fig. 6.10. In addition, the SPA-MCDM filter bank is a linear phase filter bank while other two are non-linear phase filter banks.



Fig. 6.10. Total gate count vs. number of subbands.

6.7 Summary

In this chapter, a new area and power efficient VDF using reduced second order APT and CDM is presented. It is called as APT-CDM VDF. The APT-CDM VDF provides variable LP, HP, BP and BS responses from the fixed coefficient lowpass prototype filter similar to APT-MCDM VDF and SPA-MCDM VDF presented in Chapter 5. The complexity comparison showed that the proposed VDFs, SPA-MCDM VDF, APT-MCDM VDF and APT-CDM-VDF, offer substantial savings in total gate counts over other VDFs. The complexity of the APT-CDM VDF is lowest among all these VDFs and they can be used for energy detection based serial sensing operations as well as various audio signal processing applications. On the other hand, the SPA-MCDM VDFs, due to linear phase characteristics, are favored in communication applications such as channelization, cyclostationary and higher order statistics based spectrum sensing etc.

The low complexity and reduced delay reconfigurable filter bank designed using these VDFs provide independent and individual controls over the subband bandwidth and their center frequencies. The gate count complexity comparisons showed that the linear phase SPA-MCDM filter bank provides substantial savings in gate counts and have lower delay compared to other filter banks.

Chapter 7

Conclusions and Future Works

In this chapter, a brief synopsis of the contributions as well as conclusions of the work presented in this thesis is done. Some directions for future work in this research area are also identified.

7.1 Conclusions

This thesis addressed the hardware-efficient implementation issues of variable digital filters (VDFs) and reconfigurable filter banks in the digital front-end (DFE) of multistandard wireless communication receivers (MWCRs). The wideband digitized input signal to the DFE consists of multiple channels of uniform and non-uniform bandwidth, corresponding to distinct communication standards. The task of the DFE is to extract desired channel(s) of interest for further baseband processing using subsequent digital signal processing (DSP) algorithms. Depending on the number of channels and whether the channels are processed in serial, block-serial or parallel fashion in subsequent DSP algorithms, either the VDF or reconfigurable filter bank is employed in the DFE. The VDF and filter bank architectures need to take into account inter-standard channel bandwidth variations in the upcoming standards such as high speed packet access (HSPA), long term evolution (LTE) as well as the intra-standard channel bandwidth variations. For example, the LTE supports distinct channel bandwidths ranging from 1.25 MHz to 20 MHz while channel bandwidths in Global Systems for Mobile Communications (GSM), code division multiple access (CDMA) and wideband-CDMA (W-CDMA) are 200 kHz, 1.25 MHz and 5 MHz respectively. The VDF and reconfigurable filter bank should also be in-field upgradable to support imminent communication standards. To support multiple existing as well as imminent communication standards, VDFs that provide variable lowpass (LP), highpass (HP), bandpass (BP) and bandstop (BS) response over entire normalized frequency scale, and reconfigurable filter banks that provide independent and individual control over the bandwidth and the center frequency of subbands are desired. The area, power, delay and reconfiguration delay of the VDF and the filter bank should be as small as possible to enable efficient realization of all the MWCR functionalities on battery operated resource-constrained mobile handsets.

Most of the existing VDF and filter bank architectures [7, 20-22] are designed and optimized for supporting single communication standard. In the multi-standard communications scenario, these architectures incorporate reconfigurability either by using parallel structures to switch between communication standards or by updating the filter coefficients stored in memory beforehand, corresponding to different communication standards. This is not an efficient approach due to high penalties in area complexity, power consumption and reconfigurable architectures for multi-standard operations [23-33].

However, these architectures are moderately reconfigurable since they support a fewer number of communication standards at the cost of huge penalties in terms of area, power and delay. In this thesis, new area, delay and power efficient VDFs and reconfigurable filter banks for the DFE in the emerging MWCRs of SDRs and CRs have been proposed.

The first contribution of this thesis is a low complexity reconfigurable filter bank based on coefficient decimation (CDM) and frequency response masking (FRM) technique. It is called as CDM-FRM filter bank [J1, C1]. In the CDM-FRM filter bank, the subband bandwidth is changed by changing the decimation factor D_{II} and fixedcoefficient masking filters are used to extract individual subbands by masking undesired subbands. The design example showed that the CDM-FRM filter bank provides uniform as well as non-uniform bandwidth subbands along with fractional control over the bandwidth and the center frequency of subbands. The functionality of the CDM-FRM filter bank is validated for different input signal spectrum scenario and smaller mean square error values between the samples of the extracted channels and the respective samples of input signal indicated good channelization performance [J1, C1]. The estimated gate count comparison and implementation results on Xilinx Virtex-2 FPGA showed that the CDM-FRM filter bank offers substantial savings in gate counts and total power consumption over other filter banks. The application of the CDM-FRM filter bank for accurately detecting the frequency edges of multiple channels in wideband input signal for multi-standard military communication receivers was presented [C2]. Simulation results showed that the CDM-FRM filter bank based edge detection approach

is computationally more efficient than other edge detection approaches for a given error in channel edge frequency [C2].

The aim of next contributions presented in this thesis was to improve the CDM-FRM filter bank to achieve an unabridged control over the bandwidth and the center frequency of subbands. This can be done by replacing the CDM-VDF with a VDF that offers an unabridged control over the cut-off frequency on a wide frequency range. The second contribution of this thesis is a new design of the VDF using second order fractional delay filter employing modified Farrow structure of Lagrange interpolation and it is called as modified Farrow structure based VDF (MF-VDF) [C3]. By changing the coefficients of Farrow structure, the cut-off frequency of the MF-VDF is changed. The MF-VDF is unique in the sense that the transition bandwidth (TBW) of the VDF is narrower than the TBW of the prototype filter and the cut-off frequency can be changed on either side of the cut-off frequency of the prototype filter. However, all existing lower order fractional delay filters have flat magnitude and phase/group delay responses up to lower frequencies only [35]. Hence, the MF-VDF, which employs second order fractional delay filter using Farrow structure, is suitable for applications where an unabridged control over the cut-off frequency on a lower frequency range is desired.

The third contribution of this thesis is the modified frequency transformation based VDF (MFT-VDF) [C4]. The MFT-VDF when combined with the CDM-I provides variable LP, HP, BP and BS responses from a fixed-coefficient prototype filter without the need of hardware re-implementation which makes them suitable for applications such

as serial channelization, serial spectrum sensing etc. The design example showed that the MFT-VDF has a wider cut-off frequency range compared to its predecessors based on second order frequency transform [40] and offered total gate count savings of 33% and 41% over VDFs in [40] and [48] respectively. In addition, other VDFs need to update filter coefficients and filter architecture to obtain variable BP and BS responses.

In the fourth contribution of this thesis, reconfigurable fast filter bank (RFFB) has been presented where the prototype filter in the first stage of the FFB is replaced with the MFT-VDF [J2]. By changing the cut-off frequency of the MFT-VDF, the RFFB provides an unabridged control over the subband bandwidth within desired range. The implementation results indicated that the filter banks using VDF in [40], [48] and CDM-DFTFB [25] required 45%, 78% and 135% higher gate counts respectively compared to the RFFB. The RFFB also provides fine control over center frequencies of fixed bandwidth subbands. This unique property makes the RFFB suitable for the channelization and spectrum sensing scenarios where the channel bandwidth is fixed but their locations may vary dynamically. The RFFB is useful in minimizing the dynamic power consumption of two-stage spectrum sensing by reducing the rate of activation of the second sensing stage [C6].

In existing modulated filter banks [7, 20, 21, 25], interpolation based filter banks [22, 26, 32, 91] as well as the CDM-FRM filter bank [J1, C1] and the RFFB [J2], the subband bandwidth depends on a single parameter i.e. cut-off frequency of the prototype filter. When the cut-off frequency of the prototype filter is changed, the bandwidth of all

subbands changes simultaneously. For wideband input signal in MWCRs where channel bandwidths ranges from 200 kHz (GSM) up to 20 MHz (LTE), the resolution of above filter banks, which is inversely proportional to the bandwidth of narrowest channel, is very high. Higher the resolution of the filter bank, higher is the area complexity, power consumption and delay. In order to reduce the complexity and the group delay of the filter bank, its resolution must be equal to the number of channels concurrently handled by the subsequent DSP block and the resolution should be independent of the channel bandwidth. To achieve this, a filter bank which provides independent and individual control over the bandwidth and the center frequency of subbands is desired.

The fifth contribution in the thesis is new design of low complexity and reduced delay VDF using modified CDM (MCDM) [J4]. The proposed VDF is designed by replacing the prototype filter in the MCDM with the existing VDF that is required to provide an unabridged control only over the narrow cut-off frequency range precisely over the second quarter of the normalized frequency. When linear phase spectral parameter approximation (SPA) based VDF is used, the proposed VDF is called as SPA-MCDM VDF [J4] and when non-linear phase allpass transformation (APT) based VDF is used, the proposed VDF is called as APT-MCDM VDF. The SPA-MCDM VDF and the APT-MCDM VDF provide variable LP, HP, BP and BS responses over entire Nyquist band. For the design example considered, the SPA-MCDM VDF offered total gate count savings of 318%, 247% and 4% over the MCDM-VDF [29], the SPA-VDF [41-50] and the MFT-VDF respectively besides having lower group delay than other VDFs.

The sixth contribution of this thesis is a linear phase SPA-MCDM filter bank, designed using the SPA-MCDM VDF, and it provides independent and individual control over the bandwidth and the center frequency of subbands [C7]. The gate count complexity and the group delay of the SPA-MCDM filter bank was lower compared to other filter banks. The usefulness of the SPA-MCDM filter bank for combined channelization and spectrum sensing in CRs was presented.

The seventh contribution in this thesis is a new architecture for efficient implementation of the APT-VDF by combining first and second order APT with the CDM. It is called as APT-CDM VDF [C5, J3]. The APT-CDM VDF offered further saving in gate counts over the APT-MCDM VDF and other VDFs. This is achieved by reducing the number of APT branches and eliminating the need for complimentary response. At the end, gate count complexity analysis of the SPA-MCDM filter bank, APT-MCDM filter bank and APT-CDM filter bank was presented. The SPA-MCDM filter bank offered substantial savings in gate count over others in addition of having linear phase characteristic.

For an easy evaluation, the summary of the different contributions and the key results obtained in this thesis is given in Table 1.2 of Chapter 1. The summary of comparison between existing VDFs and VDFs presented in this thesis is given in Table 7.1. Similarly, the summary of comparison between existing filter banks and filter banks presented in this thesis is given in Table 7.2.

variable LP, HP, BP and BS Group Reconf. Gate RAM/ VDFs Phase responses over entire Count Delay Delay ROM Nyquist band Programmable Very Low Low Linear Yes Yes filter [74-79] high Need of separate first and **APT-VDFs** Nonsecond order APTs leads to High NA Low No [51, 67-69] linear very high gate count complexity. Need of separate transformations leads to very Frequency transformation High High Linear No high gate count complexity Low VDFs [36-40] and limited cut-off frequency range. Yes but preferred for short **SPA-VDFs** Very Very Low Linear No range of Nyquist band due to [41-50] high low very high complexity. FRM-VDF Very Very Coarse control over bandwidth Low Linear No high [31, 33, 86] Low and center frequency. SPA-FRM VDF Very Very Yes Low Linear No [23] high high Coarse control over bandwidth **CDM-VDF** [24] Low Low Low Linear No and center frequency. MF-VDF [C3] High High Low Linear No No Limited section of Nyquist MFT-VDF [C4] Low High Low Linear No band. SPA-MCDM Very High Low Linear No Yes **VDF** [**J**4] low **APT-MCDM** Non-Low NA Low Yes No VDF linear APT-CDM VDF Non-Low NA Yes Low No [**J**3] linear

TABLE 7.1. COMPARISON OF DIFFERENT VDFs

	Cata			Decouf	Control over subband's		
Filter bank	Count	Group Delay	ROM	Delay	Center	bandwidth	
					Frequency	Independent	Unabridged
РС	Very	Low	Ves	Very	Unabridged	Ves	Ves
approach [7]	High	LOW	105	high	Ullabiluged	105	105
DFTFB	Low	Low	No	high	No	No	No
[7, 20]				8			
MPRFB [21]	High	Low	No	High	No	No	No (Coarse)
CDM-							No
DFTFB [25]	Low	Low	No	Low	No	No	(Coarse)
GFB [7]	Low	Low	No	High	Unabridged	No	No
FFR [22]	Very	Very	No	High	No	No	No
110 [22]	low	high	110	mgn	NO	110	110
Multi-	Very	Very					No
resolution	low	high	No	Low	No	No	(Coarse)
FFB [26]							
CDM filter	Low	Low	No	Low	Coarse	No	No
bank [24]							(Coarse)
Progressive							NT.
decimated	High	High	No	Low	Coarse	Yes	NO (Casesa)
1111er Dank							(Coarse)
CDM-FRM							
filter bank	Very	Very	No	Low	Coarse	No	No
[C1, I1]	low	high	110	Low	course	110	(Coarse)
	Verv	Verv					
RFFB [J2]	low	high	No	Low	Unabridged	No	Yes
SPA-MCDM		Vom					
filter bank	High	Low	No	Low	Unabridged	Yes	Yes
[C7]		LUW					

▶ Page 188

7.2 Future Work

In this thesis, five low complexity VDFs (MF-VDF, MFT-VDF, SPA-MCDM VDF, APT-MCDM VDF and APT-CDM VDF) and three reconfigurable filter banks (CDM-FRM filter bank, RFFB, SPA-MCDM filter bank) were proposed for channelization, spectrum sensing tasks in the DFE of MWCRs. The proposed architectures are also suitable for audio signal processing tasks, emerging wireless body area networks, next generation satellite based communication systems etc. Some directions to pursue further research in this area have been identified and discussed below.

7.2.1 Exploiting the Redundancies in SPA-VDF Architecture

SPA-VDFs [41-50] have many advantages such as fixed TBW, lower group delay, fewer adjustable parameters and higher accuracy over other VDFs [36-40]. The proposed SPA-MCDM VDF extends the cut-off frequency range of the SPA-VDF over entire normalized frequency scale while the SPA-MCDM filter bank provides independent and



Fig. 7.1. SPA-VDF.

individual control over the bandwidth and the center frequency of subbands. Current research on the SPA-VDF is focused on reducing the computation time and complexity of optimization algorithms used to calculate sub-filter coefficients. However, the implementation complexity of the SPA-VDF can be significantly reduced by sharing the variable multipliers among multiple branches. In the SPA-VDF, each output branch requires L variable multipliers where L is a polynomial order as shown in Fig. 7.1. These L variable multipliers determine the cut-off frequency of the VDF. In the FPGA implementation of the VDF and filter bank, gate count complexity of a variable multiplier is very high compared to that of a fixed multiplier, an adder or a multiplexer. Hence, if the number of variable multipliers is reduced by sharing them among multiple branches at the cost of few fixed multipliers, multiplexers and adders as shown in Fig. 7.2, the complexity of the SPA-VDF can be reduced further.

7.2.2 Low Complexity Variable Fractional Delay (VFD) Filters

The variable fractional delay (VFD) filters provide delays which are fractional multiple of the sampling interval [42, 104]. They are widely used for applications such as time delay estimation, beam steering of antenna array, speech coding and synthesis, music systems etc. A number of different VFD filter designs are available in the literature and the majority of these VFD filters employ a Farrow structure [42, 104] to provide on-thefly control over the delay. These VFD filters mainly differ in the type and performance of optimization algorithms used to calculate the sub-filter coefficients which decide the error between desired and actual value of delay as well as offline time for the calculation of sub-filter coefficients. However, the gate count complexity of all these VFD filters is
almost same. The primary aim is to combine the VFD filters with the CDM so as to achieve wider delay range and lower gate count complexity.

7.2.3 Area and Power Efficient Two-Stage Spectrum Sensing

In spectrum sensing, the secondary users (unlicensed users) scan the wideband input signal to search for vacant band(s). Usually, the DFE in CRs employs either VDF or filter bank to extract desired band(s) and subsequent DSP algorithms, e.g. energy detection, cyclostationary feature detector (CFD) etc., detect whether the band is vacant or not. A two-stage spectrum sensing has been proposed in [94, 95, 105, 106] which consists of basic sensing stage followed by advanced sensing stage. The main function of the basic sensing stage is to detect strong primary as well as secondary users quickly and the energy detection is generally preferred choice for the basic sensing stage [94, 95]. The advanced sensing stage is activated only if the energy detector decides the subband is empty and is usually done using the CFD. The two-stage spectrum sensing provides improved detection performance than single stage energy detection especially at low signal-to-noise ratio (SNR) and requires lower mean detection time compared to a single stage CFD [95]. However, the area complexity and power consumption of two-stage spectrum sensing is very high and dominated by CFDs. The spectrum sensing schemes in [105, 106] provide solutions to significantly reduce the dynamic power consumption of two-stage spectrum sensing up to 84% when the SNR is high but area complexity and static power consumption remains the same.

The spectrum utilization measurement surveys conducted by various countries indicated that 10-50% of the spectrum is underutilized [8-11] which means that not all the CFDs in a parallel two-stage sensing scheme are fully utilized. As a future work, it will be interesting to analyze the effect of reducing the number of CFDs on the mean detection time and implementation complexity for a given spectrum occupancy. Our preliminary results on area and power efficient two-stage spectrum sensing are presented in [C6]. In future, the proposed two-stage spectrum sensing scheme will be combined with *M*-subband SPA-MCDM filter bank followed by *M* energy detectors and *L* (< *M*) CFDs. The final aim would be to optimize the number of CFDs i.e. *L*, without compromising on detection parameters such as probability of detection (*P*_d), the probability of false alarm (*P*_{fa}) and mean detection time to search the desired number of vacant bands.

Bibliography

- [1] J. Wang, M. Ghosh, and K. Challapali, "Emerging cognitive radio applications: a survey," *IEEE Communications Magazine*, vol. 49, no. 3, pp. 74–81, Mar. 2011.
- [2] L. Van der Perre, J. Craninckx and A. Dejonghe, "Green Software Defined Radios," Springer, pp. 1-12, 2009.
- [3] E. Buracchini, "The software radio concept," *IEEE Communications Magazine*, Vol. 38, no. 9, pp. 138-143, Sep. 2000.
- [4] J. Mitola, "The software radio architecture," *IEEE Communications Magazine*, vo. 33, no. 5, pp. 26-38, May 1995.
- [5] J. Mitola, "Software radio architecture: a mathematical perspective," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 514-538, Apr. 1999.
- [6] J. H. Reed, "Software radio: A modern approach to radio engineering," pp. 2-4, Prentice Hall, 2002.
- T. Hentschel, M. Henker, and G. Fettweis, "The digital front-end of software radio terminals," *IEEE Personal Communications Magazine*, vol. 6, no. 4, pp. 40-46, Aug. 1999.
- [8] Federal Communications Commission: "Spectrum Policy Task Force," Rep. ET Docket no. 02-135, Nov. 2002.
- [9] Mark A. McHenry, Peter A. Tenhula, Dan McCloskey, Dennis A. Roberson, and Cynthia S. Hood, "Chicago spectrum occupancy measurements & analysis and a long-term studies proposal," in *Proceedings of Workshop on Technology and Policy for Accessing Spectrum (TAPAS)*, Boston, USA, August 2006.
- [10] M. Wellens, J. Wu and P. Mähönen, "Evaluation of spectrum occupancy in indoor and outdoor scenario in the context of cognitive radio," in *Proceedings of International Conference on Cognitive Radio Oriented Wireless Networks and Communications (CrownCom)*, pp. 420–427, Orlando, FL, USA, August 2007.

- [11] M. H. Islam, C. L. Koh, S. W. Oh, et al, "Spectrum survey in Singapore: occupancy measurements and analysis," in *Proceedings of the 3rd International Conference on Cognitive Radio Oriented Wireless Networks and Communications* (*CrownCom*), pp. 1-7, Singapore, May 2008.
- [12] J. Mitola and G. Q. Maguire, "Cognitive radio: Making software radios more personal," *IEEE Personal Communications*, vol. 6, no. 4, pp. 13-18, Aug. 1999.
- [13] S. Haykin, "Cognitive radio: brain-empowered wireless communications," *IEEE Journal on Selected Areas in Communications*, vol. 23, no. 2, pp. 201-220, Feb. 2005.
- [14] A. Haghighat, "A review on essentials and technical challenges of software defined radio," in *Proceedings of Military Communications Conference*, vol. 1, pp. 377-382, California, USA, Oct. 2002.
- [15] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE Journal of Solid-state Circuits*, vol. 42, no. 5, pp. 965-966, May 2007.
- [16] <u>http://www.ti.com/ww/en/analog/dataconverters/gigadc/rf-sampling.shtml</u>
- [17] National Semiconductor, "ADC12D1800- 12-Bit, Single 3.6 GSPS Ultra High-Speed ADC," App. Note, Feb. 2011.
- [18] T. Hentschel and G. Fettweis, "Sample rate conversion for software radio," *IEEE Communications Magazine*, vol. 38, no. 8, pp. 142-150, Aug. 2000.
- [19] T. Hentschel, "Channelization for software defined base-stations," Annales des Telecommunications, ISSN 0003-4347, vol. 57, no. 5-6, pp. 386-420, May 2002.
- [20] L. Pucker, "Channelization techniques for software defined radio," in *Proceedings* of SDR Forum Conference, pp. 1-6, Orlando, Nov. 2003.
- [21] W. A. Abu-Al-Saud and G. L. Stuber, "Efficient wideband channelizer for software radio systems using modulated PR filter banks," *IEEE Transactions on Signal Processing*, vol. 52, no. 10, pp. 2807-2820, Oct. 2004.
- [22] Y. C. Lim and B. Farhang-Boroujeny, "Fast filter bank (FFB)," *IEEE Transactions on Circuits & Systems II*, vol. 39, no. 5, pp. 316-318, May 1992.
- [23] D. Harris, "Computationally efficient variable linear-phase filters," *MSc thesis*, University of Miami, Florida, USA, March 2007.

[24] R. Mahesh and A. P. Vinod, "Low complexity flexible filter banks for uniform and non-uniform channelization in software radios using coefficient decimation," *IET Circuits, Devices & Systems*, vol. 5, no. 3, pp. 232-242, May 2011.

- [25] R. Mahesh and A. P. Vinod, "Reconfigurable discrete Fourier transform filter banks for variable resolution spectrum sensing," *IEEE International Conference* on Communication Systems, pp. 483-487, Singapore, Nov. 2010.
- [26] K. G. Smitha and A. P. Vinod, "A Multi-Resolution Fast Filter Bank for Spectrum Sensing in Military Radio Receivers," *IEEE Transactions on Very Large Scale Integration (VLSI) System*, vol. 20, no. 7, pp.1323-1327, June 2011.
- [27] R. Mahesh, A. P. Vinod, B. Y. Tan and E. M-K. Lai, "A tree-structured nonuniform filterbank for multi-standard wireless receivers," in *Proceedings of IEEE International Symposium on Circuits & Systems*, pp. 213-216, Taipei, Taiwan, May 2009.
- [28] L. Mengda, A. P. Vinod and S. C. Meng Samson "Progressive decimation filter banks for variable resolution spectrum sensing in cognitive radios," in *Proceedings of the 17th IEEE International Conference on Telecommunications*, pp. 857-863, Doha, Qatar, April 2010.
- [29] A. Ambede, K. G. Smitha and A. P. Vinod, "A modified coefficient decimation method to realize low complexity FIR filters with enhanced frequency response flexibility and passband resolution," 35th International Conference on Telecommunications and Signal Processing (TSP), pp. 658-661, Prague, Czech Republic, July 2012.
- [30] A. Ambede, K. G. Smitha and A. P. Vinod, "A low complexity uniform and nonuniform digital filter bank based on an improved coefficient decimation method for multi-standard communication channelizers," *Circuits, Systems & Signal Processing (Springer)*, DOI: 10.1007/s00034-012-9532-9, published online in Dec. 2012.
- [31] R. Mahesh and A. P. Vinod, "Reconfigurable frequency response masking filters for software radio channelization," *IEEE Transactions on Circuits & Systems II*, vol. 55. no. 3, pp. 274-278, Mar. 2008.

[32] J. W. Lee, Y. C. Lim and S. H. Ong, "A flexible and efficient sharp filter bank architecture for variable bandwidth systems", in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 2029- 2032, Greece, May 2006.

- [33] K. G. Smitha and A. P. Vinod, "A low complexity reconfigurable multi-stage channel filter architecture for resource-constrained software radio handsets," *Journal of Signal Processing Systems for Signal, Image and Video Technology, Springer*, Vol. 62, no. 2, pp. 217-231, Feb. 2011.
- [34] G. Stoyanov and M. Kawamata, "Variable digital filters," *J. Signal Processing*, vol. 1, no. 4, pp. 275–289, July 1997.
- [35] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay [FIR/all pass filter design]," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 30–60, Jan. 1996.
- [36] A. Oppenheim, W. Mechlenbräuker, and R. Mersereau, "Variable cutoff linear phase digital filters," *IEEE Transactions Circuits and Systems*, vol. 23, no. 4, pp. 199–203, Apr. 1976.
- [37] R. Crochiere and L. Rabiner, "On the properties of frequency transformations for variable cutoff linear phase digital filters," *IEEE Transactions Circuits and Systems*, vol. 23, no. 11, pp. 684–686, Nov. 1976.
- [38] S. S. Ahuja and S. C. Dutta Roy, "Linear phase variable digital bandpass filters," in *Proceedings of the IEEE*, vol. 67, no. 1, pp. 173–174, Jan. 1979.
- [39] S. Hazra, "Linear phase bandpass digital filters with variable cutoff frequencies," *IEEE Transactions on Circuits and Systems*, vol. 31, no. 7, pp. 661-663, July 1984.
- [40] S. D. Roy and S. Ahuja, "Frequency transformations for linear-phase variablecutoff digital filters," *IEEE Transactions Circuits and Systems*, vol. 26, no. 1, pp. 73–75, Jan. 1979.
- [41] C. K. S. Pun, S. C. Chan and K. L. Ho, "Efficient 1D and circular symmetric 2D FIR filters with variable cutoff frequencies using the Farrow structure and multiplier-block," *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 561–564, Sydney, Australia, May 2001.

[42] T. B. Deng, "Closed form design and efficient implementation of variable digital filters with simultaneously tunable magnitude and fractional delay," *IEEE Transactions on Signal Processing*, vol. 52, no. 6, pp. 1668-1681, June 2004.

- [43] T. B. Deng, "Weighted least-squares method for designing arbitrarily variable 1-D
 FIR digital filters," *Signal Processing (Elsevier)*, vol. 4, no. 4, pp. 597–613, Apr. 2000.
- [44] C. K. S. Pun, S. C. Chan, K. S. Yeung and K. L. Ho, "On the design and implementation of FIR and IIR digital filters with variable frequency characteristics," *IEEE Transactions* on *Circuits and Systems-II*, vol. 49, no. 11, pp. 689–703, Nov. 2002.
- [45] H. Johansson and P. Löwenborg, "On linear-phase FIR filters with variable bandwidth," *IEEE Transactions* on *Circuits and Systems-II*, vol. 51, no. 4, pp. 181-184, April 2004.
- [46] S. C. Chan, C. K. S. Pun, and K. L. Ho, "A new method for designing FIR filters with variable characteristics," *IEEE Signal Processing Letters*, vol. 11, no. 2, pp. 274–277, Feb. 2004.
- [47] K. M. Tsui, K. S. Yeung, S. C. Chan and K. W. Tse, "On the minimax design of passband linear-phase variable digital filters using semidefinite programming," *IEEE Signal Processing Letters*, vol. 11, no. 11, pp. 867-870, Nov. 2004.
- [48] P. Löwenborg and H. Johansson, "Minimax design of adjustable bandwidth linearphase FIR filters," *IEEE Transactions on Circuits and Systems-I*, vol. 53, no. 2, pp. 431–439, Feb. 2006.
- [49] S. S. Kidambi, "An efficient closed-form approach to the design of linear-phase FIR digital filters with variable-bandwidth characteristics," *Signal Processing* (*Elsevier*), vol. 86, no. 7, pp. 1656-1669, Oct 2005.
- [50] M. Zilong, L. Hui, A. Huiyao, W. Wang and J. Quan, "Algorithm of variable transition bandwidth FIR filters with weighted-least-square method," 2nd *International Conference on Computer Engineering and Technology*, vol. 7, pp. 321-324, Jodhpur, India, Apr. 2010.

▶ Page 197

[51] A. G. Constantinides, "Spectral transformations for digital filters," in *Proceedings* of the Institution of Electrical Engineers, vol. 117, no. 8, pp. 1585-1590, Aug. 1970.

- [52] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal of Selected Areas in Communications*, vol. 17, no. 4, pp. 539-550, Apr. 1999.
- [53] R. H. Walden, "Performance trends for analog-to-digital converters," *IEEE Communications Magazine*, vol. 37, no. 2, pp. 96-101, Feb. 1999.
- [54] P. I. Mak, U. Seng-Pan, and R. P. Martins, "Transceiver architecture selection: review, state-of-the-art survey and case study," *IEEE Circuits and Systems Magazine*, vol. 7, no. 2, pp. 6-25, second quarter 2007.
- [55] A. A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," *IEEE Transactions of Solid-State Circuits*, vol. 30, no. 12, pp.1399-1410, Dec. 1995.
- [56] M. Cao, Y. Zheng, and H. K. Garg, "A Novel Algorithm for DC Offset and Flicker Noise Cancellation in Direct Conversion Receivers," *International Conference on Communications and Systems*, pp. 441-445, Singapore, Sep. 2004.
- [57] S. J. Fang, A. Bellaouar, S. T. Lee, and D. J. Allstot, "An Image-Rejection Down-Converter for Low-IF Receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 478-487, Feb. 2005.
- [58] H. Berndt, R. Richter, and H. J. Jentschel, "A 100 MS/sec, 8th order Quadrature Sigma-Delta ADC for Complex-IF Signal Digitization in a Wideband-IF Sampling Receiver," *Proceedings of International Conference on ASIC*, vol. 1, pp. 669-672, Beijing, China, Oct. 2003.
- [59] R. M. Gray, "Oversampled sigma-delta modulation," *IEEE Transactions on Communications*, vol. 35, no. 5, pp. 481-489, May 1987.
- [60] S. Albrecht, "Sigma-delta based techniques for future multi-standard wireless radios," *PhD Thesis*, KTH, 2005.
- [61] A. Silva, N. H. Horta and J. G. Guilherme, "Reconfigurable multi-mode sigmadelta modulator for 4G mobile terminals," *Integration, The VLSI Journal*, vol. 42, no. 1, pp. 34-46, Jan 2009.

- [62] J. Markus and G. C. Temes, "An efficient ΔΣ ADC architecture for low oversampling ratios," *IEEE Transactions on Circuits and Systems-I*, vol. 51, no. 1, pp. 63-71, Jan. 2004.
- [63] O. Shoaei, "Continuous-Time Delta-Sigma A/D Converters for High Speed Applications," *PhD Thesis*, Carleton University, 1995.
- [64] S. Huang, X. Liu and Z. Ding, "Opportunistic spectrum access in cognitive radio networks", 27th Conference on Computer Communications (INFOCOM), pp. 1427-1435, Phoenix, USA, April 2008.
- [65] L. R. Rabiner, Multirate Digital Signal Processing, Prentice Hall PTR, Upper Saddle River, NJ, 1996.
- [66] J. Vankka, Digital Synthesizers and Transmitters for Software Radio, Springer-Verlag New York, pp. 239-257, 2005.
- [67] M. Karjalainen, E. Piirilä, A. Järvinen and J. Huopaniemi, "Comparison of Loudspeaker Equalization Methods Based on DSP Techniques", *Journal of Audio Engineering Society*, vol. 47, no. 1, pp. 14-31, Feb. 1999.
- [68] S. Koshita, Y. Kumamoto, M. Abe and M. Kawamata, "High-order centerfrequency adaptive filters using block-diagram-based frequency transformation," *IEEE International Conference on Acoustics, Speech and Signal Processing* (*ICASSP*), pp. 4284-4287, Prague, May 2011.
- [69] N. Ito, T. L. Deng, "Variable-bandwidth filter-bank for low-power hearing aids," 3rd International Congress on Image and Signal Processing (CISP), vol. 7, pp. 3207-3211, Yantai, China, Oct. 2010.
- [70] J. Lee, Y. Su, and C. Shen, "A comparative study of wireless protocols: Bluetooth, UWB, ZigBee, and Wi-Fi," 33rd Annual conference of the IEEE Industrial Electronics Society, pp. 46–51, Taipei, Taiwan, Nov. 2007.
- [71] A. Eghbali, H. Johansson, P. Löwenborg, and H. G. Göckler, "Dynamic frequency-band reallocation and allocation: from satellite-based communication systems to cognitive radios," *Journal of Signal Processing Systems*, vol. 62, no. 2, 187-203, Feb. 2011.
- [72] M. Bellanger, "On Computational Complexity in Digital Filters," in *Proceedings* of the European Conference on Circuit Theory and Design, pp. 58-63, 1981.

- [73] J. G. Proakis and D. G. Manolakis, "Digital signal processing," Prentice-hall, Inc., 3rd ed., 1996.
- [74] T. Solla and O. Vainio, "Comparison of programmable FIR filter architectures for low power," in *Proceedings of 28th European Solid-State Circuits Conference*, pp. 759-762, Firenze, Italy, Sep. 2002.
- [75] K. H. Chen and T. D. Chiueh, "A low-power digit-based reconfigurable FIR filter," *IEEE Transactions on Circuits and Systems-II*, vol. 53, no. 8, pp.617-621, Aug. 2006.
- [76] Woo Jin Oh and Yong Hoon Lee, "Implementation of programmable multiplierless FIR filter with powers-of-two coefficients," *IEEE Transactions Circuits and Systems-II*, vol. 42, no. 8, pp. 553–556, Aug. 1995.
- [77] H. R. Lee, C. W. Jen and C. M. Liu, "A new hardware-efficient architecture for programmable FIR filters," *IEEE Transactions Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 43, no. 9, pp. 637-644, Sept. 1996.
- [78] P. Tummeltshammer, J. C. Hoe and M. Puschel, "Time-multiplexed multipleconstant multiplication," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 26, no. 9, pp. 1551-1563, Sep. 2007.
- [79] P. K. Meher, "New approach to look-up-table design and memory-based realization of FIR digital filter," *IEEE Transactions Circuits and Systems*-I, vol. 57, no. 3, pp. 592-603, Mar. 2010.
- [80] S. K. Mitra and R. J. Sherwood, "Digital all-pass networks," *IEEE Transactions Circuits and Systems*, vol. 21, no. 5, pp. 688–700, Sep. 1974.
- [81] C. W. Farrow, "A continuously variable digital delay element," in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 2641–2645, Espoo, Finland, June 1988.
- [82] Y. C. Lim, "Frequency-response Masking Approach for the Synthesis of Sharp Linear Phase Digital Filters", *IEEE Transactions on Circuits and Systems*, vol. 33, no. 4, pp. 357-364, Apr. 1986.
- [83] Y. Lian, and C. Z. Yang, "Complexity reduction by decoupling the masking filters from bandedge shaping filter in frequency-response masking technique," *Circuits, Systems and Signal Processing*, vol.22, No.2, pp.115-135, Mar. 2003.

[84] J. Yu and Y. Lian, "Frequency-Response Masking Based Filters with the Even-Length Bandedge Shaping Filter," *in Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 536-539, Vancouver, Canada, May 2004.

- [85] M. Kapar, C. O. Solmaz, and A. H. Kayran, "Optimization of FIR filters synthesized using the generalized one-stage frequency-response masking approach," in Proceedings of 14th IEEE Signal Processing and Communication Applications, pp. 1–4, Antalya, Turkey, April, 2006.
- [86] Y. J. Yu, "Design of variable bandedge FIR filters with extremely large bandedge variation range," in Proceedings of IEEE International Symposium on Circuits and Systems, pp. 141-144, Rio de Janeiro, Brazil, May, 2011.
- [87] R. Mahesh, A. P. Vinod, C. Moy and J. Palicot, "A low complexity reconfigurable filter bank architecture for spectrum sensing in cognitive radios," in *Proceedings* of 3rd International Conference on Cognitive Radio Oriented Wireless Networks and Communications (CrownCom), pp. 1-6, Singapore, May 2008.
- [88] R. I. Hartley, "Subexpression sharing in filters using canonic signed digit multipliers," *IEEE Transactions on Circuits and Systems-II*, vol. 43, no. 10, pp. 677-688, Oct. 1996.
- [89] M. Martinez-Peiro, E. I. Boemo, and L. Wanhammar, "Design of high-speed multiplierless filters using a nonrecursive signed common subexpression algorithm," *IEEE Transactions Circuits and Systems-II*, vol. 49, no. 3, pp. 196-203, Mar. 2002.
- [90] A. G. Dempster and M. D. Macleod, "Use of minimum-adder multiplier blocks in FIR digital filters," *IEEE Transactions Circuits and Systems-II*, vol. 42, no. 9, pp. 569-577, Sep. 1995.
- [91] R. Mahesh and A. P. Vinod, "A New Low Complexity Reconfigurable Filter Bank Architecture for Software Radio Receivers Based on Interpolation and Masking Technique," in *Proceedings of Sixth IEEE International Conference on Information, Communications and Signal Processing,*, pp. 1-5, Singapore, Dec. 2007.
- [92] http://www.lyrtech.com/DSP-development/dsp_fpga/ signalmaster_quad_cpci.php.

[93] D. Cabric, S. M. Mishra and R. W. Brodersen, "Implementation issues in spectrum sensing for cognitive radios," *in 38th Asilomar Conference on Signals, Systems and Computers*, pp. 772-776, Pacific Grove, CA, Nov. 2004.

- [94] L. Luo, N. M. Neihart, S. Roy and D. J. Allstot, "A two-stage sensing technique for dynamic spectrum access," in *IEEE Transactions on Wireless Communications*, vol. 8, no. 6, pp. 3028-3037, June 2009.
- [95] S. Maleki, A. Pandharipande and G. Leus, "Two-stage spectrum sensing for cognitive radios," in IEEE International Conference on Acoustics Speech and Signal Processing (ICASSP), Texas, USA, pp. 2946-2949, Mar. 2010.
- [96] M. Narendar, A. P. Vinod, A.S. Madhukumar and Anoop Kumar Krishna, "An algorithm for spectrum sensing in cognitive radio using tree-structured filter bank," *in IEEE 17th International Conference on Telecommunications (ICT)*, pp. 418-424, Doha, Qatar, Apr. 2010.
- [97] M. Narendar, A. P. Vinod, A. S. Madhukumar and Anoop Kumar Krishna, "A tree-structured DFT filter bank based spectrum sensor for estimation of radio channel edge frequencies in military wideband receivers," in IEEE 10th International Conference on Information Sciences Signal Processing and their Applications (ISSPA), pp. 534-537, Kuala Lumpur, Malaysia, May 2010.
- [98] S. K. Mitra, Digital Signal Processing: A Computer-Based Approach, Singapore: McGraw-Hill, 1998.
- [99] V. Valimaki, "A new filter implementation strategy for Lagrange interpolation," in Proceedings of IEEE International Symposium on Circuits and Systems, vol. 1, pp. 361–364, Seattle, USA, May 1995.
- [100] C. Candan, "An efficient filtering structure for Lagrange interpolation," *IEEE Signal Processing Letters*, vol. 14, no. 1, pp. 17–19, Jan. 2007.
- [101] R. Mahesh and A. P. Vinod, "A low complexity flexible spectrum sensing scheme for mobile cognitive radio terminals," *IEEE Transactions on Circuits & Systems II*, vol. 58, no. 6, pp. 371-375, June 2011.
- [102] C. Asavathiratham, P. E. Beckmann and A. V. Oppenheim, "Frequency warping in the design and implementation of fixed-point audio equalizers," *IEEE Workshop*

on Applications of Signal Processing to Audio and Acoustics, NY, USA, pp. 55-58, Oct. 1999.

- [103] <u>http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_4/sysgen_us</u> <u>er.pdf</u>
- [104] W. S. Lu and T. B. Deng, "An improved weighted least-squares design for variable fractional delay FIR filters," *IEEE Transactions on Circuits and Systems-II*, vol. 46, no. 8, pp. 1035–1040, Aug. 1999.
- [105] Z. Khalaf, A. Nafkha and J. Palicot, "Enhanced hybrid spectrum sensing architecture for cognitive radio equipment," *XXXth URSI General Assembly and Scientific Symposium*, pp.1-4, Istanbul, Turkey, Aug. 2011.
- [106] P. R. Nair, A. P. Vinod, K. G. Smitha and Anoop Kumar Krishna, "Fast two-stage spectrum detector for cognitive radios in uncertain noise channels," *IET Communications*, vol. 6, no. 11, pp. 1341-1348, July 2012.