Loop Enhanced Passive Source- and Load-Pull Technique for High Reflection Factor Synthesis

Fadhel M. Ghannouchi, *Fellow, IEEE*, Mohammad S. Hashmi, *Member, IEEE*, Souheil Bensmida, *Member, IEEE*, and Mohamed Helaoui, *Member, IEEE*

***Abstract*—An original source- and load-pull topology based on a passive technique is presented in this paper. The proposed system consists of passive tuners and loop structures. The use of a passive loop structure in cascade with a passive tuner allows for synthesis of reflection coefficients in the order of 0.97 magnitudes at the device under test's access plane. The measurement and characterization results of a 1W GaAs MESFET device show an improvement of 0.9 dB in the gain and 6% in the power-added efficiency when the proposed impedance synthesis techniques are used.**

***Index Terms*—Load-pull, passive loop, reflection coefficient, source-pull, tuner.**

I. Introduction

POWER amplifier characterization is essential in order to optimize its performance, in terms of output power, efficiency and linearity, on one hand, and extraction or validation of its large signal model, on the other hand. One of the most used measurement technique for power amplifier optimization is the well-known source- and load-pull measurement procedure, which consists of varying the impedances presented at the device input and output ports to optimize the amplifier's performance. The variation of the impedances at the access planes of a device under test (DUT) can be performed using passive or active impedance synthesis or a combination thereof [1]–[10].

In a passive technique, the desired impedance is synthesized by varying the reflection coefficient of the impedance controlling element, as depicted in Fig. 1. The reflection coefficient is varied by tuning the phase and/or amplitude of the transmitted signal, b, with the help of a passive tuner. The main advantages of the passive technique are i) rapid impedance synthesis, ii) relatively higher power handling capability and measurements of high power devices with no nonlinear effects, iii) ease of usage, iv) low maintenance cost, v) relatively low implementation cost, and vi) the absence of any oscillation. However, due to the intrinsically passive nature of such systems, the synthesized reflection coefficients are typically limited in magnitude by the inherent losses in the tuner as well as the associated cablings. If the losses in the tuner are considered, then, depending on the operating frequency, the synthesized magnitude may range from 0.9 (few hundred MHz) down to 0.6 (approaching tens of GHz).

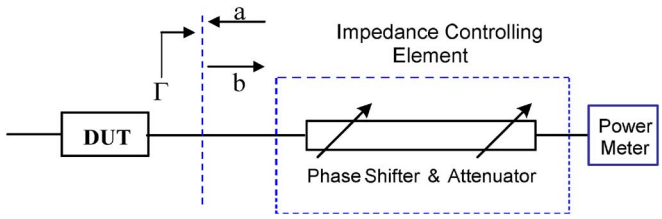

Fig. 1. A basic representation of a passive load-pull technique.

This major limitation implies that passive techniques cannot synthesize reflection coefficients whose values lie nearest to the Smith chart border. As a result, some Smith chart regions (those closer to the Smith chart border, i.e., low impedances) that are critical for high power devices are precluded. To overcome this issue, solutions have been proposed on the use of pre-matching networks [10], [11] at the device level or the use of pre-matched tuners [12], [13] at the measurement system level. In both these cases, the idea is based on the quarter-wave based pre-matching network transforming the tuner impedance to lower values.

The pre-matching network [10], [11] is capable of matching the microwave devices with sub-1 Ω output impedance; however, this requires additional hardware and calibration steps, increasing the size and cost of the system and the calibration time. State-of-the-art pre-matched passive structures [12], [13] are able to synthesize reflection coefficients in the order of 0.90–0.92 magnitudes in the practical applications, but the prices of such systems are relatively high. Passive source-/load-pull structure that are reasonably priced can typically synthesize reflection coefficient of magnitude 0.85.

Many source-/load-pull systems based on active structures have also been proposed in the literature [3]–[6], [14]–[18], in order to overcome the limitations encountered in the passive systems. Active load-pull systems consist of either active loop [4] or active branch [5] architectures. In both techniques, the reflection coefficient is synthesized at a DUT access plane by controlling the amplitude and phase of the injected signal. Active techniques of load synthesis suffers either from slow nature of load convergence in active branch structure or oscillation in the active loop architecture, thereby limiting the usefulness of active source- /load- pull systems.

Manuscript received March 19, 2010; revised August 11, 2010; accepted August 11, 2010. Date of publication October 07, 2010; date of current version November 12, 2010. This work was supported in part by iCORE, AB, Canada.

F. M. Ghannouchi, M. S. Hashmi, and M. Helaoui are with iRadio Laboratory, Department of Electrical and Computer Engineering, University of Calgary, Calgary, AB T2N 1N4, Canada (e-mail: fghannou@ucalgary.ca; mshashmi@ucalgary.ca; mhelaoui@ucalgary.ca).

S. Bensmida is with the Centre for Communications Research, University of Bristol, Bristol BS8 1UB, U.K. (e-mail: s.bensmida@bristol.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2010.2077990

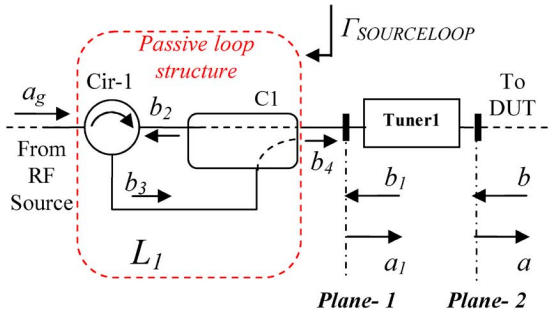

Fig. 2. The improved passive source-pull topology for synthesizing a high reflection coefficient.

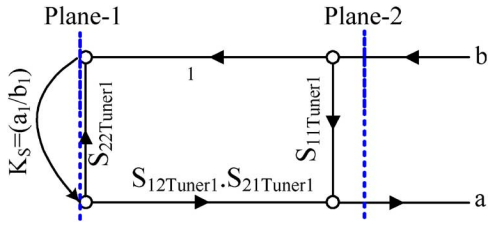

Fig. 3. Error flow model for the proposed source-pull topology.

To lessen the ultra high gain and high power requirements of the loop amplifier, a recent publication [7] has shown a load-pull system composed of an active structure and a passive structure combined together. The main claimed benefit reported in this publication is the replacement of ultra high gain loop amplifier with a reasonable high gain loop amplifier.

In this paper, a cost and calibration time effective passive structure for the synthesis of a high reflection coefficient is proposed. The passive structure is composed of a passive tuner followed by a passive loop. The passive loop is composed of a low loss circulator, a low loss coupler and a variable length transmission line. Two separate configurations are proposed for source- and load-pull measurement purposes. The proposed system, based on the fully passive elements, allows synthesis of reflection coefficients with magnitudes in the order of 0.97 at the DUT access planes. Only three transmission line lengths are required to cover the entire Smith chart, which reduces the calibration time compared to conventional pre-matching techniques.

This paper presents a comprehensive description and analysis along with an experimental evaluation and validation of the proposed source- and load-pull setups. Finally, measurement and characterization of a gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET) device is presented that validates the performances of the proposed source- and load-pull architectures.

II. Proposed Source- and Load-Pull Topology

A. Source Impedance Synthesis

The proposed source-pull topology is depicted in Fig. 2. It is apparent that the source impedance presented to the DUT input access plane, $Plane-2$, of the DUT is synthesized by the tuner, $Tuner1$, and the passive loop, which is composed of the circulator, $Cir-1$, and the directional coupler, $C1$.

The following relationships among the traveling waves b_2, b_3 and b_4 can be expressed as

$$b_2 = k_1 b_1 \tag{1}$$

$$b_3 = k_2 b_2 \tag{2}$$

$$b_4 = a_1 = k_3 b_3 \tag{3}$$

where k_1, k_2 and k_3 are complex constants that depend on the scattering parameters of the directional coupler, $C1$, and the circulator, $Cir-1$. The signal flow model for this architecture can be defined as given in Fig. 3.

The reflection coefficient presented by the passive loop structure, at Plane-1, is given by

$$\Gamma_{\mathrm{SOURCELOOP}} = K_S = \frac{a_1}{b_1} = |K_S|.e^{-2j\beta L_1} \tag{4}$$

where factor K_S represents the combined effect of the circulator, $Cir-1$, and the coupler, $C1$, and is defined by $K_S = k_1 k_2 k_3$. This factor depends on the length of the loop, L_1, and the phase velocity, β, of the travelling waves.

The error model from Fig. 3 can now be solved to obtain the total reflection coefficient of the synthesized source impedance at the DUT input access plane, $Plane-2$, as given by

$$\Gamma_S = \frac{a}{b} = S_{11\mathrm{TUNER1}} + \frac{S_{12\mathrm{TUNER1}} S_{21\mathrm{TUNER1}} K_S}{1 - S_{22\mathrm{TUNER1}} K_S}. \tag{5}$$

It is apparent from (5) that the incorporation of a passive-loop between the RF source and the $Tuner1$ enhances the Γ_S by the additional second term. In principle the cascade of the RF source and the passive-loop structure can be considered as a generator with non-50 Ω output impedance. This is the result of intentionally mismatching the source impedance of $Tuner1$. In other words, this can also be considered as the superposition of two waves a_g and b_4 travelling towards $Tuner1$ contributing in the enhancement of the Γ_S, where a_g is the wave generated by the RF source and b_4 is the wave caused by the reflected wave b_1 passing through the passive-loop and redirected toward $Tuner1$ by the passive-loop. The other parameter affecting the Γ_S is the length of the passive loop, L_1. It can be altered by utilizing cables of appropriate lengths.

B. Load Impedance Synthesis

The topology for the proposed load-pull setup is given in Fig. 4. The architecture combines a passive tuner and a passive loop at the DUT output access plane, $Plane-3$. The coupling port of the directional coupler, C_2, is connected to a power meter, in order to monitor and measure the DUT performances in term of output power or linearity during source- and/or load-pull characterization.

From Fig. 4, the following expressions can be derived that relate the travelling waves

$$a_4 = k_4 a_3 \tag{6}$$

$$a_5 = k_5 a_4 \tag{7}$$

$$b_3 = k_6 a_5 \tag{8}$$

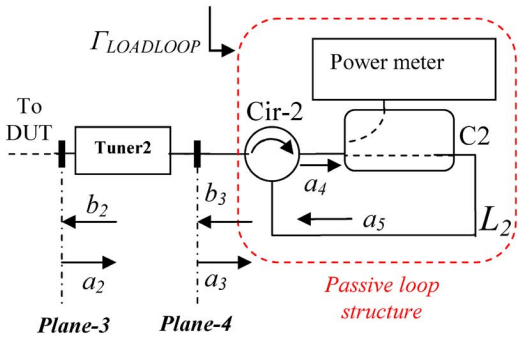

Fig. 4. Proposed load-pull architecture for synthesizing a high load reflection coefficient.

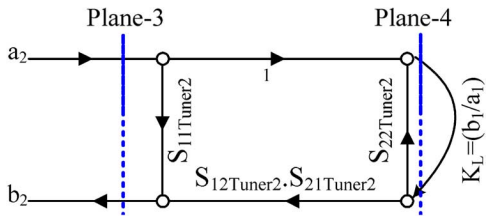

Fig. 5. Error flow model for the proposed load pull architecture.

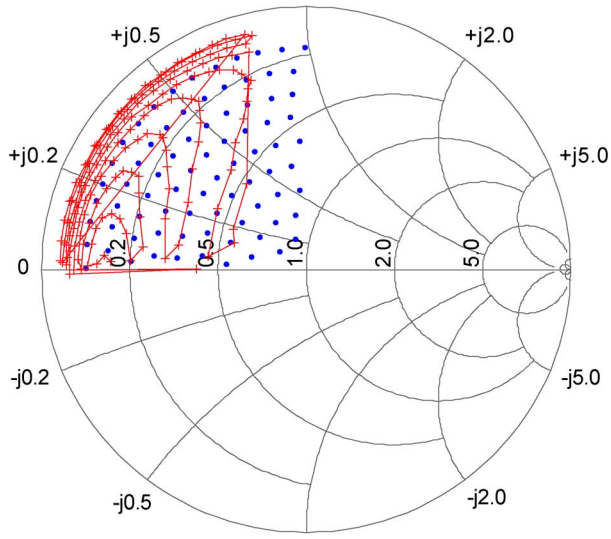

Fig. 6. Higher reflection coefficient synthesis at the DUT input access plane, Plane-2, using the proposed source-pull topology (+), as compared to the reflection coefficient synthesis using a tuner alone (•).

where k_4, k_5 and k_6 are the complex factors dependent on the scattering parameters of the circulator, $Cir-2$, and the directional coupler, $C2$.

Thus, between $Tuner2$ and the passive loop plane, $Plane-4$, the following expression for the mismatch reflection coefficient can be derived

$$\Gamma_{LOADLOOP} = K_L = \frac{b_3}{a_3} = |K_L|.e^{-2j\beta L_2}. \quad (9)$$

The parameter $K_L(= k_4.k_5.k_6)$ is a complex factor that depends on the passive loop structure characteristics, i.e., the transmission factors of coupler $C2$ and circulator $Cir-2$. It is evident from (9) that it is also dependent on the phase velocity, β, of the travelling waves and the length of passive loop, L_2. The topology in Fig. 4 can be represented by the error model given in Fig. 5, which can then be analyzed to obtain the expression for the total reflection coefficient at the DUT output access plane, $Plane-3$, given in

$$\Gamma_L = \frac{b_2}{a_2} = S_{11\mathrm{TUNER2}} + \frac{S_{12\mathrm{TUNER2}}S_{21\mathrm{TUNER2}}K_L}{1 - S_{22\mathrm{TUNER2}}K_L}. \quad (10)$$

Thus, it can be seen from (10) that the total load reflection coefficient, Γ_L, is the reflection coefficient synthesized by $Tuner2$, plus the additional contribution from the passive loop. As the parameter K_L is dependent on the length of the cable, L_2, in the passive loop, it can be altered by employing cables of appropriate lengths.

From the mathematical explanation it is clear that the new source- and load-pull topologies are able to synthesize higher reflection coefficients. Although similar to the popular pre-matching techniques [10], [11], these new architectures have two main benefits over the pre-matching approach: i) there is no need to consider the architecture as two different blocks of the pre-match tuner and the main tuner—the whole tuner and passive loop can be considered as a single impedance controlling element; and, ii) it is substantially more economical.

The next section provides the experimental evaluation of the proposed topologies.

III. Experimental Evaluation of the New Setup

For evaluation purposes, the source- and load-pull topologies were integrated into a nonlinear measurement system [19], while replacing the DUT with a 'Thru' standard. First, the measurement for validation of the performance of the source-pull topology is performed. The reflected and transmitted waves at the input port of the DUT are measured by employing a tuner alone and then again by deploying the proposed source-pull architecture. The synthesized source impedances using the tuner alone and the new source-pull architecture is shown in Fig. 6.

The maximum synthesized reflection coefficient in terms of magnitude, using $Tuner1$ alone, is around 0.85, which is equivalent to a minimum real impedance of 4.05 Ω. The proposed source-pull architecture can synthesize a reflection coefficient of around 0.95, which is equivalent to 1.28 Ω. This is a significant improvement in the performance of the passive tuner and, hence, allows source-pull measurements of highly mismatched devices.

It is also evident that the synthesized impedances are concentrated in a certain region of the Smith chart. By varying the length of the loop, L_1 (i.e., changing the cables connecting $Cir-1$ and $C1$), the location of the synthesized reflection coefficients can be changed.

To evaluate the new load-pull architecture, measurements were carried out to obtain the transmitted and reflected travelling waves at the output access plane, $Plane-3$, of the

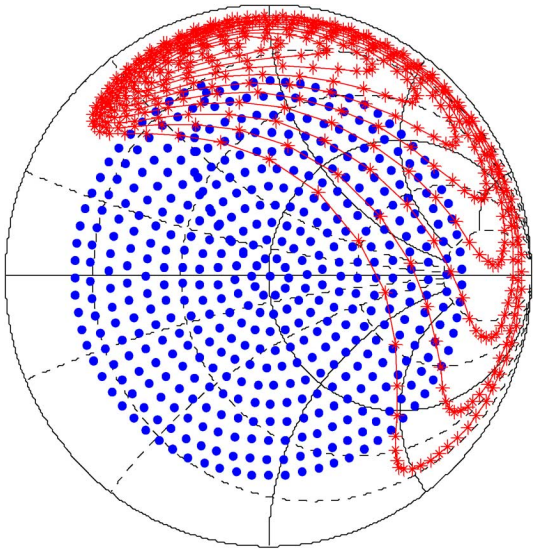

Fig. 7. Higher reflection coefficient synthesis at the DUT output access plane, Plane-3, using the proposed load-pull topology $(*)$, as compared to the reflection coefficient synthesis using a tuner alone.

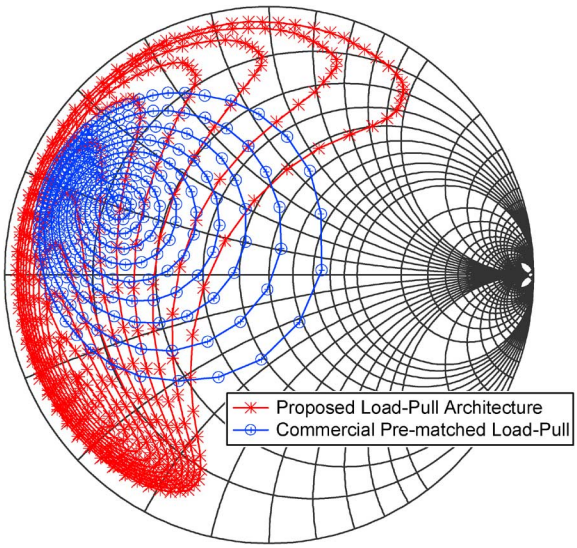

Fig. 8. Comparing the achieved load reflection coefficients of the proposed load-pull topology with those of the state-of-the-art commercial pre-matched load-pull system.

DUT by successively employing the passive tuner and then by employing the proposed architecture. The obtained results are depicted in Fig. 7. It demonstrates that the increase in the achievable load reflection coefficient is relatively significant. While the passive tuner was able to synthesize maximum load reflection coefficients of 0.75, equivalent to 7.14 Ω, the proposed architecture was able to synthesize a load reflection coefficient of 0.97, equivalent to 0.76 Ω.

It is also apparent from (9) that the orientation and location of the load reflection coefficient can be altered by changing the length of cable L_2. To demonstrate this, an experiment was performed with a different setup and employing a different length, L_2. The obtained result is displayed in Fig. 8.

TABLE I
COMPARISON OF THE DIFFERENT TYPES OF EXISTING PASSIVE ARCHITECTURES EMPLOYED FOR SOURCE- AND LOAD-PULL WITH THE DEVELOPED ARCHITECTURES AT CARRIER FREQUENCY OF 2.425 GHz

Passive Source-Pull Techniques	Maximum Achievable Reflection Coefficient (Γ_S)	Passive Load-Pull Techniques	Maximum Achievable Reflection Coefficient (Γ_L)
Passive Tuner (Without Pre-Match)	0.85	Passive Tuner (Without Pre-Match)	0.75
Commercial Passive Tuner (With Pre-Match)	0.88 - 0.92	Commercial Passive Tuner (With Pre-Match)	0.88 - 0.90
Proposed Source-Pull Architecture	0.95	Proposed Load-Pull Architecture	0.97

It was, therefore, experimentally proven that the theoretical formulation in (9) is correct. The new load-pull architecture requires just three different sets of loop lengths, L_2, to cover the whole Smith chart and, hence, provides speedy and precise calibration of the setup as compared to the conventional pre-matching approach, which requires time-consuming calibration of a considerably higher number of positions for the pre-match tuner [11]. Moreover, in the conventional state-of-the art pre-matching technique, the points' density increases around one region, as shown in Fig. 8, close to the edge of the Smith chart, which covers just a small portion [11], thereby, affecting the accuracy of the interpolation algorithms [20]. The proposed approach, however, relocates the impedance points in a larger region on the edge of the Smith chart, which results in a less condensed constellation, hence higher coverage range and more accurate interpolation algorithms. Thus, the proposed architectures also improve the calibration time and the precision in setting the desired reflection coefficients.

It is also important to note that the proposed source- and load-pull structures utilize low loss circulators to close the respective loops. This helps in achieving the maximum source and load reflection coefficients, Γ_S and Γ_L, respectively, for all settings of the passive tuners, as shown in Figs. 6–8.

The data presented in Table I compare the performance of the various types of passive source- and load-pull architectures at a carrier frequency of 2.425 GHz. It is evident that the proposed architectures perform better than the commercial pre-matched tuners. In addition to improved performance the proposed architecture is cost-effective, compared to commercial pre-matched tuners which are considerably more expensive.

It is also evident from Figs. 2 and 4 that the magnitudes of the source and load reflection coefficients, Γ_S and Γ_L, depend on the magnitudes of the waves, b_4 and a_5, respectively. The higher the wave values of b_4 and a_5, the higher are the Γ_S and Γ_L, respectively. The source-pull architecture contains a coupled path of the directional coupler (Fig. 2), which is not the case in the load-pull architecture (Fig. 4). Therefore, a_5 is higher in terms of magnitude than b_4. This leads to a slight higher achievable

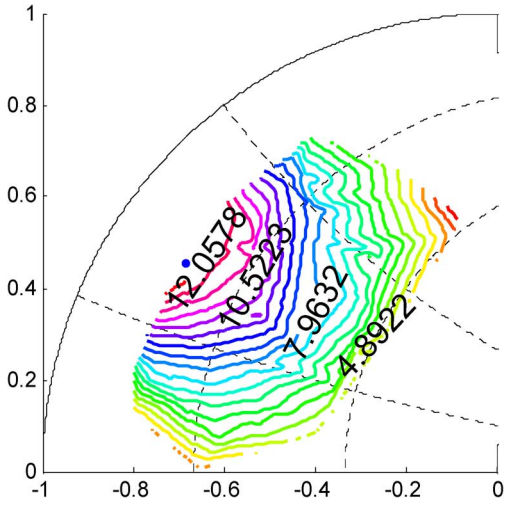

Fig. 9. Fundamental gain contours for source impedance sweep using the passive tuner (Device: FLL107ME).

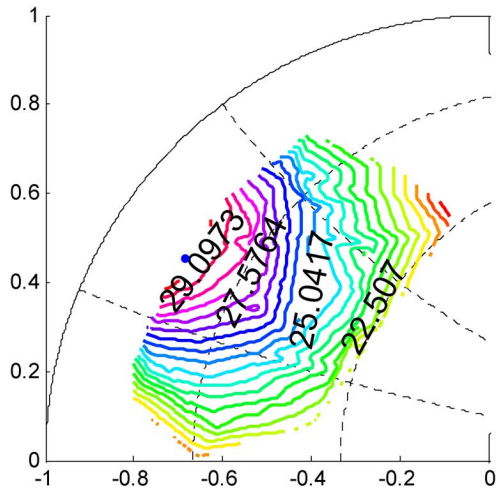

Fig. 11. Fundamental output power contours for source impedance sweep using the passive tuner (Device: FLL107ME).

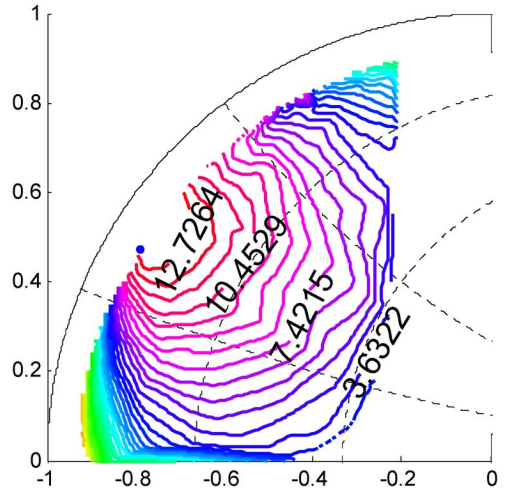

Fig. 10. Fundamental gain contours for source impedance sweep using the proposed source-pull topology (Device: FLL107ME).

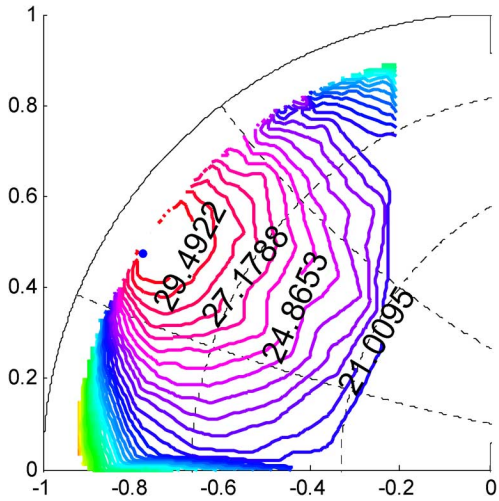

Fig. 12. Fundamental output power contours for source impedance sweep using the proposed source-pull topology (Device: FLL107ME).

Γ_L compared to the achievable Γ_S, as shown in Table I, using the proposed architectures.

IV. Device Characterization Using the New Setup

The proposed impedance synthesis techniques were integrated into a measurement system [19] at the iRadio Lab. Initially, a 1W MESFET from Fujitsu was characterized at a carrier frequency of 2.425 GHz to demonstrate the usefulness of the developed architectures.

As a first step, the optimal load impedance, identified from the device's data sheet, was set using the load tuner, $Tuner2$. Then, the source impedance was swept using the source tuner, $Tuner1$, around the anticipated optimal source impedance.

The gain contours plotted and shown in Fig. 9 demonstrate that the gain showed a progressive nature as the source impedance moved towards the edge of the Smith chart. The proposed source-pull topology (Fig. 2) finds immediate application here. As demonstrated earlier, the source-pull architecture is capable of achieving a reflection coefficient of 0.95; therefore, the optimal load was set, and the source impedance was swept using the new source-pull architecture. The obtained result is given in Fig. 10: an optimal gain of 13.5 dB, which is an improvement of 0.9 dB over the result achieved and a gain of 12.6 dB, using a simple source tuner as shown in Fig. 9.

The impact of better source matching is also evident on the achieved output power contours shown in Figs. 11 and 12. The optimal output power obtained using the passive tuner, $Tuner1$, as the source-pull architecture was 29.6 dBm, whereas the optimal output power obtained using the proposed source-pull topology was 30.3 dBm.

According to Fig. 6, the setup is able to synthesize the source reflection coefficient of the order of 0.95 therefore a 1W device with very low source impedance was selected on purpose to demonstrate the usefulness of the developed system. The optimal source reflection coefficient was determined using the enhanced source-pull architecture and set at 0.92, as mentioned

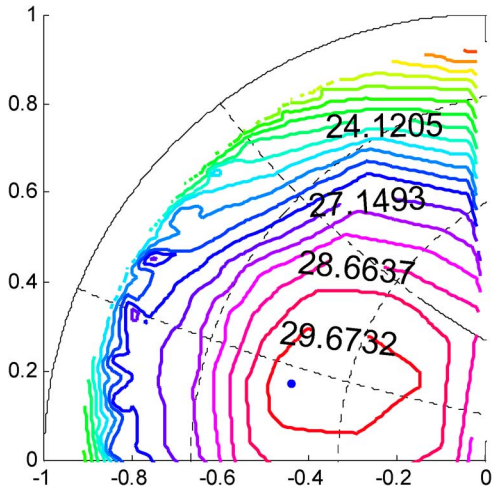

Fig. 13. Load-pull output power contour achieved using the proposed load-pull architecture (Device: FLL107ME).

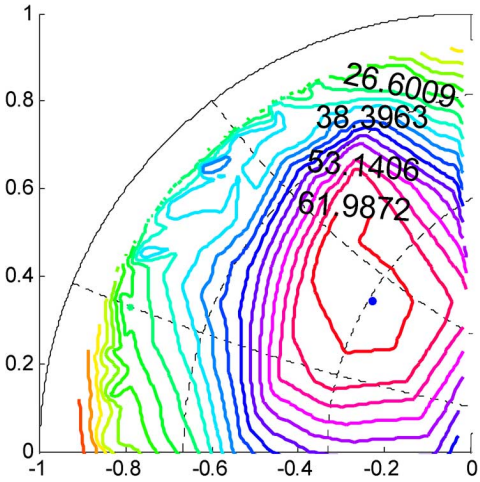

Fig. 14. The obtained load-pull PAE contours using the proposed load-pull architecture. (Device: FLL107ME).

in the source pull measurement above, then the load impedance was swept around the anticipated optimum location in the Smith chart according to the device datasheet. To prevent the device from instability and oscillation the highest load reflection coefficient presented to the DUT was limited to 0.92 despite that the developed system can achieve a load reflection coefficient of 0.97 as shown in Figs. 7 and 8. Moreover, for this chosen device there was no need to present higher load reflection coefficient since the optimal magnitude of load reflection coefficient is around 0.5. The respective achieved results for the output power and power-added efficiency (PAE) are displayed in Figs. 13 and 14, respectively.

The optimal output power when using the proposed loop enhanced source- and load-pull architecture turns out to be 30.6 dBm, as shown in Fig. 13. For this device, the source impedance lies closer to the edge; hence, this source-pull setup is ideal for synthesizing the required impedance. The result in Fig. 14 displays the overall sensitivity of the varying load impedance on the PAE once the source impedance is set at the optimal value. For this device at the chosen bias and frequency conditions, the PAE without the optimal source impedance was around 59%, whereas it improved to 65% once the optimal source impedance was set.

The passive loop in the proposed load- and source-pull architecture is essentially a narrow band structure, due to the limited bandwidth of the used circulator, and therefore it re-injects power only at the fundamental frequency and rejects the harmonic components without passing through the loop. Thus, it provides an enhanced reflection coefficient only at the chosen fundamental frequency. The harmonic terminations in both the cases, with or without the passive loop, remains the same since same isolator was used in both configurations and therefore any increase in the achieved gain and PAE is attributed to the improved fundamental matching conditions at the source and load ports provided by the enhanced source- and load-pull architectures reported in this paper. Although this experiment can be performed using the solutions reported in [7], [10], [11] and [15], those solutions might lead to loop oscillation, are not cost effective or may not be able to synthesize the required input or and output reflection coefficients closer to the border of the Smith chart needed to pull the best performance from the device.

The proposed source-pull topology is also scalable to higher power and higher frequency applications without any problems. This was verified by characterizing a 3W MESFET from Fujitsu at the carrier frequency of 2.5 GHz. The measurement was carried out using both the passive tuner, $Tuner1$, and the proposed topology, respectively. The obtained result gave the optimal gain achievable using the passive tuner, $Tuner1$, as 11.9 dB. The gain contour, for the 3W device, obtained using the proposed source-pull architecture gave an optimal gain of 12.5 dB, which is an improvement of 0.6 dB. Thus, the measurement and characterization demonstrates that the proposed source-pull setup is easily scalable for higher power devices.

V. Summary & Conclusion

This paper gives a comprehensive theoretical and experimental investigation of an innovative loop enhanced source- and load-pull architectures based wholly on using passive components. These passive structures are capable of synthesizing high reflection coefficients and have an advantage over active loop or hybrid active-passive architectures, since they do not suffer from the possibility of oscillations and nonlinearity problems. The implementation cost and calibration time are significantly lower compared to the commercialized systems that provide pre-matching techniques with similar or lower performances.

To the authors' knowledge, there has been no report in literature of such a cost-effective and full passive solution which can synthesize highly reflective reflection coefficients. The proposed architectures would find immediate application in the characterization of microwave devices, particularly in the characterization of high power devices where the load-pull topology needs to synthesize a reflection coefficient nearer to the edge of the Smith chart.

Further application of these architectures may be in the design and characterization of switching-mode power amplifiers where ideally the harmonic impedances need to be terminated at the edge of the Smith chart to achieve short and open conditions. The harmonic load-pull system using the proposed architectures could be based on the triplexer/diplexer based setup such as reported in [16]. The higher reflection coefficient synthesis using the proposed architectures will also enable the "all passive harmonic load-pull" to achieve higher reflection coefficients for the harmonic frequencies in comparison with the existing commercial systems [21], [22]. Obviously the magnitude of reflection coefficient will depend on the insertion loss of the used triplexer/diplexer.

ACKNOWLEDGMENT

The authors would like to acknowledge the technical assistance from the iRadio Lab staff at the University of Calgary.

REFERENCES

[1] R. B. Stancliff and D. P. Poulin, "Harmonic load pull," in *Proc. IEEE MTT-S Symp. Dig.*, Jun. 1979, pp. 185–187.
[2] M. S. Hashmi, F. M. Ghannouchi, S. Bensmida, and M. Helaoui, "Novel Passive Source- and Load-Pull Architecture for High Reflection Factor Synthesis," U.S. Patent Pending.
[3] D.-L. Le and F. M. Ghannouchi, "Multi-tone characterization and design of FET resistive mixers based on combined active source-pull/load-pull techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 9, pp. 1201–1208, Sep. 1998.
[4] G. P. Bava, U. Pisani, and V. Pozzolo, "Active load technique for load-pull characterisation at microwave frequencies," *IEEE Electron. Lett.*, vol. 18, no. 4, pp. 178–180, Feb. 18, 1982.
[5] Y. Takayama, "A new load-pull characterization method for microwave power transistors," in *Proc. IEEE MTT-S Symp. Dig.*, Jun. 1976, pp. 218–220.
[6] M. S. Hashmi, A. L. Clarke, S. P. Woodington, J. Lees, J. Benedikt, and P. J. Tasker, "Electronic multi-harmonic load-pull system for experimentally driven power amplifier design optimization," in *Proc. IEEE MTT-S Symp. Dig.*, Jun. 2009, pp. 1549–1552.
[7] V. Teppati, A. Ferrero, and U. Pisani, "Recent advances in real-time load-pull systems," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 11, Nov. 2008.
[8] P. Bouysse, J. Nebus, J. Coupat, and J. Villotte, "A novel accurate load pull setup allowing the characterization of highly mismatched power transistors," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 2, pp. 327–332, Feb. 1994.
[9] M. S. Hashmi, A. L. Clarke, J. Lees, M. Helaoui, P. J. Tasker, and F. M. Ghannouchi, "Agile harmonic envelope load-pull system enabling reliable and rapid device characterization," *IOP J. Meas. Sci. Technol.*, vol. 21, p. 055109, Apr. 2010.
[10] J. Sevic, "A sub 1 Ω load-pull quarter wave prematching network based on a two-tier TRL calibration," in *Proc. 52nd Autom. RF Techniques Group (ARFTG) Conf. Dig.*, 1998, pp. 73–81.
[11] S. Basu, M. Fennelly, J. E. Pence, and E. Strid, "Impedance Matching Probes for Wireless Applications," Application Note, AR126, Cascade Microtech, 1998.
[12] ""Device Characterization With Harmonic Load and Source Pull," Maury Microwave Corporation, Ontario, CA, Application Note: 5C-044, Dec. 2000.
[13] "Load Pull Measurements on Transistors With Harmonic Impedance Control," Focus Microwave, Montreal, QC, Canada, Aug. 1999.
[14] P. Colantonio, A. Ferrero, F. Giannini, E. Limiti, and V. Teppati, "Harmonic load/source pull strategies for high efficiency PAs design," in *Proc. IEEE MTT-S Symp. Dig.*, Jun. 2003, pp. 1807–1810.
[15] M. Spirito, M. J. Plek, F. van Rijs, S. J. C. H. Theeuwen, D. Hartskeerl, and L. C. N. de Vreede, "Active harmonic load-pull for on-wafer out-of-band device linearity optimization," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, Dec. 2006.
[16] M. S. Hashmi, A. L. Clarke, S. P. Woodington, J. Lees, J. Benedikt, and P. J. Tasker, "Ac accurate calibrate-able multi-harmonic active load-pull system based on the envelope load-pull concept," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 3, pp. 656–664, Mar. 2010.
[17] J. E. Mueller and B. Gyselinckx, "Comparison of active versus passive on-wafer load-pull characterization of microwave MM-wave power devices," in *Proc. IEEE MTT-S Symp. Dig.*, Jun. 1994, pp. 1077–1080.
[18] M. G. El Din, B. Bunz, and G. Kompa, "10W broadband load-pull for GaN/AlGaN characterization," in *Proc. German Microw. Conf.*, Apr. 2005, pp. 185–188.
[19] S. Bensmida, P. Poire, R. Negra, F. M. Ghannouchi, and G. Brassard, "New time-domain voltage and current waveform measurement setup for power amplifier characterization and optimization," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 224–231, Jan. 2008.
[20] C. Roff, J. Graham, J. Sirois, and B. Noori, "A new technique for decreasing the characterization time of passive load-pull tuners to maximize the measurement throughput," in *Proc. 72nd ARFTG Conf.*, Dec. 2008, pp. 92–96.
[21] Focus Microwave, Comparing Harmonic Load-Pull Techniques With Regards to Power Added Efficiency Application Note, May 2007.
[22] G. Simpson, "Harmonic load-pull with high gamma tuners," *Microw. J.*, vol. 51, no. 5, p. 232, May 2008.

Fadhel M. Ghannouchi (S'84–M'88–SM'93–F'07) is currently an iCORE professor and Senior Canada Research Chair at Electrical and Computer Engineering Department of The Schulich School of Engineering of the University of Calgary and Director of Intelligent RF Radio Laboratory .

He held several invited positions at several academic and research institutions in Europe, North America and Japan. He has provided consulting services to a number of microwave and wireless communications companies. His research interests are in the areas of microwave instrumentation and measurements, nonlinear modeling of microwave devices and communications systems, design of power and spectrum efficient microwave amplification systems and design of intelligent RF transceivers for wireless and satellite communications. His research activities led to over 450 publications and 12 patents (5 pending).

Prof. Ghannouchi is a Fellow IET and a Distinguish Microwave Lecturer for IEEE-MTT Society.

Mohammad S. Hashmi (S'04–M'09) was born in India. He received the B.Tech degree from Aligarh Muslim University, India, in 2001 and the M.S. degree from Darmstadt University of Technology, Darmstadt, Germany in 2005, and the Ph.D. degree in non-linear microwave instrumentation from Cardiff University, Cardiff, U.K., in 2009.

He had a postdoctoral stint at Cardiff University in 2009. Since September 2009 he is a postdoctoral fellow at the iRadio Lab, University of Calgary, Canada. Previously he also worked for Philips Semiconductors and Thales Electronics in Germany in the field of RF circuits and systems. His current research interest is in the nonlinear microwave instrumentation, design and linearization of power amplifiers for mobile and satellite applications, and design of microwave circuits and systems for dual-band applications. His research activities have led to over 25 publications and 2 patents (pending).

Dr. Hashmi was the recipient of ARFTG Microwave Measurement Fellowship for the year 2008.

Souheil Bensmida received the DEA degree in electronics and instrumentation from the University of Pierre and Marie Curie Paris 6, Paris, France, in 2000, and the Ph.D. degree in electronics and communications from the Ecole Nationale Supérieure des Télécommunications (ENST), Paris, France, in 2005.

He was a Postdoctoral Fellow between October 2006 and September 2008 at the iRadio Laboratory, University of Calgary, AB, Canada. He is now research associate at University of Bristol, Bristol, U.K. His research interest is the nonlinear characterization and linearization of power amplifiers for mobile and satellite applications and microwave instrumentation. His research activities have led to over 30 publications and 2 patents (pending)

Mohamed Helaoui (S'06–M'09) received the M.Sc. degree in communications and information technology from École Supérieure des Communications de Tunis, Tunisia, in 2003 and the Ph.D. degree in electrical engineering from the University of Calgary, Calgary, AB, Canada, in 2008.

His current research interests include digital signal processing, power efficiency enhancement for wireless transmitters, switching mode power amplifiers, and advanced transmitter design for software defined radio applications. His research activities have led to over 40 publications and 4 patents (pending).

Dr. Helaoui is a member of the COMMTTAP chapter in the IEEE southern Alberta section.