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Name: Jawar Singh **Date of Birth**: 15th August 1977 **Nationality**: Indian
Permanent Address: 61, Maya Mansion, Gaytri Vihar, Gwalior, MP, India, 474011
Education:

1. Doctor of Philosophy (Ph.D.): submitted
   Department of Computer Science, University of Bristol, UK
   Area of Research: VLSI, Low power systems, Nano-CMOS and TFET SRAMs, Process variation and fault tolerant SRAM design, Statistical analysis of process variations in Nano-CMOS devices.
2. Master of Technology (M.Tech.): July 1999 to July 2001
   First Division
   Department of Electrical Engineering, Indian Institute of Technology (IIT) Roorkee, India.
   Specialization: Measurement and Instrumentation
3. Bachelor of Engineering (B.E): June 1995 to July 1999
   First Division
   Department of Electrical Engineering, MITS, Gwalior, India
   Specialization: Electrical Engineering

Work Experience:

1. Lecturer: July 2001 to January 2007
   Co-Investigator: An AICTE sponsored project, "Computer Aided Analysis and Diagnosis of Hansen's Disease", Total Cost: Rs. 1.1 Million
   Department of Electrical Engineering,
   Madhav Institute of Technology & Science (MITS), Gwalior, India.
2. Teaching Assistant:
   (a) CMOSM30125: Fault Tolerant Computer Design
   (b) COMSM1302: Overview of Computer Architecture
   Department of Computer Science, University of Bristol, UK.

Skills:

1. Programming languages: ALP, C, MATLAB
2. Hardware description languages: VHDL and Verilog
3. EDA Tool Suits: Synopsys (HSPICE and Sentaurus TCAD), Cadence (Virtuoso, Spectre) and Modelsim

Awards and Scholarships:

1. GATE 1999, Government of India: For M. Tech.
2. National Overseas Fellowship, Government of India: For Ph.D.
3. Worldwide University Network Fellowship, Government of UK: For research (four months) at the Pennsylvania State University, USA.

Invited Talk:

1. ESRC, 08 Oct. 09, ARM, Cambridge, UK, on "Low Power Process Variation Aware SRAM Bitcell Designs"

References:

1. Dhiraj K. Pradhan, Professor
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Research Interest:

Main focus of research is low power System on Chip (SoC) applications in which Static Random Access Memories (SRAMs) are omnipresent. Also exploring the alternative devices to replace the traditional CMOS, since aggressive scaling of CMOS technology for increased performance and lower costs have pushed the devices to their physical limits. Aggressive scaling of CMOS technology presents a number of distinct challenges for embedded memory fabrics. Owing to the scaling effects, the current designs methodologies and topologies of the SRAM design may fail to provide the expected yield. Thus, the need of time is to find out the new design methodology and topology that can meet the future challenges.

Hence, two SRAM bitcell designs for single port and multiport cache architectures were proposed using conventional COMS devices. The proposed designs were simulated and tested under the nano-regime challenges such as process variability. Sensitivity of the process variations and susceptibility to soft-errors were compared with the existing design, simulation results show that proposed designs have better noise margins and stability. However, proposed designs show the less power dissipation and silicon area overhead with increasing number of I/O ports. We have also filed the patent of both the SRAM bitcell designs.

As an alternative device to replace the traditional CMOS, I have started exploring and characterization of the emerging technologies such as Tunnel-fets (TFETs) which have strong potential to replace the traditional MOSFETs for sub-threshold leakage reduction because of steep sub-threshold slope. Since analytical or compact SPICE models for TFETs are not available, we have built a behavioral model for circuit simulation. Developed model accurately captures the higher Miller capacitance effect and comply with TCAD simulation results with a great degree of accuracy. Because of unidirectional feature of the TFETs, implementation of SRAM bitcell is a bit non-trivial than CMOS while keeping the minimum number of devices. Hence, a six transistor (6T) SRAM bitcell is proposed with improved read and write margins compared to 6T CMOS SRAM bitcell. Patent filing application of this design is under development. However, implementation of logic gates with TFETs does not possess any difficulty due to unidirectional feature. The proposed 6T TFET SRAM bitcell shows the more than 100 times less static power dissipation as compared to its counterpart 6T SRAM bitcell. In this study, 30nm proposed TFET and 32nm Predictive Technology Model were used.

Patents

1. **Jawar Singh**, Dhiraj K. Pradhan and Jimson Mathew; "Static Random Access Memory", Ref. No. P110161US/JMR; Filed in July 2008, USA.
2. **Jawar Singh**, Dhiraj K. Pradhan and Simon Hollis, "An Area Optimal Multi-Port Six Transistor Static Random Accesses Memory (M6T-SRAM)", Ref. No. 0902683.2 Filed in Feb 2009, UK.

Recent Publications

Refereed Journal:

1. **Jawar Singh**, Dhiraj K. Pradhan, Simon Hollis and Saraju P. Mohanty, "*A single ended 6T SRAM cell design for ultra-low-voltage applications*" IEICE, Electronics Express *Vol. 5 (2008), No. 18 pp. 750-755.*

Refereed Conferences (Blind review):

1. Andrew Ricketts, **Jawar Singh**, VijayKrishnan Narayan, Dhiraj K. Pradhan, "Investigating the Impact of NBTI on Different Power Saving Cache Strategies" IEEE International Conference, DATE, 2010, Germany, (Under review).
2. S. Mookerjea, D. Mohata, R. Krishnan, **Jawar Singh**, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu and S. Datta, "Experimental Demonstration of 100nm Channel Length In0.53Ga0.47As-based Vertical Inter-band Tunnel Field Effect Transistors (TFETs) for Ultra Low-Power Logic and SRAM Applications", To appear in the proceedings of IEEE International Electron Devices Meeting (IEDM), December, Baltimore, 2009.
3. **Jawar Singh**, Ramakrishnan Krishnan, Saurabh Mookerjea, Suman Datta, VijayKrishnan Narayan, Dhiraj K. Pradhan, "A Novel Si-Tunnel FET based SRAM Design for Ultra Low-Power 0.3V VDD Applications" To appear in the proceedings of IEEE International Conference, ASP-DAC, January 2010, Taiwan.
4. **Jawar Singh**, Dhiraj K. Pradhan, Simon Hollis, Saraju P. Mohanty and J. Mathew "Single Ended 6T SRAM with Isolated Read-Port for Low-power Embedded Systems" IEEE International Conference, DATE 09, Nice, France, 20-24 April, 2009.
5. **Jawar Singh,** Dhiraj K. Pradhan, Jimson Mathew and Saraju P. Mohanty, Single Ended Static Random Access Memory for Low-Vdd, High Speed Embedded Systems" 22nd International Conference on IEEE VLSI Design, 5th-9th January 2009, India.

6. **Jawar Singh**, Jimson Mathew, Saraju P. Mohanty and Dhiraj K. Pradhan, "A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies" 21st IEEE International SOCC Conference, California, USA Sep. 17-20, 2008.
7. **Jawar Singh**, Jimson Mathew, Saraju P. Mohanty and Dhiraj K. Pradhan, "Failure Analysis for Ultra Low Power Nano-CMOS SRAM Under Process Variations" 21st IEEE International SOCC Conference, California, USA Sep. 17-20, 2008.
8. **Jawar Singh**, Jimson Mathew, Saraju P. Mohanty and Dhiraj K. Pradhan, "Process Variation Induced Read Failure Tolerant Low Power SRAM Cell Design", 20th IEEE International Symposium on Circuits and Systems, Seattle, Washington, USA, 18-21 May 2008.
9. 7. J. Mathew, **Jawar Singh**, A.M Jabir and Dhiraj K. Pradhan, "Fault Tolerant Bit Parallel Finite Field Multipliers using LDPC Codes", 20th IEEE International Symposium on Circuits and Systems, Seattele, Washington, USA, 18-21 May 2008.
10. J. Mathew, **Jawar Singh**, Taleb, A.A and Dhiraj K. Pradhan, "Fault Tolerant Reversible Finite Field Arithmetic Circuits", 20th IEEE International Symposium on Circuits and Systems, Seattele, Washington, USA, 18-21 May 2008.
11. Su, Y.X.; Mathew, J.; **Jawar Singh;** Pradhan, D. K.; "Pseudo parallel architecture for AES with error correction" 21st IEEE International SOCC Conference, California, USA Sep. 17-20, 2008.
12. **Jawar Singh**, Jimson Mathew, Saraju P. Mohanty and Dhiraj K. Pradhan "Statistical Analysis of Steady State Leakage Currents in Nano-CMOS Devices" IEEE NORCHIP 2007, pp. 1-4.
13. **Jawar Singh** , J. Mathew, M. Hosseinabady, D. K. Pradhan, "Single Event Upset Detection and Correction" , 10th IEEE International Conference on Information Technology (ICIT '07) 18th to 20th Dec. 2007, Rourkela, INDIA.
14. Babita R.Jose, P. Mythili, **Jawar Singh**, Jimson Mathew"A Triple-Mode Sigma-Delta Modulator Design for Wireless Standards" 10th IEEE International Conference on Information Technology (ICIT '07) 18th to 20th Dec. 2007, Rourkela, INDIA.

(Jawar Singh)
5 November 2009