# Analog Circuit Design (ACD) – ECE520

# Home Assignment - 5

Total Marks: 10 Submission Deadline: 01.11.2013

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**Instructions:**

- **Answer all the questions.**
- **Please adhere to institute's plagiarism policy.**
- **Submit before 5:00pm on the submission day. No late submission allowed.**

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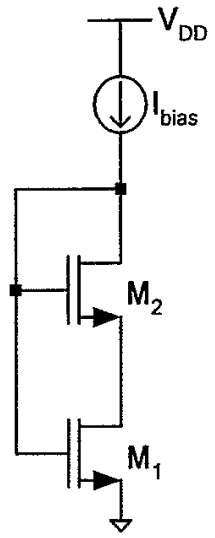
**Q1. [3 marks]** In the following circuit assume that the bulk of the two NFETs are connected to the ground, $\lambda = 0$, and $\Upsilon \neq 0$.

(a) What is the region of operation of transistor $M_1$?

(b) Does the region of operation of $M_1$ depend on the relative sizing of the transistors?

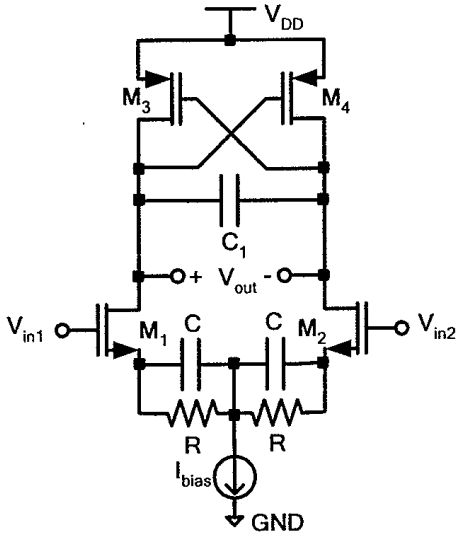
(c) Assume that the $\mathbf{I_{bias}}$ and the transistor sizes are chosen such that the drain voltage of $M_1$ is very close to zero. Give an expression for the output resistance of the circuit seen at the drain of $M_2$ in terms of circuit parameters.




**Q2. [3 marks]** Assuming that the following circuit is symmetrical and $\Upsilon = 0$: and $\lambda \neq 0$:

- Find the expression for the small-signal differential voltage gain [ $V_{out} / (V_{in1} - V_{in2})$ ] of the circuit at very low frequencies.
- What is the gain of the circuit at very high frequencies?

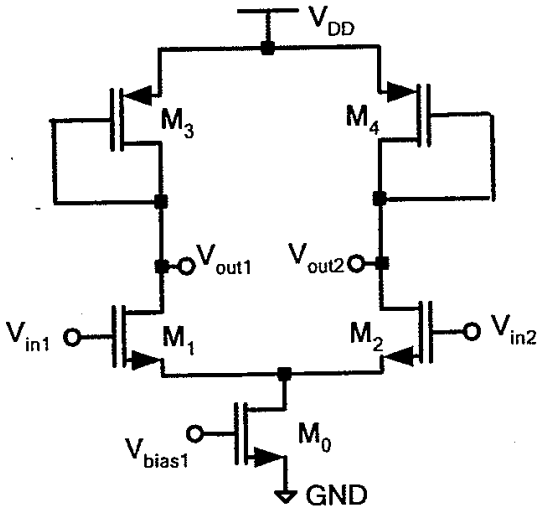
**Note:** In this question neglect all other capacitances that are not shown in the circuit




**Q3. [4 marks]** Design a symmetric differential amplifier based on the topology shown below with the following design specifications:

- $V_{DD}$ = 1.8V
- Total power consumption of 1.8mW
- Output DC level of 0.9V
- Total gain of 5
- L = 0.4µm for all devices

Assume that the minimum required voltage at the drain of $M_0$ to keep it in saturation is 0.2V.




The technology parameters are:

$\lambda$(NMOS) = 0, $\lambda$(PMOS) = 0, $\Upsilon$=0, $V_{DD}$ = 1.8V, $V_{TN} = |V_{TP}|$ = 0.4V,

$\mu_n C_{ox}$ = 1mA/V$^2$, $\mu_p C_{ox}$ = 0.5 mA/V$^2$

(a) Find $V_{bias1}$, and all the transistor widths

(b) Find the minimum and maximum allowable input common-mode (input DC) levels.