Analog Circuit Design (ACD) – ECE520

Home Assignment - 2
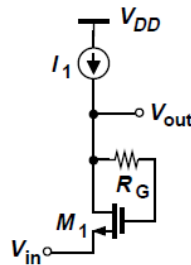
Total Marks: 10   Submission Deadline: 16.09.2013
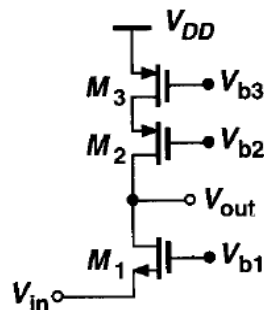
Instructions:
- **Answer all the questions.**
- **Please adhere to institute's plagiarism policy.**
- **Submit before 5:00pm on the submission day. No late submission allowed.**

Q1. [2.5 marks] Calculate the voltage gain of the circuit shown below and comment on the type of configuration of the circuit

Q2. [2.5 marks] Calculate the voltage gain of the circuits shown below:

Q3. [2 marks] The MOS cascode shown below must provide a voltage gain of 200. If $\mu_n c_{ox}=100\mu A/V^2$ and $\lambda=0.1$ for both transistors, determine the required value of $(W/L)_1=(W/L)_2$
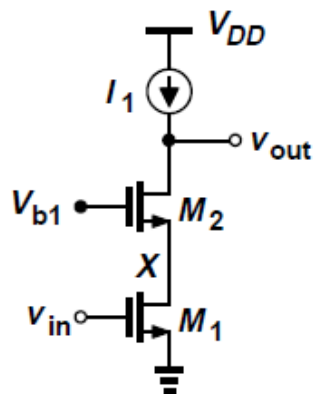
Q4. [3 marks] The MOS cascode of the circuit below must provide a bias current of 0.5 mA with an output impedance of at least 50k. If $\mu_n C_{ox} = 100\mu A/V^2$ and $(W/L) = 20/0.18$ for both transistors, compute the maximum tolerable value of λ.