Analog Circuit Design (ACD) – ECE520

Home Assignment - 1

Total Marks: 10 Submission Deadline: 05.09.2013

Instructions:

- **Answer all the questions.**
- **Please adhere to institute's plagiarism policy.**
- **Submit before 5:00pm on the submission day. No late submission allowed.**

Q1. The CS stage of Fig.1 must provide a voltage gain of 10 with a bias current of 0.5 mA. **[1.5 marks]**

a). Compute the required value of $\mathbf{(W/L)_1}$

b). Calculate the required value of $\mathbf{V_b}$ if $\mathbf{(W/L)_2 = 20/0.18}$

Assume λ_1=0.1 V^{-1} and λ_2=0.15V^{-1}.

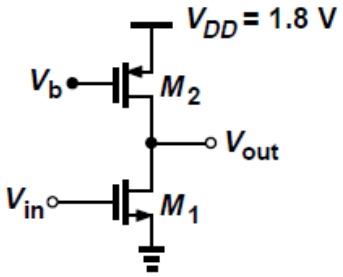


Fig.1

Q2. Determine the voltage gain of the stage shown in Fig. 2. Assume $\lambda \neq 0$. **[1.5 marks]**

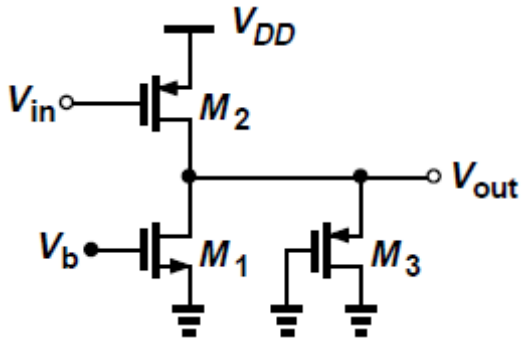


Fig.2

Q3. A MOSFET when used as an amplifier is typically operated in the saturation region, and a large intrinsic gain (g_m/g_d) is desirable. **[1.5 marks]**

(a) Explain why there is an optimal gate bias voltage (V_{GS}) to maximize the MOSFET transconductance g_m.

(b) Does intrinsic gain degrades with decreasing channel length L. Give reason for your answer.

Q4. If you want your design to be "Body Effect" free, which type of MOSFET will you prefer and why? **[0.5 marks]**

Q5. The CS stage of Fig. 4 carries a bias current of 1mA. If R_D = 1K Ω and λ =0.1V^{-1}, compute the required value of (W/L) for a gate voltage of 1V. What is the voltage gain of the circuit? **[1.5 marks]**

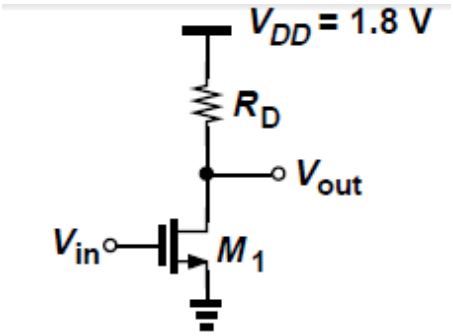
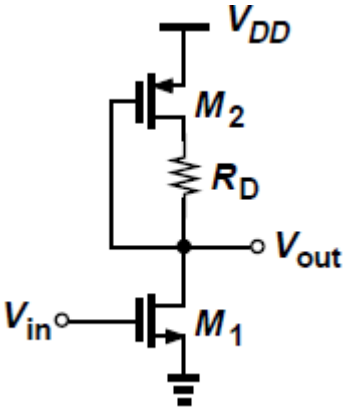


Fig.4

Q6. Assuming all MOSFETs are in saturation, calculate the small signal voltage gain of the following circuit: **[1.5 marks]**



Q7. Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit below. We know that circuit samples free from this error, exhibit V_{gs}=V_{ds} whereas defective samples exhibit V_{gs} =V_{ds} +V_{th}. Determine the values of (W/L) and Rp. **[2 marks]**