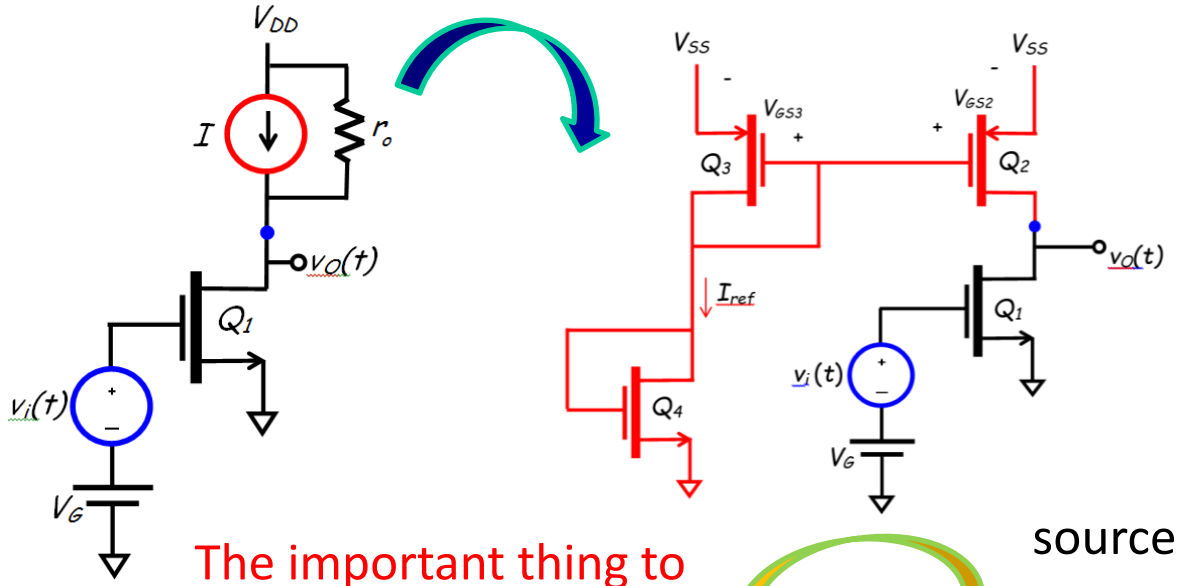
ECE315 / ECE515

Lecture – 8 **Date: 05.09.2016**

- CS Amplifier with Constant Current Source
- Current Steering Circuits
- CS Stage Followed by CG Stage
- Cascode as Current Source
- Cascode as Amplifier

CS Amplifier with Constant Current Source



Transistors Q_2, Q_3, and Q_4 form the **current mirror** that acts as the **current source**. Note that transistor Q_4 is an **enhancement load**—it acts as the **resistor** in the current mirror circuit.

The important thing to realize when analyzing **this** circuit is that the gate-to-source voltage for transistors Q_2, Q_3, and Q_4 are **DC values**!

source resistance r_o of this current source → requires the **small-signal analysis** → there are **four** (count em') transistors in this circuit, determining the small-signal circuit must **take forever**! → the answer is actually a **NO**.

??

A: In other words, the small signal voltages v_{gs} for each transistor are equal to **zero**:

$$v_{gs2} = v_{gs3} = v_{gs4} = 0$$

CS Amplifier with Constant Current Source (contd.)

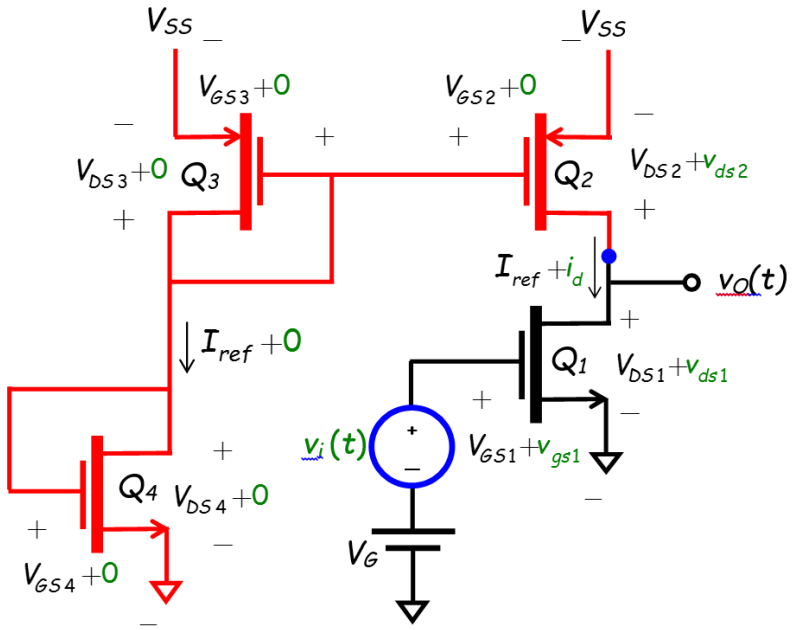
Q: But doesn't the small-signal source $v_i(t)$ **create** small-signal voltages and currents **throughout** the amplifier?

A: For **some** of the circuit yes, but for **most** of the circuit no!

Note that for transistor $\mathbf{Q_1}$ there will be small-signal voltages $v_{gs1}(t)$ and $v_{ds1}(t)$, along with $i_{d1}(t)$. Likewise for transistor $\mathbf{Q_2}$, a small-signal voltage $v_{ds2}(t)$ and current $i_{d2}(t)$ will occur.

But, for the remainder of the voltages and currents in this circuit (e.g., V_{DS4}, V_{GS2} , I_{D3}), the small-signal component is zero!

CS Amplifier with Constant Current Source (contd.)



Q: But wait! **How** can there be a small-signal **drain current** $i_{d2}(t)$ through transistor Q_2, **without** a corresponding small-signal $v_{gs2}(t)$ **gate-to-source voltage**?

A: Transistor Q_2 is **the** important device in this analysis.

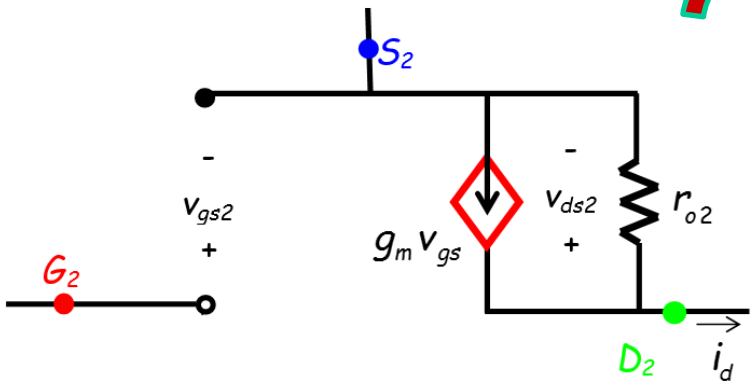
- Note its gate-to-source voltage is a **DC value** (no small-signal component, $v_{gs2}(t) = 0$), yet there **must** be (by KCL) a **small-signal** drain current!
- This is a case where we **must** consider the **MOSFET output resistance** r_{o2}. The small-signal drain current for a **PMOS** device is:

$$i_{d2} = g_{m2}\, v_{gs2} - \frac{v_{ds2}}{r_{o2}}$$

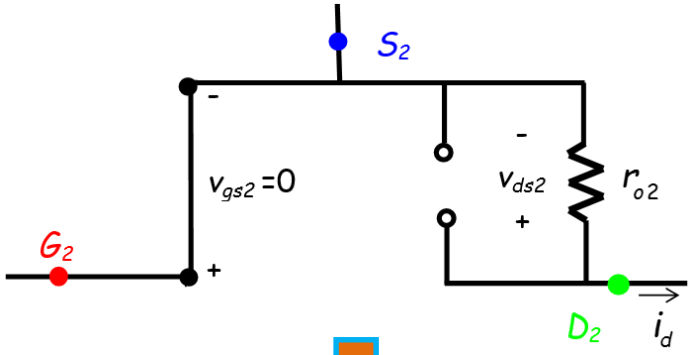
- Since $v_{gs2} = 0$, this equation **simplifies** to: $i_{d2} = -\dfrac{v_{ds2}}{r_{o2}}$

CS Amplifier with Constant Current Source (contd.)

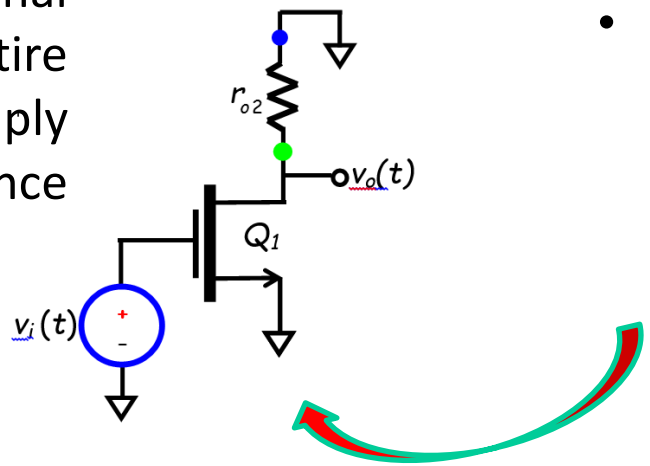
- Equivalently, the **small-signal PMOS model** is:



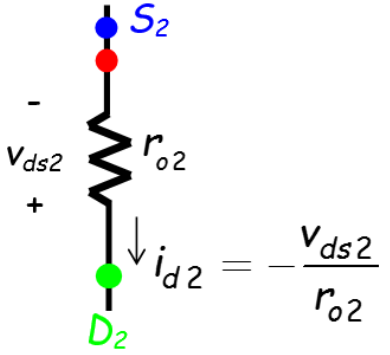
- Thus for $v_{gs2} = 0$, the small-signal model becomes:



- Thus, the small-signal model of the entire current mirror is simply the output resistance of the MOSFET Q_2 !



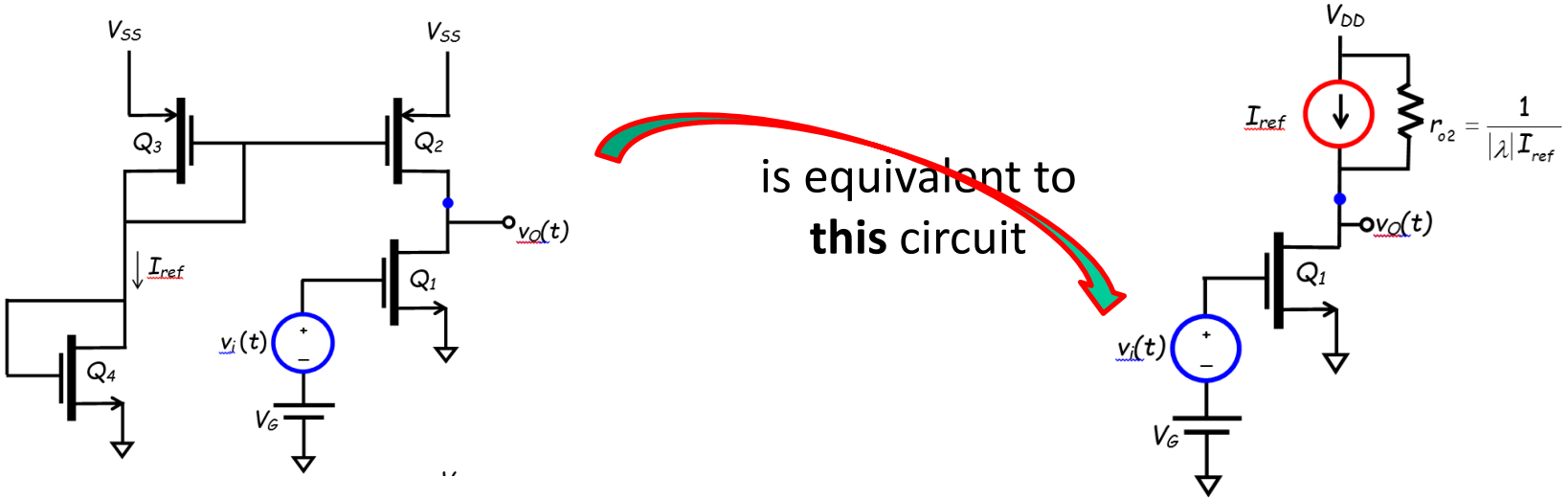
- Or, simplifying further:



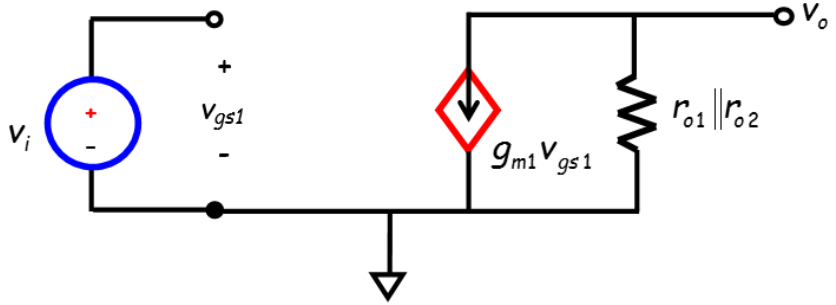
CS Amplifier with Constant Current Source (contd.)

It is evident that the output resistance of the current mirror is simply equal to the output resistance of MOSFET Q_2 !!!!

$$r_o = r_{o2}$$



- The resulting small-signal circuit of this amp is:



- the small signal **voltage gain** is:

$$A_v = -g_{m1}\ r_{o1} \| r_{o2} = 2\sqrt{K_1}\sqrt{I_{ref}}\ r_{o1} \| r_{o2}$$

CS Amplifier with Constant Current Source (contd.)

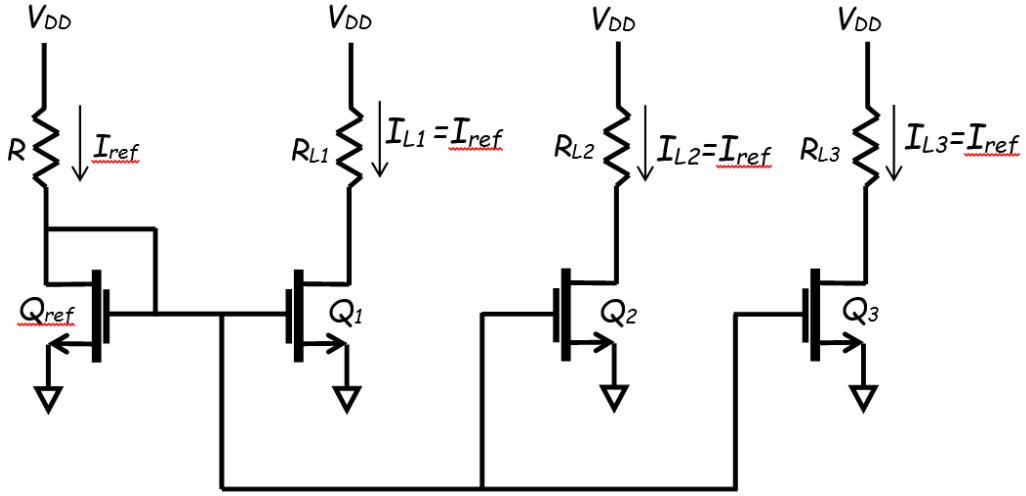
- Note **this** result is **far different** (i.e., larger) than the result when using the **enhancement load** for R_D:

$$A_v = -\sqrt{\frac{K_1}{K_2}}$$

- However, we find that the **output** and **input** resistances of this amplifier are the **same** as with the enhancement load:

$$R_i = \infty \qquad R_o = r_{o1} \| r_{o2}$$

- A current mirror may consist of **many** MOSFET current sources!



This circuit is particularly useful in integrated circuit design, where **one** resistor R is used to make **multiple** current sources.

Q: What if we want to make the sources have **different** current values? Do we need to make **additional** current mirrors?

Current Steering Circuits

A: NO!!

- Recall that the current mirror simply ensures that the gate to source voltages of **each** transistor is **equal** to the gate to source voltage of the **reference**:

$$V_{GS}^{ref} = V_{GS1} = V_{GS2} = V_{GS3} = \cdots$$

- Therefore, **if** each transistor is identical (i.e., $K_{ref} = K_1 = \cdots$, and $V^{ref}{}_T = V_{T1} = V_{T2} = \cdots$) then:

$$I_{ref} = K_{ref}\left(V_{GS}^{ref} - V_T^{ref}\right)^2 = K_n\left(V_{GSn} - V_{Tn}\right)^2 = I_{Dn}$$

In other words, **if** each transistor Q_n is **identical** to Q_{ref}, then each current I_{Dn} will **equal** reference current I_{ref}.

- **But,** consider what happens if the MOSFETS are not identical. Specifically, consider the case where $K_n \neq K_{ref}$ (but $V_{Tn} = (V_T)^{Ref}$).

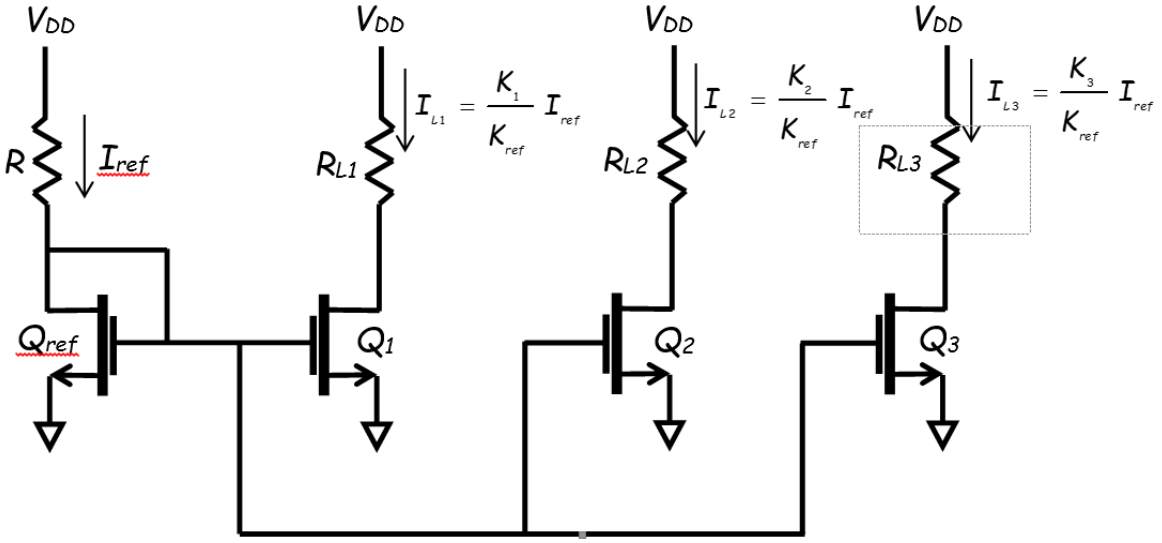
- In such a scenario the drain current I_{Dn} will now be:

$$I_{Dn} = K_n\left(V_{GSn} - V_{Tn}\right)^2 = K_n\left(V_{GS}^{ref} - V_T^{ref}\right)^2 = K_n\left(\frac{I_{ref}}{K_{ref}}\right) = \left(\frac{K_n}{K_{ref}}\right) I_{ref}$$

The drain current is a scaled value of I_{ref}!

Current Steering Circuits (contd.)

For example, if K_1 is twice that of K_{ref} (i.e., $K_1 = 2K_{ref}$), then I_{D1} will be twice as large as I_{ref} (i.e., $I_{D1} = 2I_{ref}$).

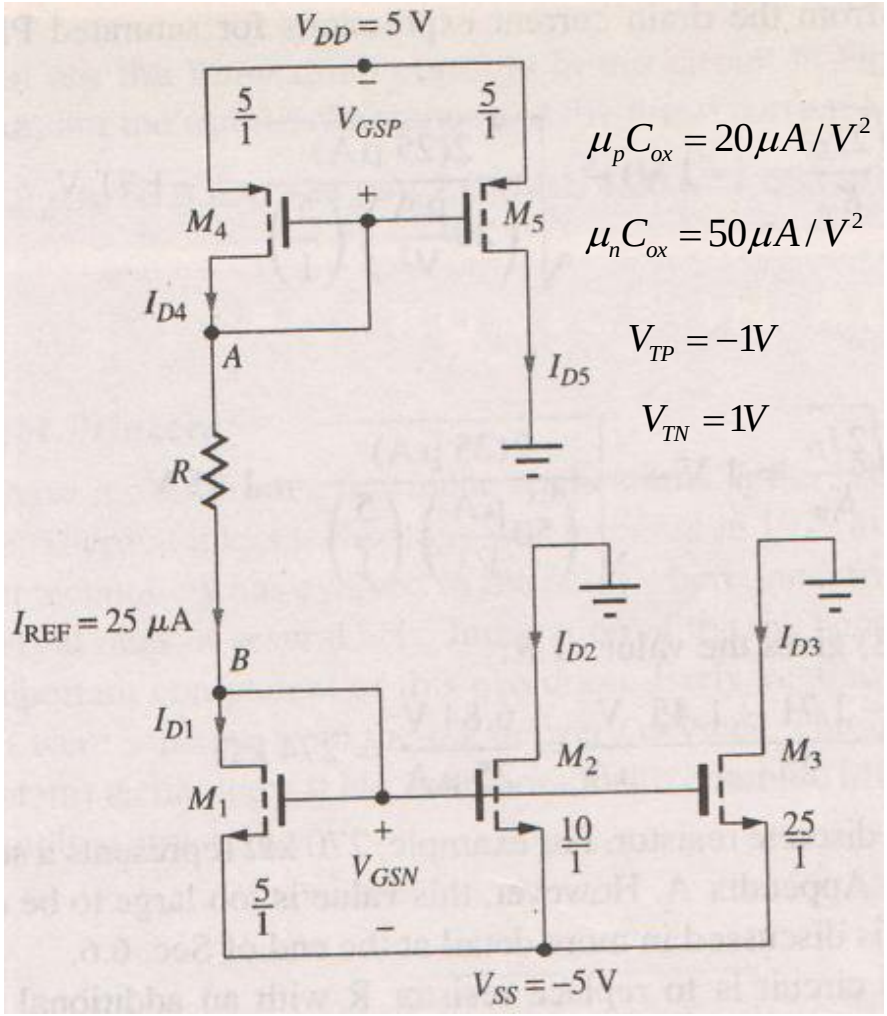


$$\frac{K_n}{K_{ref}} = \frac{\left(W/L\right)_n}{\left(W/L\right)_{ref}}$$

From the standpoint of integrated circuit design, we can change the value of *K* by modifying the MOSFET channel **width-to-length ratio** (*W*/*L*) for each transistor.

Example-1

- Determine all the currents in the following and find the value of R



$\mu_p C_{ox} = 20\mu A/V^2$

$\mu_n C_{ox} = 50\mu A/V^2$

$V_{TP} = -1V$

$V_{TN} = 1V$

$$I_{D2} = I_{REF}\frac{(W/L)_2}{(W/L)_1}$$

$$= 25\mu A * \frac{10/1}{5/1} = 50\mu A$$

$$I_{D3} = I_{REF}\frac{(W/L)_3}{(W/L)_1} = 125\mu A$$

$$I_{D4} = I_{REF} = 25\mu A$$

$$I_{D5} = I_{D4}\frac{(W/L)_5}{(W/L)_4} = 25\mu A$$

Example-1 (contd.)

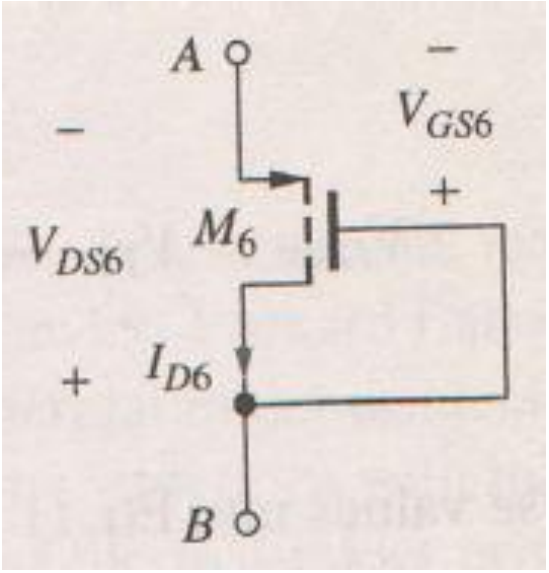
$$R = \frac{+5-(-V_{GSP})-V_{GSN}-(-5)}{I_{REF}}$$

$$\Rightarrow R = \frac{10+V_{GSP}-V_{GSN}}{I_{REF}}$$

$$V_{GSP} = V_{TP} - \sqrt{\frac{2I_{D4}}{\mu_p C_{ox}(W/L)_4}}$$

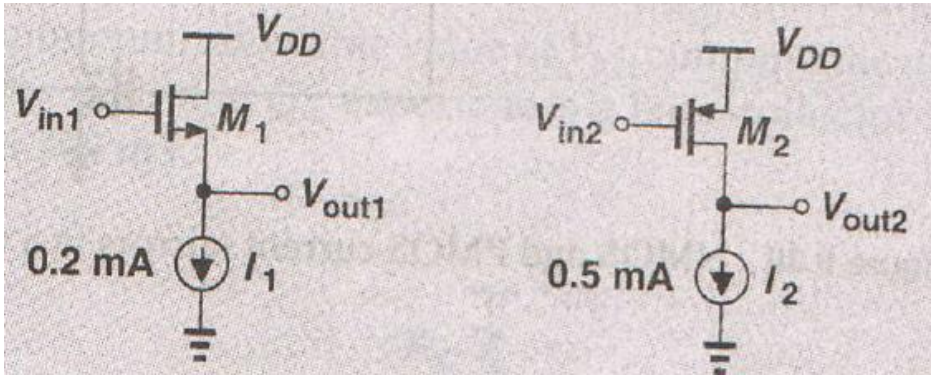
$$V_{GSN} = V_{TN} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W/L)_1}}$$

- The resistor R can be replaced by an active load such as the PFET shown here → what will be its W/L?



Example-2

- An integrated circuit employs the following CD and CS stages. Design an NMOS type current mirror that produces I_1 and I_2 from a 0.8mA reference.

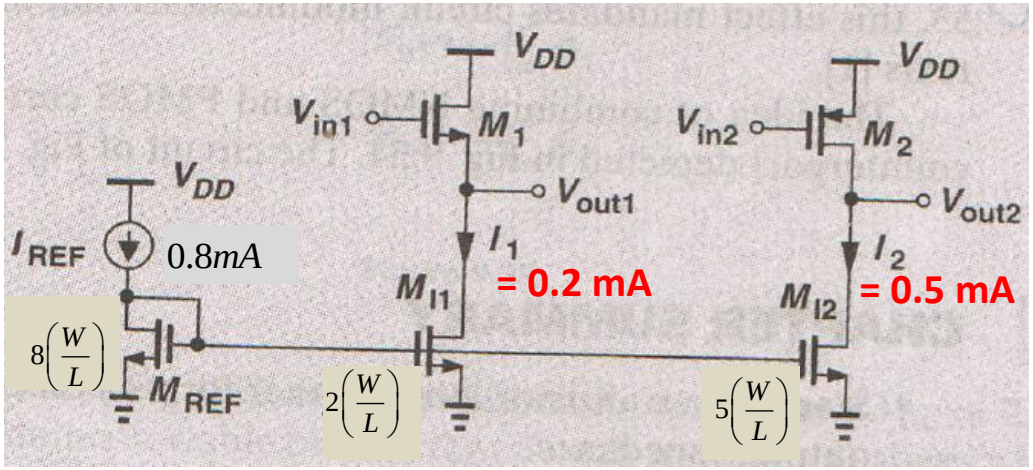


- Required current for CD stage is 0.2 mA, hence mirror equation gives:

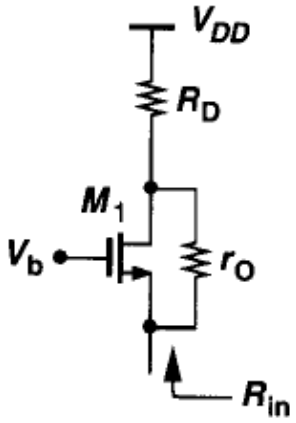
$$\frac{I_{DMI1}}{I_{REF}} = \frac{(W/L)_{MI1}}{(W/L)_{REF}} \quad \Rightarrow \frac{0.2}{0.8} = \frac{(W/L)_{MI1}}{(W/L)_{REF}}$$

They are in the ratio of 2 to 8

- Similarly, for CS stage the ratio is 5 to 8



Common Gate Stage



$$\therefore R_{in} = \frac{R_D + r_o}{1 + (g_m + g_{mb})r_o} \approx \frac{R_D}{(g_m + g_{mb})r_o} + \frac{1}{(g_m + g_{mb})}$$

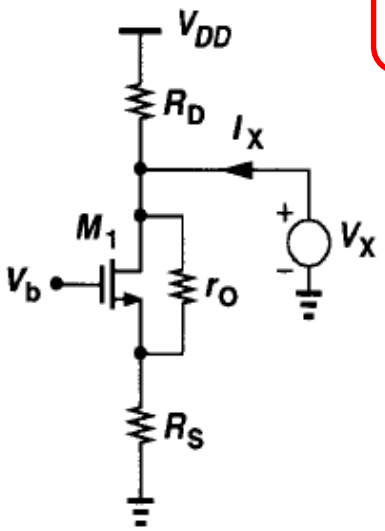
- **Case-I:** $R_D = 0$

$$R_{in} = \frac{V_X}{I_X} = \frac{r_o}{1 + (g_m + g_{mb})r_o}$$

- **Case-II**: R_D is an ideal current source ie, $R_D \rightarrow \infty$

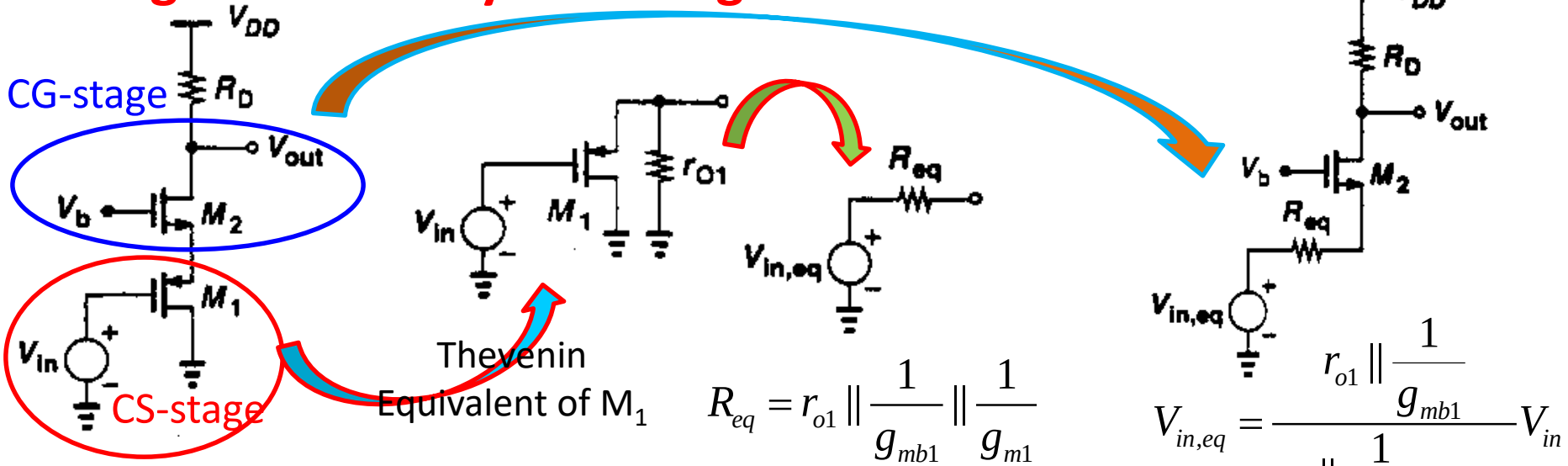
$$R_{in} \rightarrow \infty$$

the input impedance of common-gate stage is low only if the load impedance connected to the drain is low



$$R_{out} = \frac{V_X}{I_X} = \left\{\left[1 + (g_m + g_{mb})r_o\right]R_S + r_o\right\} \| R_D$$

CS-stage followed by a CG-stage



$$R_{eq} = r_{o1} \| \frac{1}{g_{mb1}} \| \frac{1}{g_{m1}}$$

$$V_{in,eq} = \frac{r_{o1} \| \frac{1}{g_{mb1}}}{r_{o1} \| \frac{1}{g_{mb1}} + g_{m1}} V_{in}$$

- Use the CG stage expression to obtain the small signal voltage gain as:

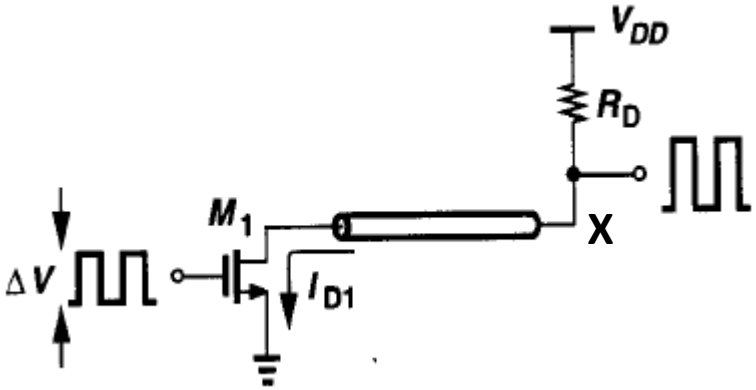
$$\frac{V_{out}}{V_{in}} = A_v = \frac{(g_{m2} + g_{mb2}) r_{o2} + 1}{r_{o2} + \left[1 + (g_{m2} + g_{mb2}) r_{o2} \left(r_{o1} \| \frac{1}{g_{mb1}} \| \frac{1}{g_{m1}} \right) \right] + R_D} R_D \frac{r_{o1} \| \frac{1}{g_{mb1}}}{r_{o1} \| \frac{1}{g_{mb1}} + \frac{1}{g_{m2}}}$$

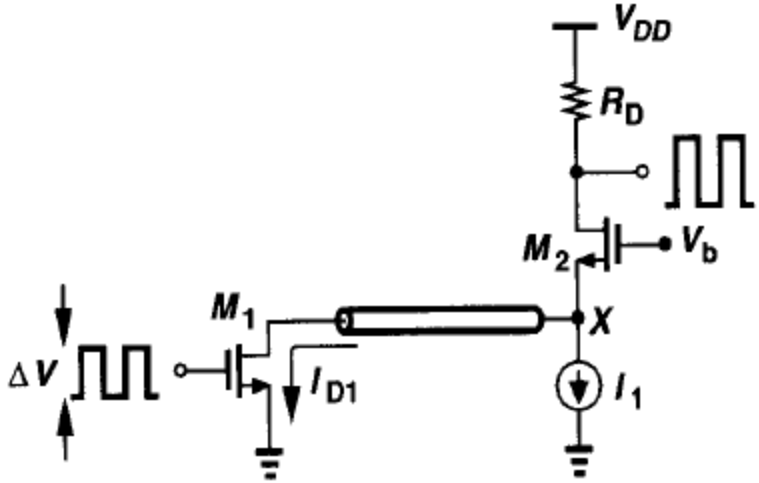
significantly larger gain when compared to CS stage

Example – 3

The CS-stage in both the following circuits senses ΔV at node X and delivers a proportional current to a 50Ω transmission line.

(a) Calculate small signal gain at low frequencies.
(b) What condition is necessary to minimize wave reflections at node X



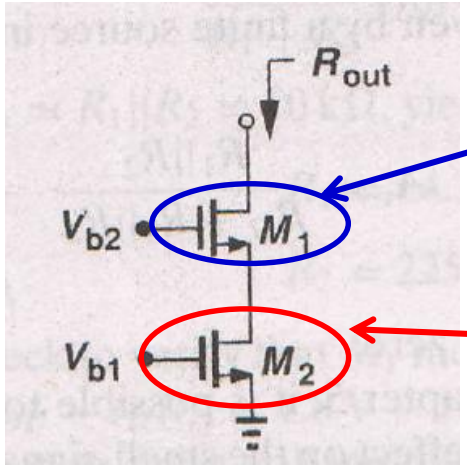


Cascode Stage

- **Terminology:** It stems from erstwhile vacuum tube in which cathodes were cascaded. In practice, the output of first tube (anode) feeds the input of second tube (cathode)
- **Configuration:** CG-stage in cascade with CS-stage → actually CS-stage is called the main device whereas CG is called the cascode device
- **Basic Idea:** combines high input impedance and large transconductance of CS with the current buffering property and the superior high frequency response of CG stage
- **Cascode Provides:** wider bandwidth, increased small-signal gain, high input impedance, customized output impedance
- **Applications:** Current Source, Small-Signal Amplifier

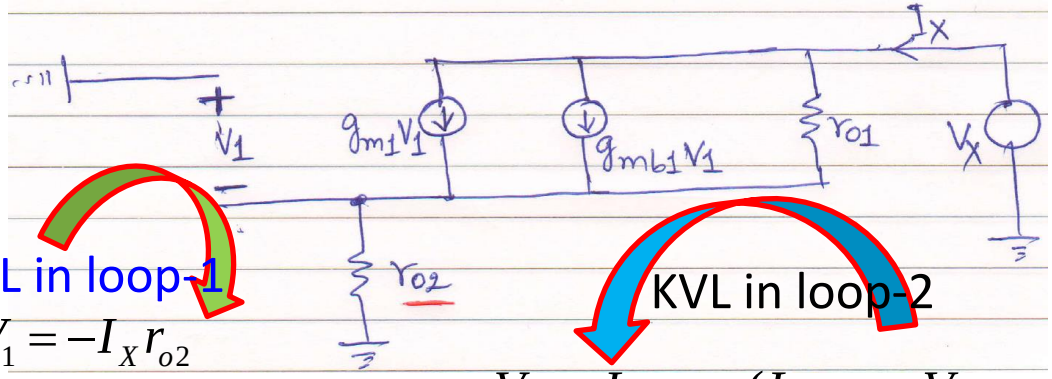
Cascode – as a current source

- Current Source: requires very high output impedance



Cascode Transistor (CG Stage): always in saturation and is the main device that provides a constant current source

Degeneration Transistor (CS Stage): in saturation and acts as a degeneration resistor for a fixed bias point → provides an impedance of r_{o2}



KVL in loop-1

$$V_1 = -I_X r_{o2}$$

KVL in loop-2

$$V_X = I_X r_{o2} + (I_X - g_{m1}V_1 - g_{mb1}V_1) r_{o1}$$

$$\Rightarrow \frac{V_X}{I_X}$$

$$= r_{o2} + r_{o1} + r_{o1}(g_{m1}r_{o2} + g_{mb1}r_{o2}) = R_{out}$$

Cascode – as a current source

$$\Rightarrow R_{out} = r_{o2} + r_{o1} + r_{o1}(g_{m1}r_{o2} + g_{mb1}r_{o2}) = r_{o2} + r_{o1}\left[1 + r_{o2}(g_{m1} + g_{mb1})\right]$$

$$R_{out} = r_{o1} + r_{o2}\left[1 + r_{o1}(g_{m1} + g_{mb1})\right]$$

However: $r_{o1}(g_{m1} + g_{mb1}) \gg 1$

$$r_{o1}(g_{m1}r_{o2} + g_{mb1}r_{o2}) \gg r_{o1}$$

$$\therefore R_{out} \approx (g_{m1} + g_{mb1})r_{o1}r_{o2}$$

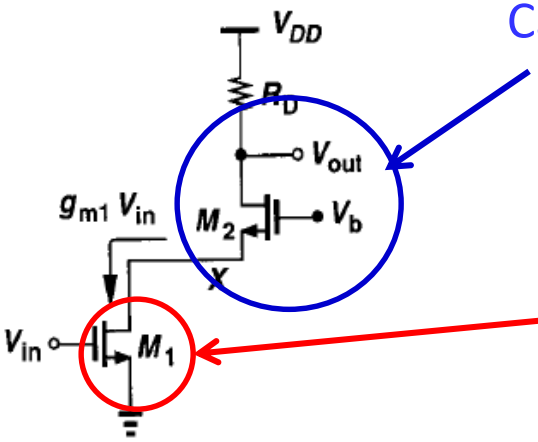
Very High Output Impedance

M_1 already in saturation

Appropriate candidate for constant current source

In this case, M_1 boosts the output resistance of M_2 by a factor of $(g_{m1}+g_{mb1})r_{o1}$

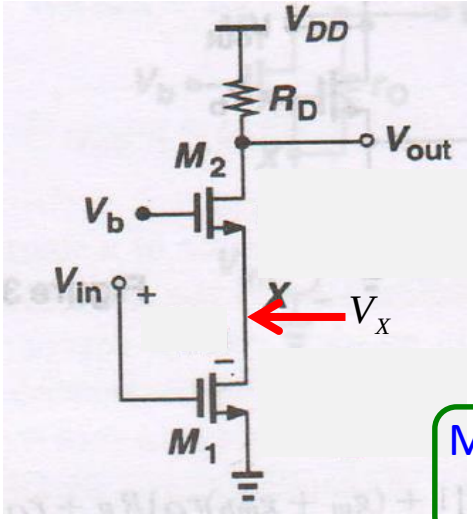
Cascode – Amplifier



Cascode device (in CG) → in saturation → routes the current generated by main device to R_D

main device (in CS) → in saturation → converts and amplifies an input voltage signal into output current

Bias Conditions of Cascode:



- For M_1 to be in saturation: $V_X > V_{in} - V_{T1}$

$$\Rightarrow V_b - V_{GS2} > V_{in} - V_{T1} \qquad \Rightarrow V_b > V_{in} + V_{GS2} - V_{T1}$$

- For M_2 to be in saturation: $V_{out} - V_X \geq V_{GS2} - V_{T2}$

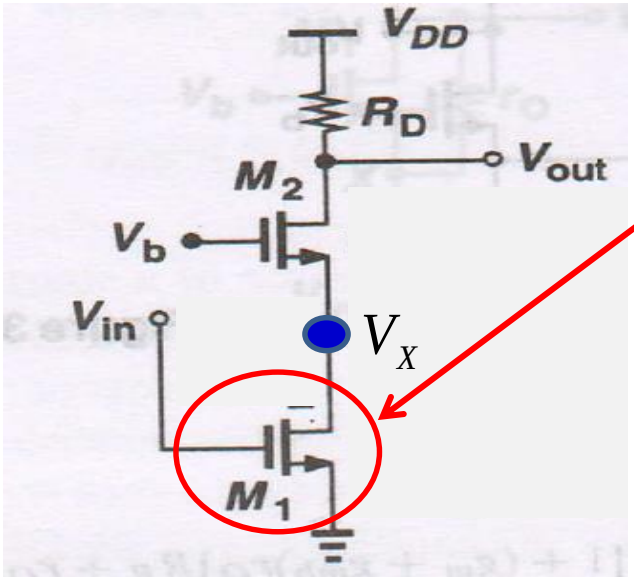
$$\Rightarrow V_{out} \geq \underbrace{V_{in} - V_{T1}}_{V_{OV1}} + \underbrace{V_{GS2} - V_{T2}}_{V_{OV2}}$$

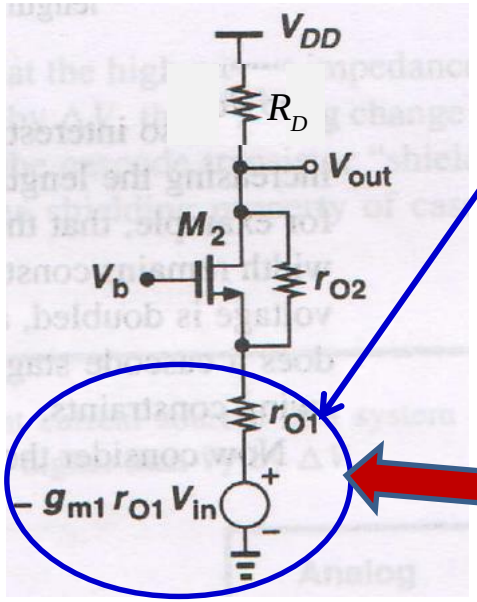
Minimum output voltage equals overdrive voltage of M_1 and M_2 → addition of M_2 reduces the output voltage swing by V_{GS2}-V_{T2}

Cascode – Amplifier (contd.)

It is a CS stage and therefore generates:

$$V_X = -g_{m1} r_{o1} V_{in}$$

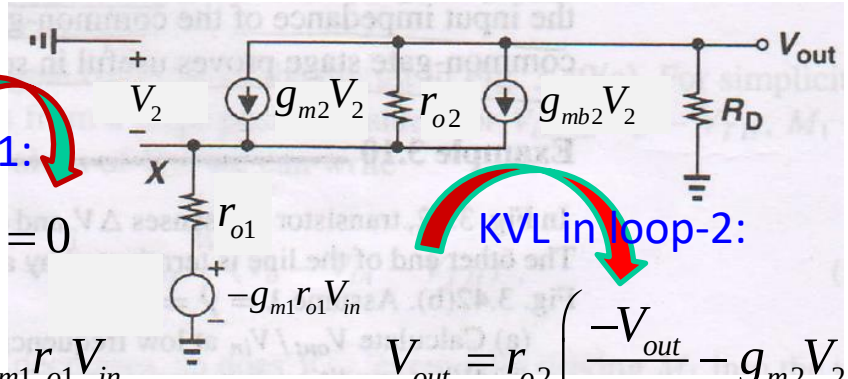




Contribution from M_1

Thevenin Equivalent

Small Signal Model of Cascode:



KVL in loop-1:

$$V_2 - \frac{V_{out}}{R_D} r_{o1} - g_{m1} r_{o1} V_{in} = 0$$

$$\Rightarrow V_2 = \frac{V_{out}}{R_D} r_{o1} + g_{m1} r_{o1} V_{in}$$

KVL in loop-2:

$$V_{out} = r_{o2}\left(\frac{-V_{out}}{R_D} - g_{m2} V_2 - g_{mb2} V_2 \right) - \frac{V_{out}}{R_D} r_{o1} - g_{m1} r_{o1} V_{in}$$

Cascode – Amplifier (contd.)

Simplification gives:

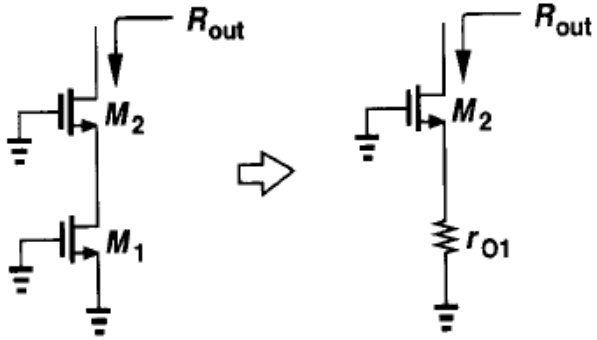
$$\frac{V_{out}}{R_D}\left[R_D + r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2}\right] = -\left[g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2} + g_{m1}r_{o1}\right]V_{in}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = A_v = -\frac{\left[g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2} + g_{m1}r_{o1}\right]}{\left[R_D + r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2}\right]}R_D$$

Now: $g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2} >> g_{m1}r_{o1}$

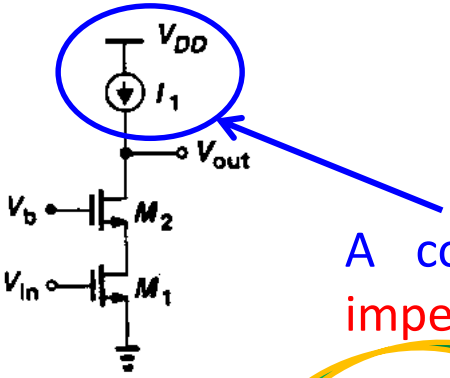
$$\therefore A_v \approx -\frac{g_{m1}(g_{m2} + g_{mb2})r_{o1}r_{o2}}{\left[R_D + r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o1}r_{o2}\right]}R_D$$

Output Impedance: ability to synthesize desired output impedance



$$R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$$

Cascode – Amplifier (contd.)



the gain of Cascode stage:

$$\Rightarrow A_v \approx -\frac{g_{m1}(g_{m2}+g_{mb2})r_{o1}r_{o2}}{\left[R_D + r_{o1} + r_{o2} + (g_{m2}+g_{mb2})r_{o1}r_{o2}\right]} R_D$$

A constant current source possesses very high output impedance ($R_D \rightarrow \infty$), therefore the gain equation changes to:

$$A_v \approx -g_{m1}(g_{m2}+g_{mb2})r_{o1}r_{o2} = -(g_{m1}r_{o1}).(g_{m2}+g_{mb2})r_{o2}$$

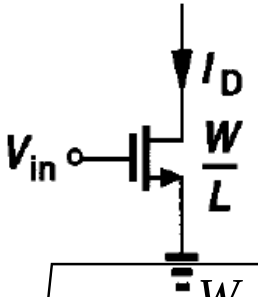
It is apparent that the maximum small-signal voltage gain is the multiplication of gains from CS and CG stages → definitely a big plus!

$$R_{out} \approx \left(g_{m2}+g_{mb2}\right)r_{o2}r_{o1}$$

Cascode – Amplifier (contd.)

Discussion with respect to alteration in dimension

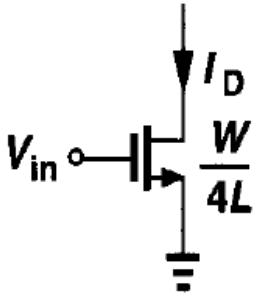
What happens if **Length (L)** of the main device is quadrupled while the **Width (W)** remains sa



$$A_v \approx -g_m r_o = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}\,\frac{1}{\lambda I_D}$$

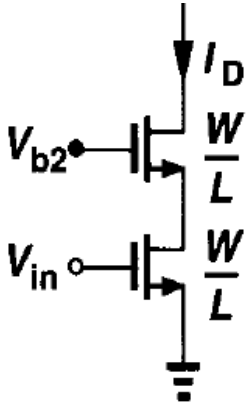
$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$

$$\left(V_{GS} - V_{TH}\right)^2 = \frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}$$



$$A_{v1} = 2A_v$$

$$g_{m1} = \frac{g_m}{2}$$



$$A_{v2} = \left(A_v\right)^2$$

$$g_{m2} = g_m$$

Cascode more suited for noise applications

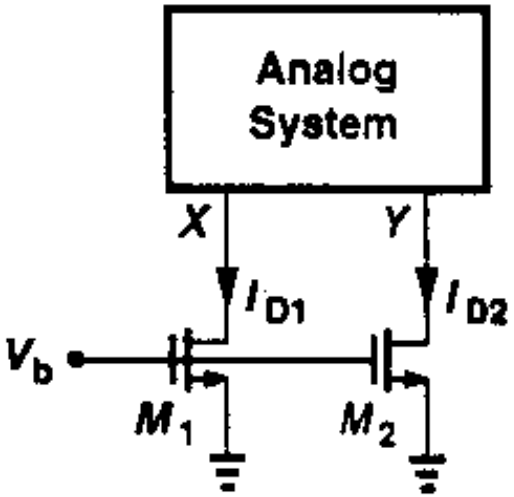
Quadruppling of **Length (L)** while keeping the **Width (W)** results in doubling of overdrive voltage

For **identical devices**, cascode also exhibits doubling of overdrive voltage

Shielding Property of Cascode

Cascode amplifier and Cascode current source → could be used in applications where the output varies drastically due to any reason! → This variation doesn't affect the subsequent sections greatly → shielding property of Cascode

Example: Two identical NFETs are used to generate constant current sources. However, due to internal circuitry of the system, V_X is higher than V_Y by ΔV.



Q: determine the resulting difference between I_{D1} and I_{D2} if $\lambda \neq 0$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(1+\lambda V_X\right)$$

(V_{DS1})

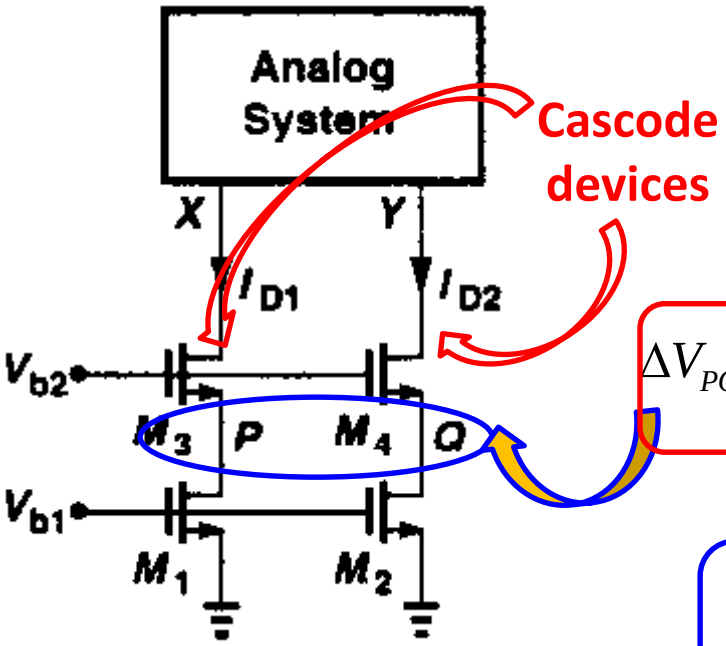
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(1+\lambda V_Y\right)$$

(V_{DS2})

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\lambda \Delta V\right)$$

Shielding Property of Cascode (contd.)

Q: Add Cascode devices to M1 and M2 and then check the difference between I_{D1} and I_{D2} if $\lambda \neq 0$



Cascode devices

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\lambda \Delta V_{PQ}\right)$$

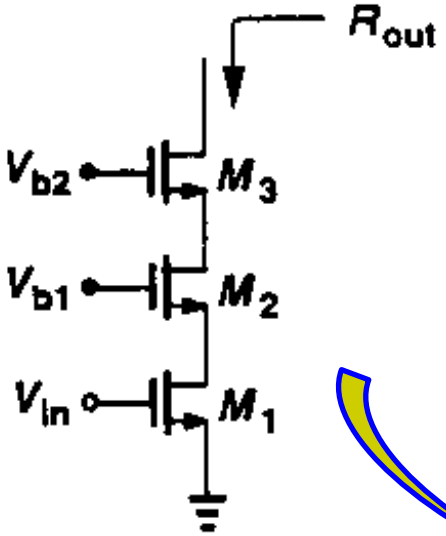
$$\Delta V_{PQ} = \Delta V \frac{r_{o1}}{\left[1+\left(g_{m3}+g_{mb3}\right)r_{o3}\right]r_{o1}+r_{o3}} \approx \frac{\Delta V}{\left(g_{m3}+g_{mb3}\right)r_{o3}}$$

$$\therefore I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\frac{\lambda \Delta V}{\left(g_{m3}+g_{mb3}\right)r_{o3}}\right)$$

This is a large value and thus the Cascode structure gives smaller variation → perfect example of Shielding property!!!

Triple Cascode

- Cascoding can be extended to three or more devices to achieve higher output impedance



It limits the voltage swing

Here the minimum output voltage equals the sum of three overdrive voltages

Folded Cascode **Self Study**