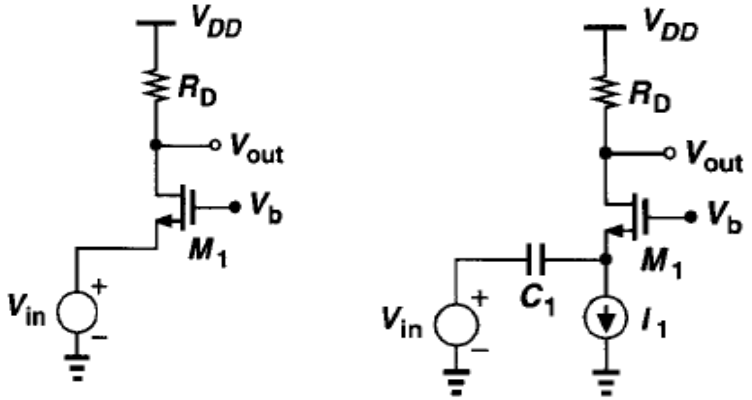
Lecture – 7

Date: 01.09.2016

- CG Amplifier
- Examples
- Biasing in MOS Amplifier Circuits

Common Gate (CG) Amplifier



- CG Amplifier- Input is applied at the Source and the output is sensed at the Drain.
- The Gate terminal is used for establishing appropriate bias conditions for the transistor.

- Its characteristic can be studied through large-signal behavior as well.
- For large V_{in} i.e. for $V_{in} > V_b - V_T$: M_1 is off and therefore: $V_{out} = V_{DD}$
- For lower V_{in}: $$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_b - V_{in} - V_T\right)^2$$

$$V_{out} = V_{DD} - I_D R_D = V_{DD} - \left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_b - V_{in} - V_T\right)^2\right)R_D$$

- Then small signal gain is: $$\frac{\partial V_{out}}{\partial V_{in}} = -\left(\mu_n C_{ox}\frac{W}{L}\left(V_b - V_{in} - V_T\right)\left(-1 - \frac{\partial V_T}{\partial V_{in}}\right)\right)R_D$$

Common Gate (CG) Amplifier (contd.)

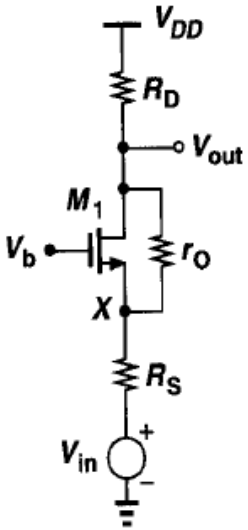
- Since, $\partial V_T/\partial V_{in} = \partial V_T/\partial V_{SB} = \eta$:

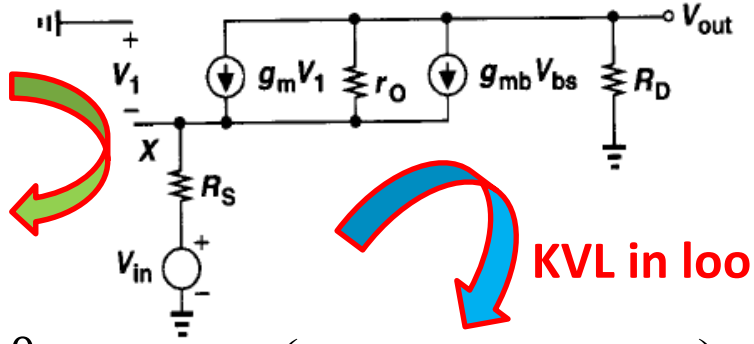
$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}\left(V_b - V_{in} - V_T\right)\left(1+\eta\right)R_D$$

$$A_v = g_m\left(1+\eta\right)R_D$$

Non-inverting Amplifier

Higher as compared to CS stage





KVL in loop-1:

$$V_1 - \frac{V_{out}}{R_D}R_S + V_{in} = 0$$

KVL in loop-2:

$$V_{out} = r_o\left(\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb}V_1\right) - \frac{V_{out}}{R_D}R_S + V_{in}$$

$$\frac{V_{out}}{V_{in}} = A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D}R_D$$

CG Amplifier (contd.)

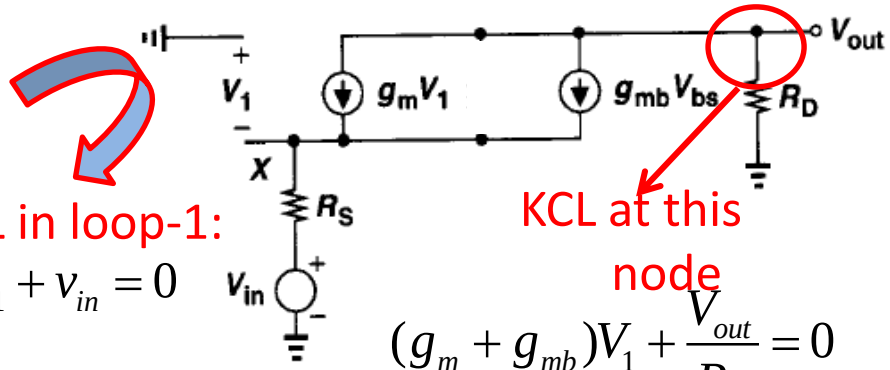
$$\frac{V_{out}}{V_{in}} = A_v = \frac{(g_m + g_{mb})r_o + 1}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D} R_D$$

Non-inverting with slightly higher value as compared to the CS stage → body effect is useful in this scenario

- If the resistor R_D is replaced by a current source then: $\frac{V_{out}}{V_{in}} = A_v = (g_m + g_{mb})r_o + 1$

$R_D \rightarrow \infty$ for an ideal current source

- Let us look at small-signal model – without channel length modulation and biased with a constant current source



KVL in loop-1:

$$v_1 + v_{in} = 0$$

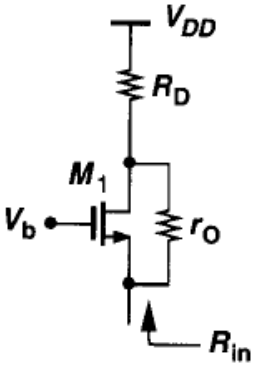
KCL at this node

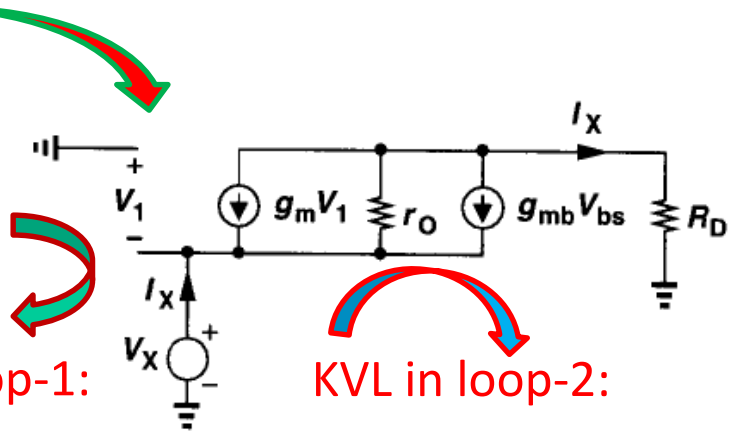
$$(g_m + g_{mb})V_1 + \frac{V_{out}}{R_D} = 0$$

$$\Rightarrow A_v = \frac{V_{out}}{V_{in}} = (g_m + g_{mb})R_D = g_m(1+\eta)R_D$$

CG Amplifier (contd.)

- Input Impedance:





KVL in loop-1:

$$V_1 = -V_X$$

KVL in loop-2:

$$R_D I_X + r_o\left[I_X - (g_m + g_{mb})V_X\right] = V_X$$

$$R_{in} = \frac{V_X}{I_X} = \frac{R_D + r_o}{1 + (g_m + g_{mb})r_o} \approx \frac{R_D}{(g_m + g_{mb})r_o} + \frac{1}{(g_m + g_{mb})}$$

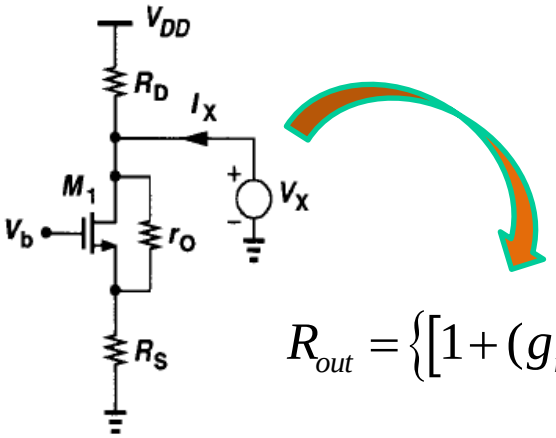
- **Case-I:** $R_D = 0$ ⇒ $R_{in} = \dfrac{V_X}{I_X} = \dfrac{r_o}{1 + (g_m + g_{mb})r_o}$

- **Case-II**: R_D is an ideal current source ie, $R_D \to \infty$ ⇒ $R_{in} \to \infty$

It is apparent that the input impedance of common-gate stage is low only if the load impedance connected to the drain is low

CG Amplifier (contd.)

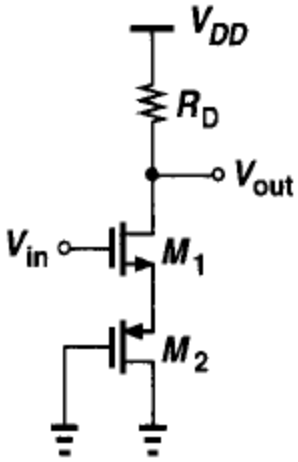
- Output Impedance:



$$R_{out} = \{[1+(g_m + g_{mb})r_o]R_S + r_o\} \| R_D$$

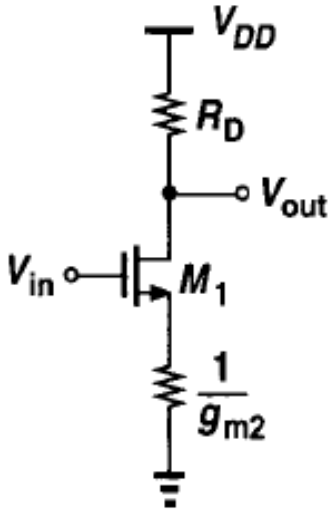
Example – 1

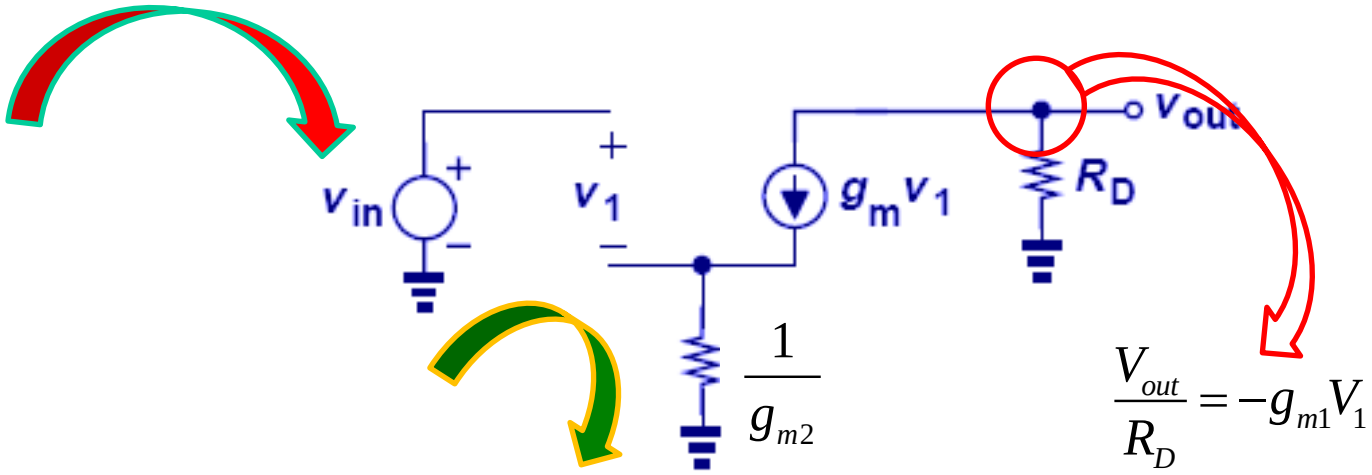
- Derive the small-signal voltage gain expression for this amplifier. Consider the cases when channel length modulation are absent and present.



Example – 1 (contd.)

- **Case-I:** λ = 0 both for M_1 and M_2 → In such a case M_2 presents a degenerating impedance of $1/g_{m2}$ to a single stage CS amplifier as shown below.





$$V_{in} = V_1 + g_{m1}V_1.\frac{1}{g_{m2}} = V_1\left(1+\frac{g_{m1}}{g_{m2}}\right)$$

$$\frac{V_{out}}{R_D} = -g_{m1}V_1$$

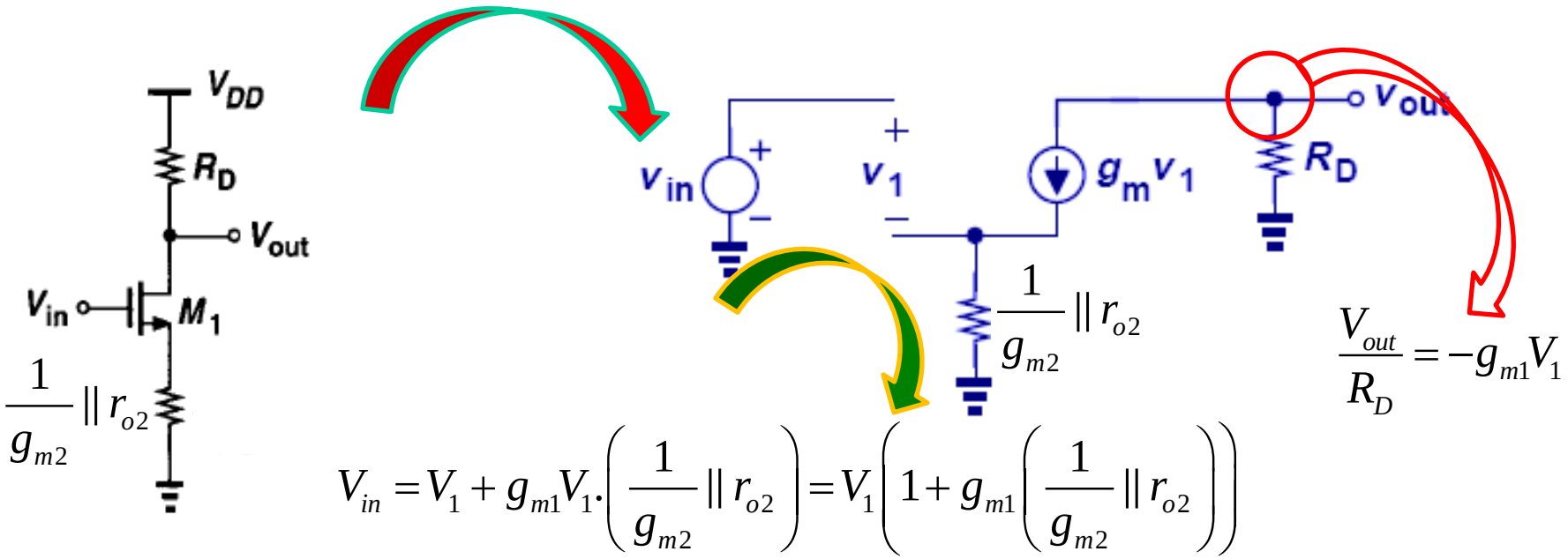
Simplification gives: $V_{out} = -g_{m1}V_1R_D$

$$\Rightarrow V_{out} = -g_{m1}R_D.\frac{g_{m2}.V_{in}}{g_{m2}+g_{m1}}$$

$$\therefore A_v = -\frac{R_D}{\frac{1}{g_{m1}}+\frac{1}{g_{m2}}}$$

Example – 1 (contd.)

- **Case-II:** λ = 0 for M_1 and λ ≠ 0 for M_2 → In such a case M_2 presents a degenerating impedance of $(1/g_{m2} \| r_{o2})$ as shown below.



$$V_{out} = -g_{m1} V_1 R_D$$

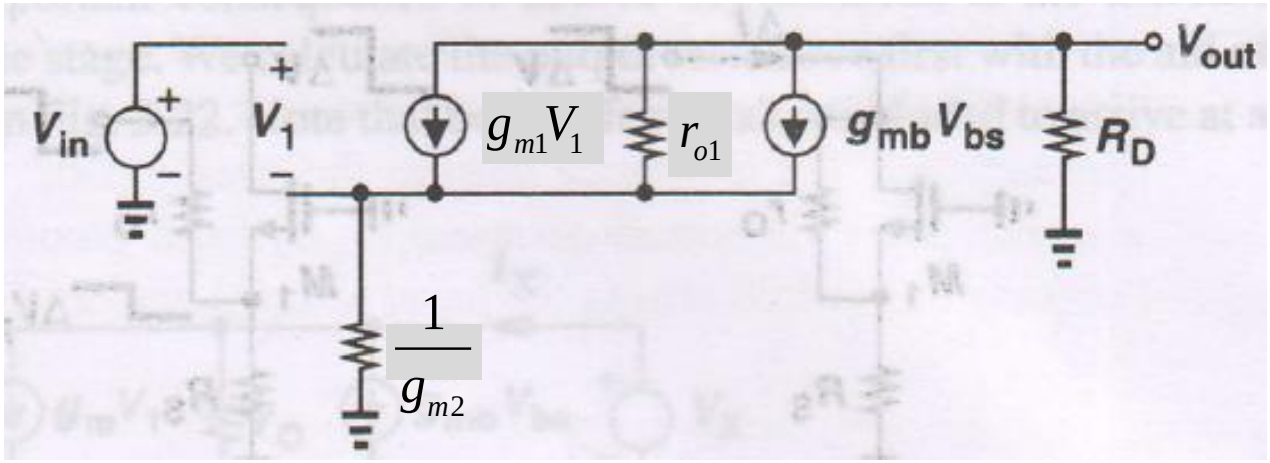
$$V_{in} = V_1 + g_{m1} V_1 \cdot \left(\frac{1}{g_{m2}} \| r_{o2} \right) = V_1 \left(1 + g_{m1} \left(\frac{1}{g_{m2}} \| r_{o2} \right) \right)$$

Simplification gives:

$$\therefore A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \left(\frac{1}{g_{m2}} \| r_{o2} \right)}$$

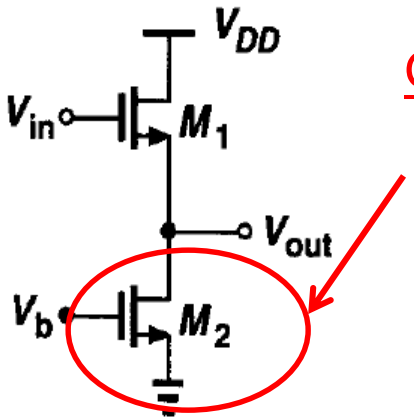
Example – 1 (contd.)

- **Case-III:** $\lambda = 0$ for M_2 and $\lambda \neq 0$ for M_1 → In such a case the small signal model looks like:

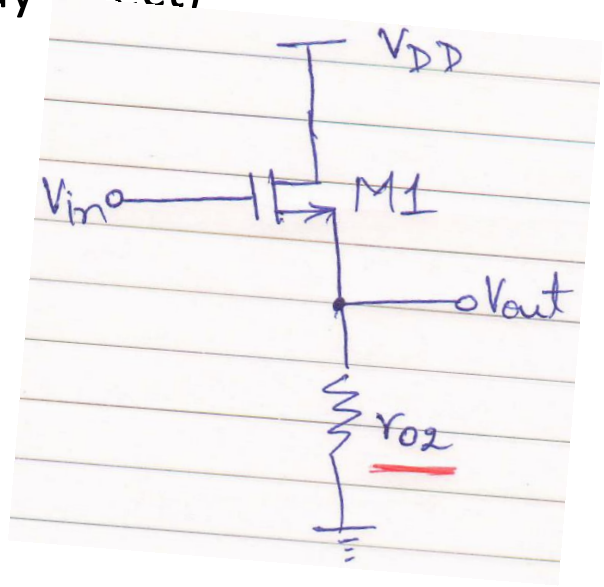


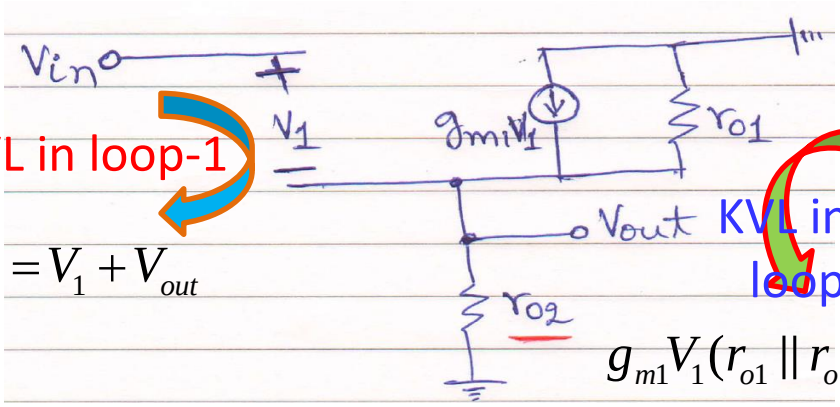
Example – 2

- Derive expression for the small-signal voltage gain of the following circuit. (Assume: λ ≠ 0 for both M_1 and M_2. Neglect body effect)



Gate and Source are fixed. Therefore this NMOS works as a constant current source with an impedance r_{o2} across its drain and source





KVL in loop-1

$$V_{in} = V_1 + V_{out}$$

KVL in loop-2

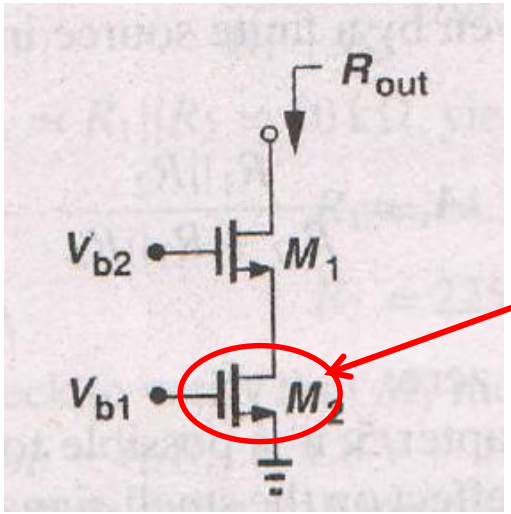
$$g_{m1}V_1(r_{o1} \| r_{o2}) = V_{out}$$

$$g_{m1}(V_{in} - V_{out})(r_{o1} \| r_{o2}) = V_{out}$$

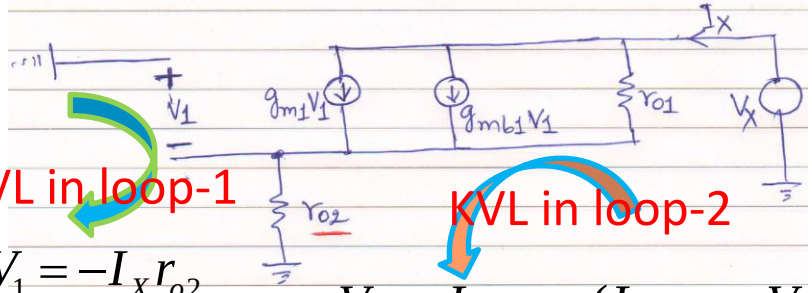
$$\therefore A_v = \frac{V_{out}}{V_{in}} = \frac{(r_{o1} \| r_{o2})}{\left[\frac{1}{g_{m1}} + (r_{o1} \| r_{o2})\right]}$$

Example – 3

- What is R_{out} in the following circuit. (Assume: $\lambda \neq 0$ for both M_1 and M_2 and both are in saturation.)



Gate and Source are fixed. Therefore this NFET works as a constant current source with an impedance r_{o2} across its drain and source



KVL in loop-1

$$V_1 = -I_X r_{o2}$$

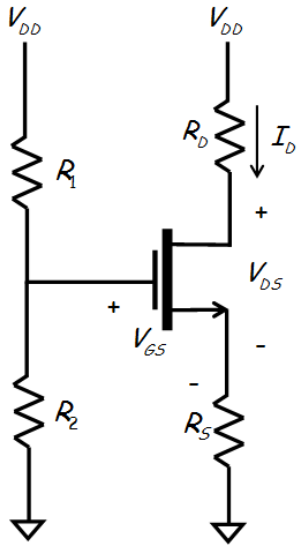
KVL in loop-2

$$V_X = I_X r_{o2} + (I_X - g_{m1}V_1 - g_{mb1}V_1)r_{o1}$$

$$\Rightarrow \frac{V_X}{I_X} = r_{o2} + r_{o1} + r_{o1}(g_{m1}r_{o2} + g_{mb1}r_{o2}) = R_{out}$$

Biasing using Single Power Supply

- The general form of a **single**-supply MOSFET amplifier biasing circuit is:



- We typically attempt to satisfy three main bias design goals:

1) Maximize Gain

Typically, the small-signal **voltage gain** of a MOSFET amplifier will be proportional to transconductance g_m.

$$A_v \propto g_m$$

Thus, to maximize the amplifier voltage gain, we must **maximize** the MOSFET transconductance.

Q: What does this have to do with **D.C. biasing?**

A: Recall that the transconductance depends on the **DC excess gate voltage**:

$$g_m = 2K(V_{GS} - V_T)$$

- Another way to consider transconductance is to express it in terms of DC drain current I_D.

Biasing using Single Power Supply (contd.)

- Recall this DC current is related to the DC excess gate voltage (in saturation!) as:

$$I_D = K(V_{GS} - V_T)^2 \quad \Rightarrow \quad (V_{GS} - V_T) = \sqrt{\frac{I_D}{K}}$$

- And so transconductance can be alternatively expressed as:

$$g_m = 2K(V_{GS} - V_T) = 2K\sqrt{\frac{I_D}{K}} = 2\sqrt{KI_D}$$

- Therefore, the amplifier voltage gain is typically **proportional** to the square-root of the DC drain current:

$$A_v \propto \sqrt{I_D}$$

To maximize A_v, maximize I_D

2) Maximize Voltage Swing

Recall that if the DC drain voltage V_D is biased too close to V_{DD}, then even a small **small-signal** drain voltage $v_d(t)$ can result in a **total** drain voltage that is too **large**, i.e.:

$$v_D(t) = V_D + v_d(t) \geq V_{DD}$$

In other words, the MOSFET enters **cutoff**, and the result is a **distorted** signal!

Biasing using Single Power Supply (contd.)

- To avoid this (to allow $v_d(t)$ to be as large as possible without MOSFET entering cutoff), we need to bias our MOSFET such that the DC drain voltage V_D is as **small** as possible.
- Note that the drain voltage is: $V_D = V_{DD} - R_D I_D$
- Therefore V_D is minimized by designing the bias circuit such that the DC drain current I_D is as **large** as possible.
- However, we must **also** consider the signal distortion that occurs when the MOSFET enters **triode**. This of course is avoided if the total drain-to-source voltage remains greater than the excess gate voltage, i.e.:

$$v_{DS}(t) = V_{DS} + v_{ds}(t) > (V_{GS} - V_T)$$

- Thus, to avoid the MOSFET triode mode—and the resulting signal distortion—we need to bias our MOSFET such that the DC voltage is as **large** as possible.

To minimize signal distortion, maximize V_{DS}

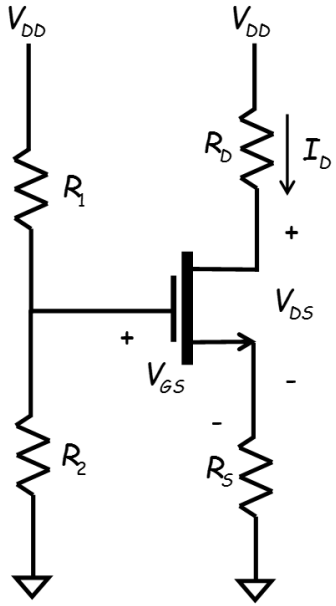
Biasing using Single Power Supply (contd.)

3) Minimize Sensitivity to changes in K, V_T

- We find that MOSFETs are **sensitive** to temperature—specifically, the value of K is a function of temperature.
- Likewise, the values of K and V_T are not particularly constant with regard to the manufacturing process.
- Both of these facts lead to the requirement that our bias design be **insensitive** to the values of K and V_T. Specifically, we want to design the bias network such that the DC bias current does **not** change values when K and/or V_T does.
- **Mathematically,** we can express this requirement as minimizing the value: $\frac{dI_D}{dK}$ **and** $\frac{dI_D}{dV_T}$
- These derivatives can be minimized by maximizing the value of **source resistor R_S.**
- So, let's **recap** what we have learned about designing our bias network:

1. Make I_D as large as possible.
2. Make V_{DS} as large as possible.
3. Make R_S as large as possible.

Biasing using Single Power Supply (contd.)



$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

or

$$I_D R_D + V_{DS} + I_D R_S = V_{DD}$$

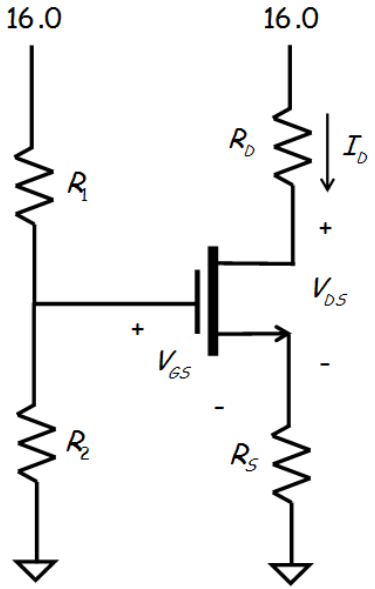
Maximize A_v by **maximizing** this term.

Minimize distortion by **maximizing** this term.

Minimize sensitivity by **maximizing** this term.

But the **total** of the three terms must equal this!

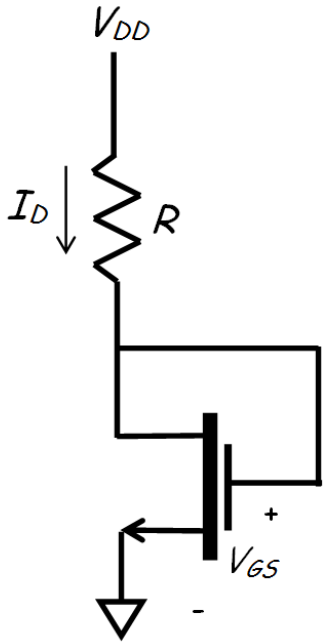
Example – 1



- If the MOSFET has device values $K = 1.0\ {}^{mA}/_{V^2}$ and $V_T = 1.0V$, determine the resistor values to bias this MOSFET with a DC drain current of $I_D = 4.0mA$.

The MOSFET Current Mirror

- Consider the following MOSFET circuit:



- Note $V_D = V_G$, therefore: $V_{DS} = V_{GS}$
- and thus: $V_{DS} > V_{GS} - V_T$
- **The MOSFET is in saturation if $V_G > V_T$.**
- We know that for a MOSFET in saturation, the drain current is: $V_{DS} = V_{GS}$

Say we want this current I_D to be a **specific** value—call it I_{ref}.

- Since $V_S = 0$, we find that from the above equation, the drain voltage must be: $V_D = \sqrt{\frac{I_{ref}}{K}} + V_T$

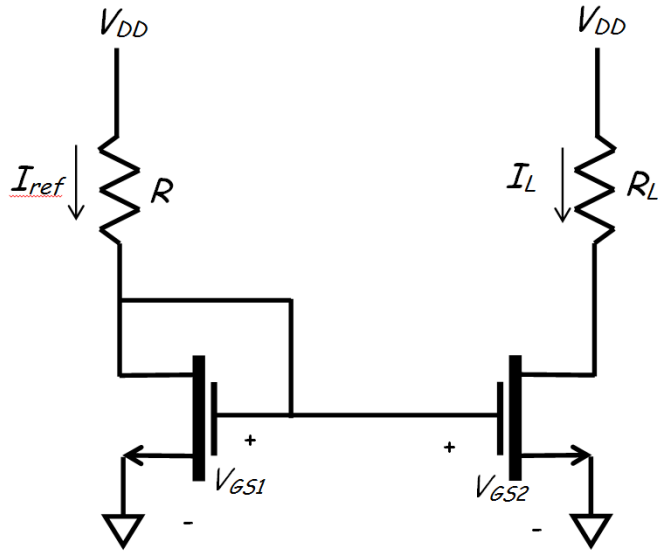
- Likewise, from KVL we find that: $I_{ref} = \frac{V_{DD} - V_D}{R}$

- And thus the **resistor** value to achieve the desired drain current I_{ref} is: $R = \frac{V_{DD} - V_D}{I_{ref}}$

The MOSFET Current Mirror (contd.)

Q: Why are we doing this?

A: Say we now add another component to the circuit, with a second MOSFET that is **identical** to the first :



Q: So what is current I_L?

A: Note that the gate voltage of each MOSFET is the **same** (i.e., $V_{GS1} = V_{GS2}$), and if the MOSFETS are the **same** (i.e., $K_1 = K_2, V_{T1} = V_{T2}$), and if the second MOSFET is likewise in **saturation.**

- The drain current I_L is:

$$I_L = K_2 (V_{GS2} - V_{T2})^2$$
$$= K_1 (V_{GS1} - V_{T1})^2 = I_{ref}$$

Therefore, the drain current of the **second** MOSFET is **equal** to the current of the **first**!

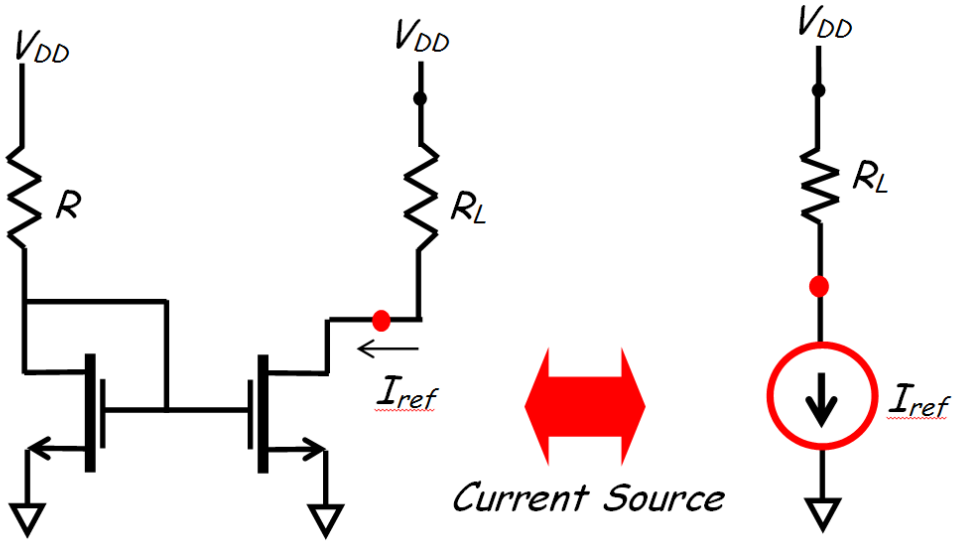
$$I_{ref} = I_L$$

The MOSFET Current Mirror (contd.)

Q: Wait a minute! You mean to say that the current through the resistor R_L is **independent** of the value of resistor R_L?

A: Absolutely! As long as the second MOSFET is in **saturation**, the current through R_L is equal to I_{ref}—**period**.

- The current through R_L is independent of the value of R_L (provided that the MOSFET remains in saturation). Think about what this means—this device is a **current source** !



- Remember, the second MOSFET **must** be in saturation for the current through R_L to be a constant value I_{ref}. As a result, we find that:

$$V_{DS2} > V_{GS2} - V_{T2}$$

- For this example: $V_{D2} > V_{G2} - V_{T2}$

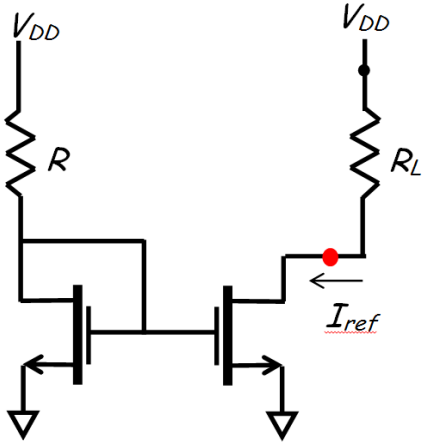
The MOSFET Current Mirror (contd.)

- Since $V_{D2} = V_{DD} - R_L I_{ref}$, we find that the MOSFET will be in saturation if:

$$V_{DD} - R_L I_{ref} > V_{G2} - V_{T2} = V_{G1} - V_{T1}$$

- Alternatively, we find the limitation on the load resistor R_L:

$$R_L < \frac{V_{DD} - V_{G1} + V_{T1}}{I_{ref}}$$



- We know that: $V_{G1} = V_{DD} - R\, I_{ref}$
- Thus we can alternatively write the above equation as:

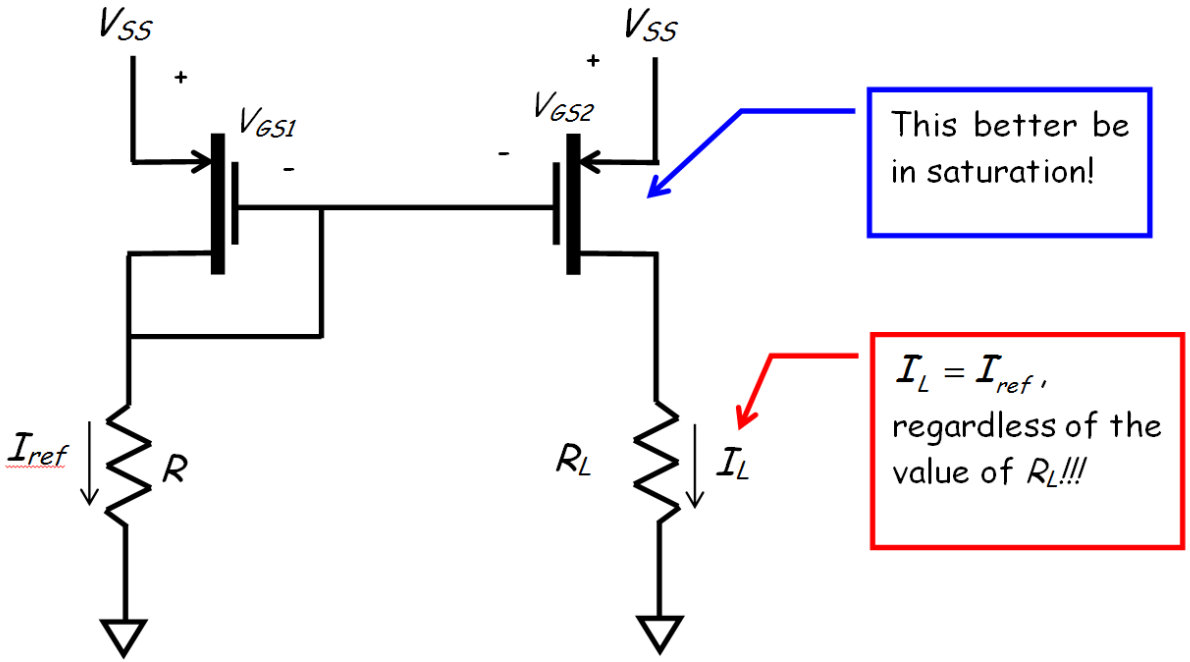
$$R_L < R + \frac{V_{T1}}{I_{ref}}$$

- If the **load** resistor becomes **larger** than $R + {}^{V_{T1}}/_{I_{ref}}$, the voltage V_{DS2} will drop **below** the excess gate voltage $V_{GS2} - V_{T2}$, and thus the second MOSFET will enter the **triode** region. As a result, the drain current will **not** equal I_{ref}—the current source will **stop working**!

The MOSFET Current Mirror (contd.)

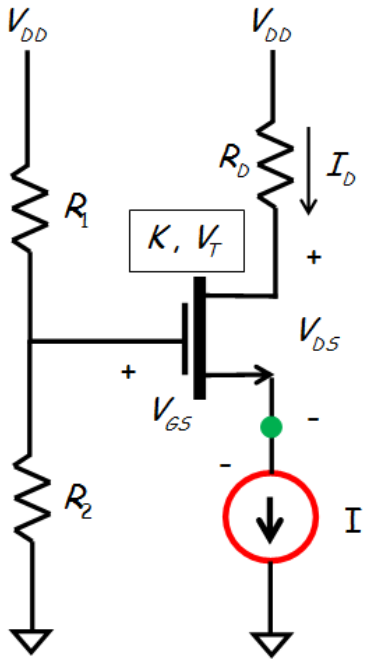
Although the circuit is sometimes referred to as a current sink, understand that the circuit is clearly a way of designing a current source.

- We can also use **PMOS** devices to construct a current mirror!



MOSFET Biasing using Current Mirror

- We can bias a MOSFET amplifier using a **current source** as:

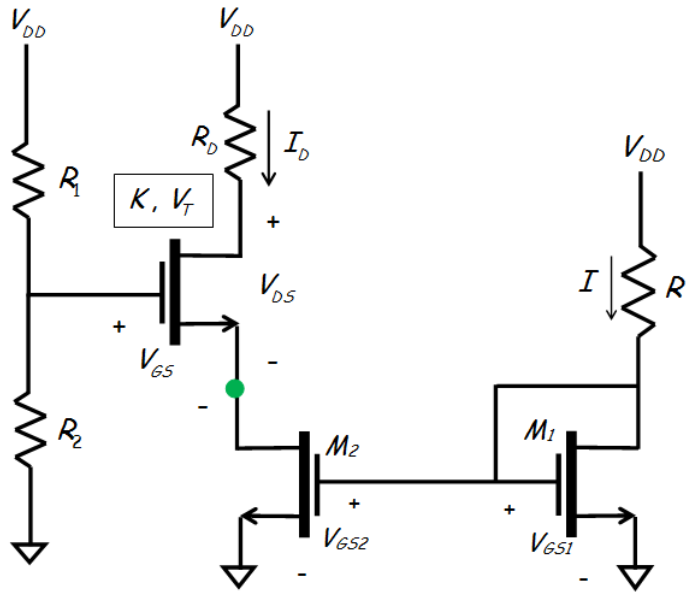


It is evident that the DC drain current I_D, is equal to the current source I, **regardless** of the MOSFET values K or V_T!

Thus, this bias design maximizes drain current **stability**!

MOSFET Biasing using Current Mirror (contd.)

- We now know how to implement this bias design with MOSFETs—we use the **current mirror** to construct the current source!



- Since $I_D = I$, it is evident that V_{GS} **must** be equal to:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_T$$

- Since the DC **gate** voltage is:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

- Therefore:

$$V_S = V_G - V_{GS}$$
$$= V_{DD}\left(\frac{R_2}{R_1 + R_2}\right) - \left(\sqrt{\frac{I}{K}} + V_T\right)$$

MOSFET Biasing using Current Mirror (contd.)

- Since we are biasing with a current source, we do **not** need to worry about drain current **stability**—the current source will determine the DC drain current for **all** conditions (i.e., $I_D = I$).
- We might conclude, therefore, that we should make DC source voltage V_S as **small** as possible. After all, this would allow us to **maximize** the output voltage swing (i.e., maximize $I_D R_D$ and V_{DS}).
- Note however, that the **source** voltage V_S of the MOSFET is numerically equal to the **drain** voltage V_{D2} (and thus V_{DS2}) of the second MOSFET of the **current mirror**.

Q: So what?!

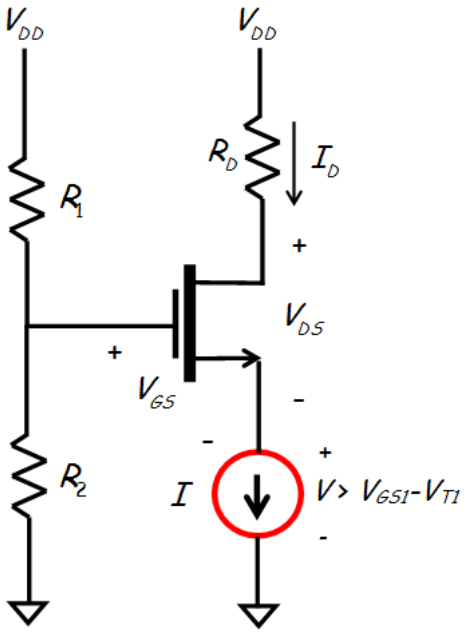
A: The voltage must be **greater** than:

$$V_{GS2} - V_{T2} = V_{GS1} - V_{T1} = \left(V_{DD} - I_{ref} R\right) - V_{T1}$$

in order for the **second** MOSFET to remain in **saturation**.

There is a **minimum voltage** across the current source in order for the current source to properly operate!

MOSFET Biasing using Current Mirror (contd.)



- Thus, to maximize output swing, we **might** wish to set:

$$V_S = V_{GS1} - V_{T1}$$

(although to be practical, we should make V_S **slightly greater** than this to allow for some design **margin**).

Q: How do we "set" the DC **source** voltage V_S??

A: By setting the DC **gate** voltage V_G!!

- Recall that the DC voltage V_{GS} is determined by the DC current source value **I**:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_T$$

- and the DC gate voltage is determined by the **two** resistors R_1 and R_2:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

- Thus, we should **select** these resistors such that:

$$V_G = V_{GS} + V_S$$
$$= \left(\sqrt{\frac{I}{K}} + V_T\right) + \left(V_{GS1} - V_{T1}\right)$$

MOSFET Biasing using Current Mirror (contd.)

Q: So what should the value of resistor $\mathrm{R_D}$ be?

A: Recall that we should set the DC **drain** voltage $\mathrm{V_D}$:

a) much **less** than V_{DD} to avoid **cutoff**.
b) much **greater** than $V_G - V_T$ to avoid **triode**.

- Thus, we **compromise** by setting the DC drain voltage to a point **halfway** in between!

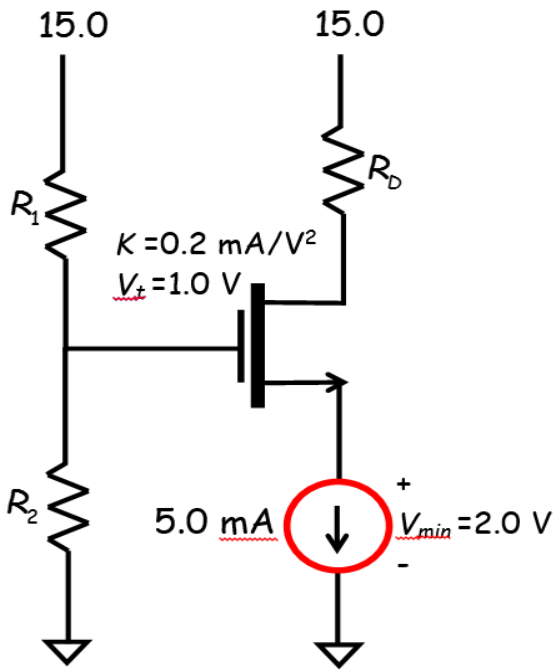
$$V_D = \frac{V_{DD} + (V_G - V_T)}{2}$$

- To achieve this, we must select the drain **resistor** R_D so that:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{V_{DD} - (V_G - V_T)}{I_D}$$

Example – 2

Let's determine the proper resistor values to DC bias this MOSFET. The current source is 5.0 mA and has a minimum voltage of 2.0 Volts in order to operate properly



- Since $I = I_D = 5\,mA$, we know that the value of V_{GS} should be:

$$V_{GS} = \sqrt{\frac{I}{K}} + V_T$$
$$= \sqrt{\frac{5.0}{0.2}} + 1.0$$
$$= 6.0\,V$$

- Assuming that we want the DC source voltage to be the minimum value of $V_S = 2.0V$, we need for the DC gate voltage to be:

$$V_G = V_{GS} + V_S$$
$$= 6.0 + 2.0$$
$$= 8.0\,V$$

Example – 2 (contd.)

- Thus, we need to select resistors R_1 and R_2 so that: $V_G = 8.0 = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$
- or in other words, we want: $\left(\frac{R_2}{R_1 + R_2}\right) = \frac{8.0}{15.0}$
- Since we can make R_1 and R_2 large, let's assume that we want: $R_1 + R_2 = 300\,\text{K}$

So that $R_1 = 140\ k\Omega$ and $R_2 = 160\ k\Omega$.

- Finally, we want the DC drain voltage to be:

$$V_D = \frac{V_{DD} + (V_G - V_T)}{2} = \frac{15.0 + (8.0 - 1.0)}{2} = 11.0\,\text{V}$$

- So that the resistor is:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15.0 - 11.0}{5.0} = 0.8\,\text{K}\Omega$$

Example – 2 (contd.)