Lecture-1

Date: 01.08.2016

- Introduction
- MOSFET
- NMOSFET Qualitative Analysis
- PMOSFET
- MOSFET – Region of Operation

Analog CMOS Circuit Design (ECE315 / ECE515)

Instructor: Dr. Mohammad S. Hashmi

TAs: Anuradha Ahlawat, Deepayan Banerjee, Dinesh Rano

Class Timings: Monday (14:30 – 16:00) & Thursday (14:30 – 16:00)

Office Hours: Tuesday (14:00 – 16:00)

TA Hours: TBA

ECE315 / ECE515

Pre-requisites: Circuit or Network Analysis, Electronics Devices

Course URL:
Available at: http://www.iiitd.edu.in/~mshashmi/Teaching.html

Course Focus:
MOSFET based analog circuit blocks and associated advanced circuits

Course Objectives:
On the completion of this course students should

- Have a basic knowledge of the fundamental concepts of active circuits and their analysis techniques.
- Particularly understand the theory and operation of circuit & components such as Current Mirror, Linear Amplifier, Differential Amplifier, Power Amplifier etc.
- Acquire the ability to solve, analyze, design, and simulate moderately complex MOS based circuits.

ECE315 / ECE515

Lab Component:

- Introduction to SPICE and Cadence Tools – by TAs
- Advanced Topics is mostly self learning – may be assisted by the TAs

Evaluation:

- Assignments (SPICE and Cadence Based)– 15% (6 assignments)
- Surprise Quizzes – 15% (5 quizzes)
- Exams – mid-sem (20%) & end-sem (20%)
- Project – 30%

Attendance and Classroom Behavior:

- Attendance not mandatory
- Students will be responsible for any notes, announcements etc. made during the class
- Prompt arrival to the class is requested
- No eating, drinking, smoking allowed in the class

ECE315 / ECE515

Text Books:

- Design of Analog CMOS Circuits *by* Behzad Razavi
- CMOS Analog Circuit Design *by* Allen & Holberg

Other Recommended Books:

- Microelectronic Circuit Design ***by*** Jaeger & Blalock
- Analog Integrated Circuit Design ***by*** Johns & Martin

Course Website:

http://www.iiitd.edu.in/~mshashmi/Teaching.html

Info related to ECE315 / ECE515 can be found here

Why Analog?

- All the world is an analog stage and digital circuits play only bit parts.

- Anonymous

- It's bad enough that hundreds of people are already "designing" CMOS VLSI without any significant knowledge of silicon devices and circuits and sometimes without much idea of the physics of hardware in the broader sense. As electronic systems become increasingly complex, this type of design will inevitably dominate, certainly for large-scale digital systems. But I wonder how many potentially useful ideas in the meadowlands of analog circuits will never be discovered because the world of the twenty-first century was taught that analog is dead?

Barrie Gilbert, "Where do little circuits come from?"

- As an old analog guru once said when comparing the analog and digital disciplines, "Any idiot can count to one, but analog design requires the engineer to make intelligent trade-offs to optimize a circuit." Analog design is not black or white as in "ones" and "zeros;" analog design is shades of gray.

- Samual Wilensky, "Reflections of a dinosaur"

Some Thoughts!!!

- Analog circuit design is like chess -just because you know how the pieces move doesn't mean you know how to play the game.

- Patrick M. Lahey

- Since this course deals in analog design, we take to heart a quote from **Chris Manglesdorf (Analog Devices)** at ISSCC '96, where he said that *"Analog circuit designers tend to think of themselves as lone cowboys, brave pioneers, creative and independent types, in contrast to the herd animals of the digital IC world"*

- Some thirty years ago, I asserted at a seminar presented at UC Berkeley that the art of analog design demanded 30% attention to the signal path and 70% to biasing. The comment was met with tolerant disbelief. However, after having taught this maxim widely and persistently during the intervening decades, I find no reason to change my mind.

-BARRIE GILBERT, "Biasing Techniques for RF/IF Signal Processing"

Has the analog job market emerged into daylight? Certainly brighter times are upon us
http://www.planetanalog.com/showArticle.jhtml?articleID=16401444

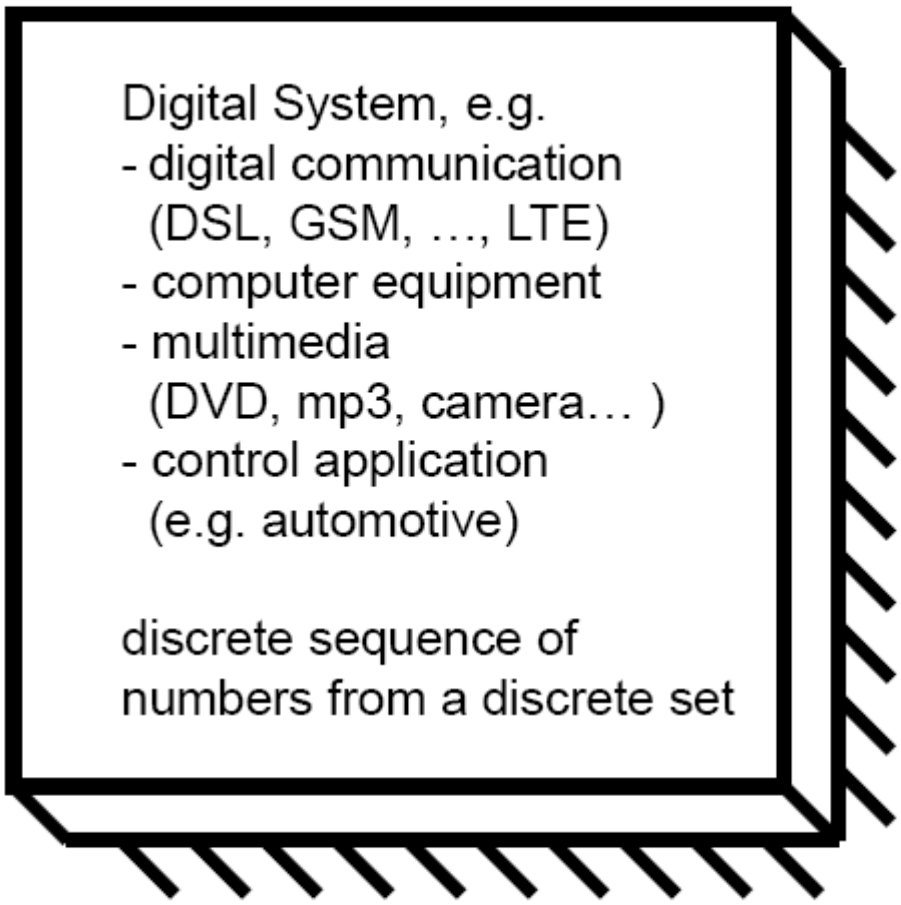
- Consequently, we're seeing analog job requisitions in several key areas including WiFi (wireless LANs and Internet access), ultra wideband technology (UWB) and power management. Demand for designers with expertise in high-speed data conversion seems to be high across a variety of industries.

- At the height of communications funding bubble, designers of Serdes, CDR (clock-data recovery) and PLL (phase-locked loops) could count on receiving 10 job offers almost as soon as they flashed their resumes. While the comms bubble has burst, there remain a number of openings for designers with solid analog experience.

Obituary Note on Jim Williams (Linear Technology) – Most Popular Analog Design Expert !!!

Test equipment has to be more advanced than the circuits it tests. So learning the design of test equipment turned Jim into one of the best analog engineers in the world. He never confused description with understanding. When he would give seminars on how to design piezoelectric transformer lamp drivers, he pointed out that professors who fill the blackboard with math really don't know how a circuit works. Jim knew that the math can describe how a circuit works but understanding how it works was a much more fundamentally intuitive and poetic endeavor.

Analog Applications



Mixed Signal Electronics is a bridge

Analog Applications

- Sensor interface (P, Temp, accel, mass, gas, virus……)
- Bio system
- Audio/video applications
- Digital storage media
  - HDD, CD, DVD, BlueRay, Flash etc
  - USB I/II/wireless USB, 1394 Std.
  - Read/write channel
- Every digital system with high Clk speed
- RF system

Analog Circuit Design Approaches

Approach – I: quantum mechanics → solid state physics → semiconductor device physics → device modelling → design of circuits

Approach – II: semiconductor device as black box → describe behavior of these black box in terms of terminal I and V → design of circuits

Extremely tedious and time consuming

Extremely difficult to identify the cause of the problems

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

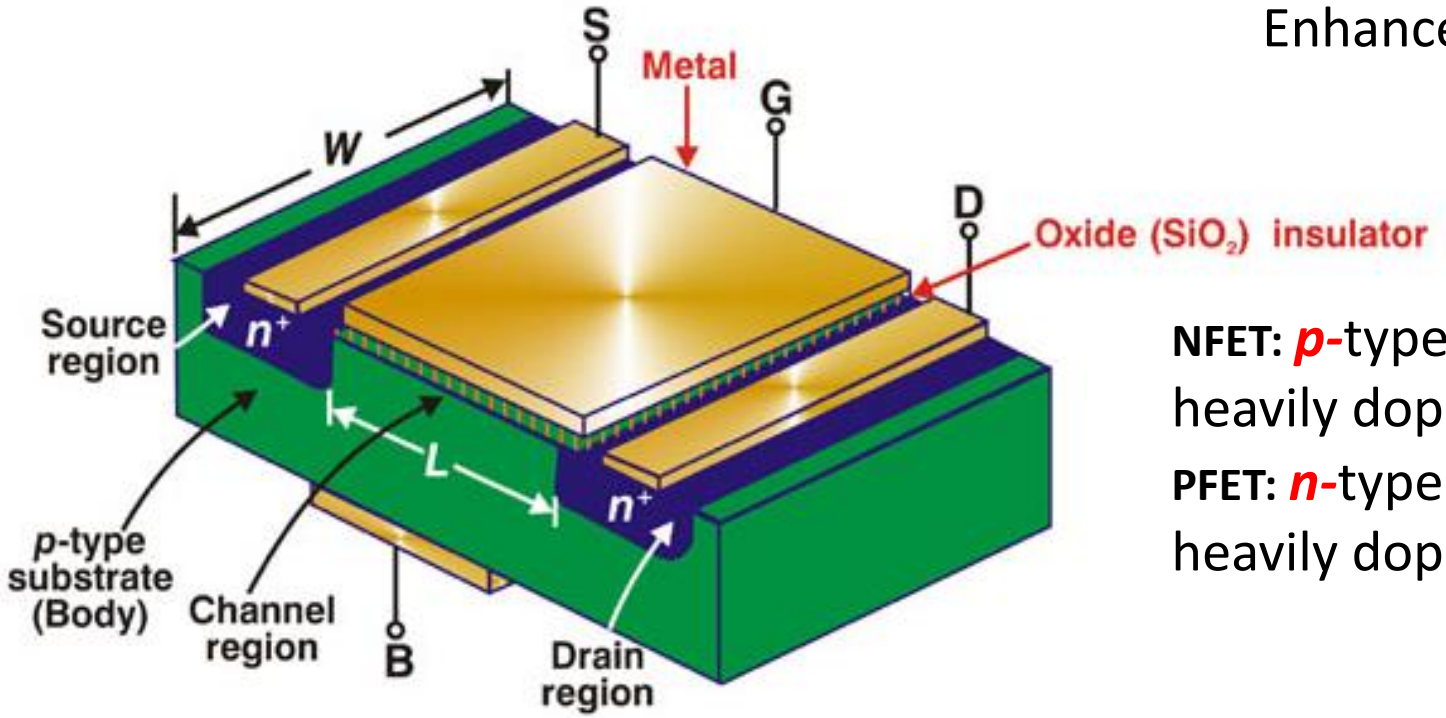
What?

4 terminal device

Gate (G), Drain (D), Source (S), Body (B)

Why?

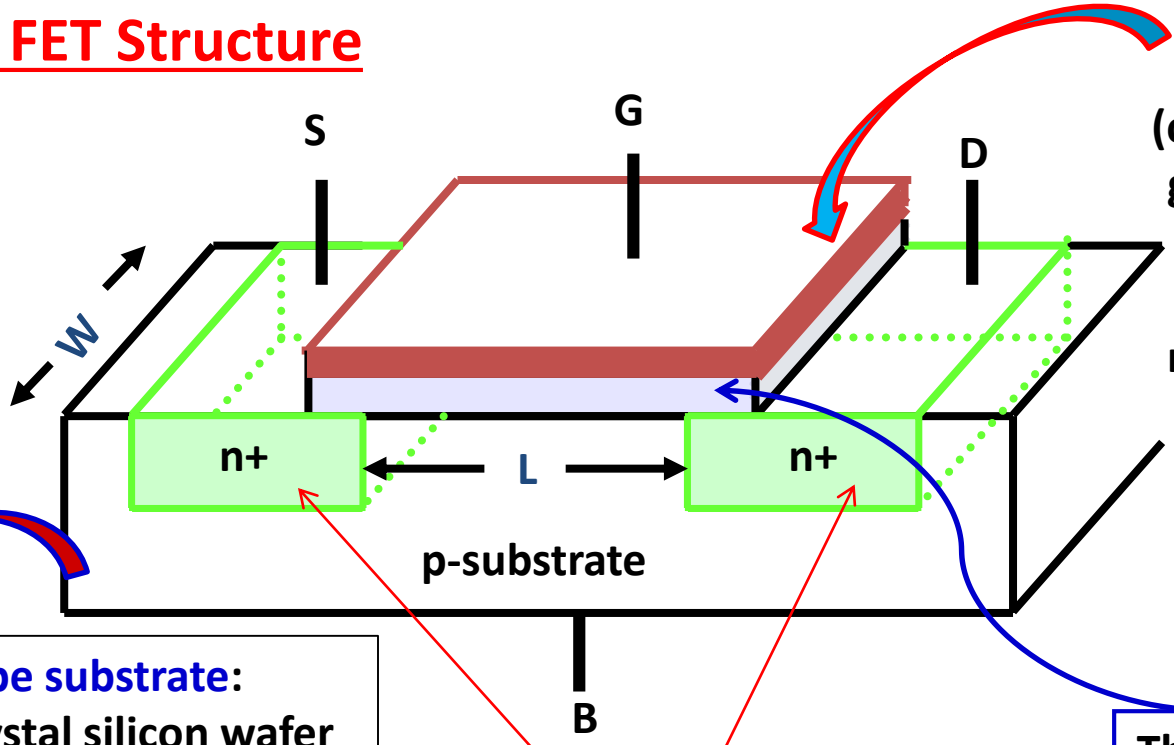
- Ease of Fabrication
- Overall Better Performance
- Cost Effective/Economic
- Continuous Performance Enhancement



NFET: ***p***-type substrate and heavily doped ***n***-regions

PFET: ***n***-type substrate and heavily doped ***p***-regions

NMOS - FET Structure



heavily doped (conductive) polysilicon gate (G) : conductivity can be increased by depositing metal or metal silicide over the gate

***p*-type substrate**: Single crystal silicon wafer that provides physical support for the device

heavily doped n-regions for **source(S)** and **drain (D)**

Thin layer of SiO_2 that insulates G and the substrate

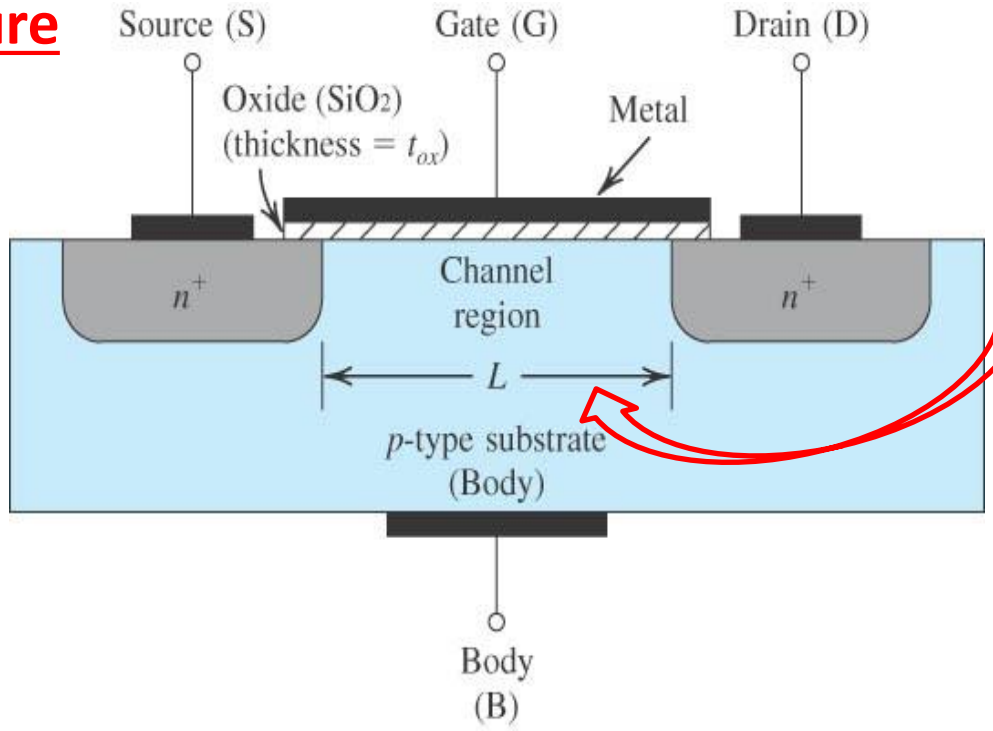
The dimension of the gate along the source-drain path is called the length, **L**, and the perpendicular to the length is called the width, **W**.

NMOS - FET Structure

L = 0.1 to 3 μm

W = 0.2 to 100 μm

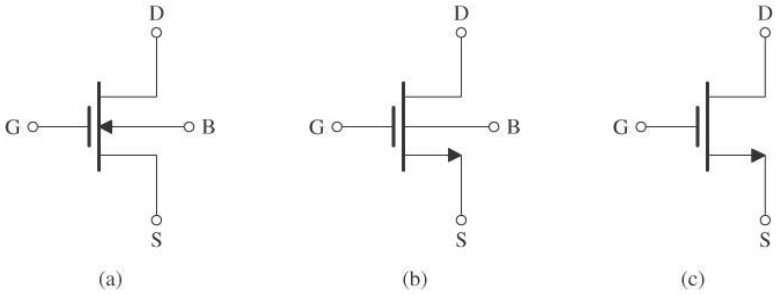
t_{ox}= 2 to 50 nm

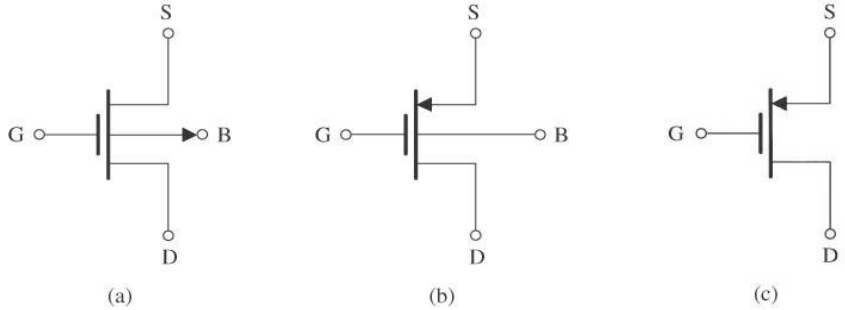


It is the effective length of the channel → takes into account the diffusion that occurs in the implantation of S and D regions

- Silicon Dioxide is essentially glass! Glass is a very good **insulator**—thus, no current can flow from the gate into the MOSFET device!
- Thus, the Silicon Dioxide layer is **sandwiched** between the metal Gate electrode and the p-type channel. It is these **three** materials that give the **MOS**FET its name—**M**etal (Gate electrode) **O**xide (SiO_2) **S**emiconductor (Substrate) FET.

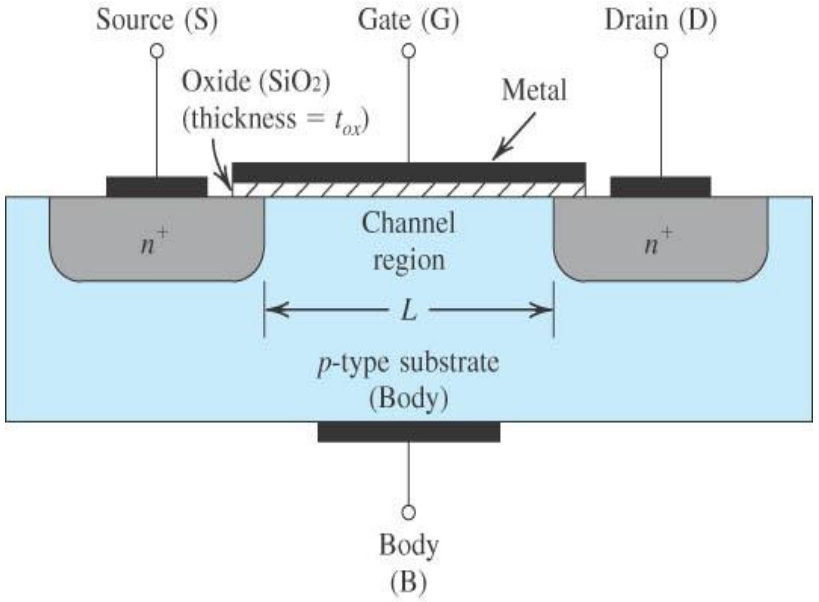
NMOS and PMOS Symbols



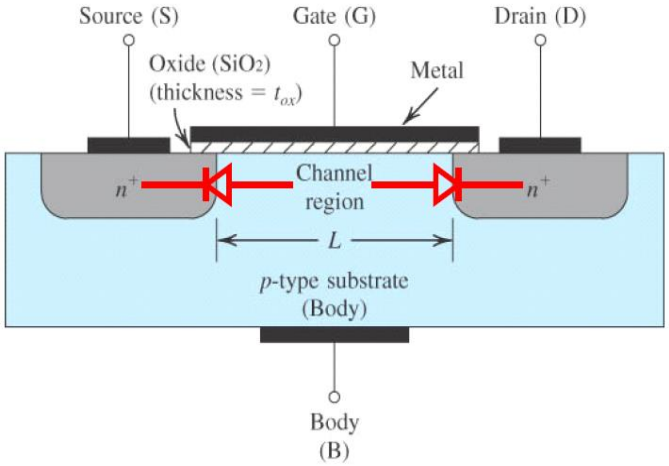


Channel Creation for Current Flow

- First glance at an **NMOS** device: it appears that **no** current can flow from the Drain to the Source (or vice versa) as we must contend with two **p-n junctions**!



- Current cannot flow **into** channel from the Drain, as this requires current flowing from an n-type (cathode) region into a p-type (anode) region.
- Similarly, current cannot flow **into** channel from the Source, as this requires current flowing from an n-type (cathode) region into a p-type (anode) region.
- Note that current **cannot** flow into (or out of) the channel from (into) the **gate**, as the SiO_2 layer is a very good **insulator**!



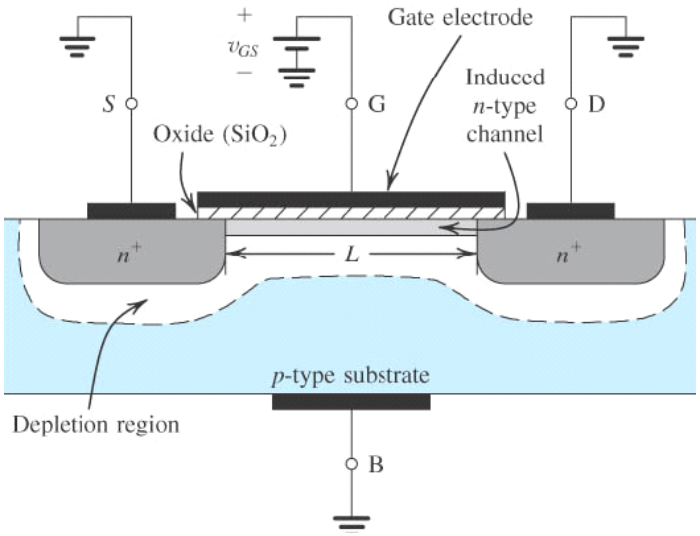
Q: Pardon me, but this NMOS device does **not** appear to be particularly **useful.** I mean, what good is a device if **no** current can flow into it?

A: An NMOS device would indeed be useless **if** no current could flow from drain to source. However, we can **modify** the channel so that this current **can** indeed flow!

We must **induce a channel**—that is, create a thin layer of n-type channel connecting the source and drain!

Channel Creation for Current Flow (contd.)

- **For inducing a channel** - we place a **positive voltage** at the **gate** electrode.
- This creates an **electric field** within the p-type substrate, which pushes the positively charged holes in the p-type substrate away from the gate —a **depletion region** is formed in the Silicon under the gate!



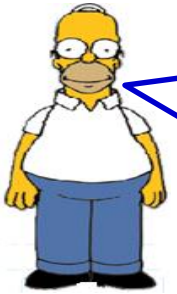
The electric field under the gate will **repel** positively charged holes, but will **attract** negatively charged free electrons!

Q: I see! The minority carriers in the p-type substrate (i.e., **free electrons**) are attracted to the **gate** electrode!

A: True! But we also find that many of the free electrons attracted to the gate come from the **heavily doped** n+ wells called the source and drain.

Channel Creation for Current Flow (contd.)

- There is a Silicon Dioxide **insulator** separating the gate electrode and the Silicon substrate, so the free electrons attracted by the gate simply "**pile up**" at the **top** of the Silicon substrate, just **under** the SiO_2 layer.
- The result is an "**inversion layer**"—A **thin** layer in the p-type silicon where the majority carriers are actually **free electrons**!
- This inversion layer forms **n-type conducting channel** connecting the n^+ **drain** to the n^+ **source**. By applying a positive voltage to the gate, we have **induced a conducting channel**!
- In other words, current flowing from drain to source **no longer** encounters any **p-n junctions**!



Q: So, will **any** positive gate voltage suffice for inducing a channel, **or** must this gate voltage be somehow sufficiently **large**?

A: The later. The gate voltage must be **sufficiently large** to create an inversion layer—it must be sufficiently large to **induce** a conducting channel.

→ In fact, the voltage value must exceed some **threshold (V_T)** ↔ $V_{GS} > V_T$

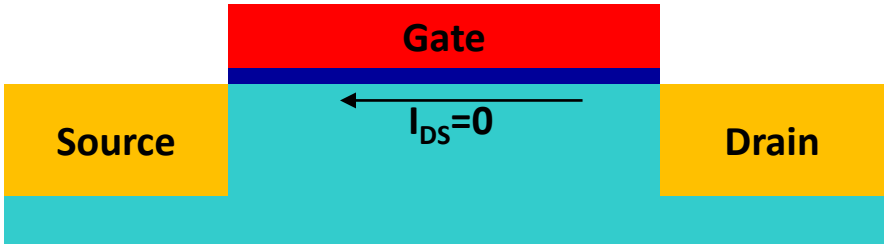
NMOS Qualitative Analysis – Enhancement Type

Assumption: V_{SB} =0

Case-I: $0 \le V_{GS} < V_T$ $V_{GS} < V_T$

V_{GS} : Gate-Source Voltage

V_T : Threshold Voltage **(lies between 0.3 to 0.5 V)**

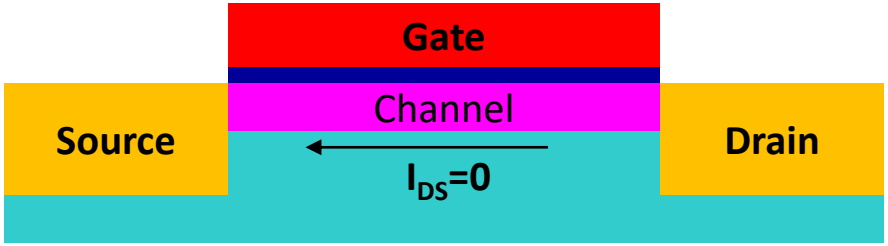


- The channel doesn't exist and therefore no current can flow between D and S
- The transistor is said to be in **cut-off mode**

Home Assignment # 0

Why is V_T always above 0 for an NMOS - FET? **Due by 08.08.2016**

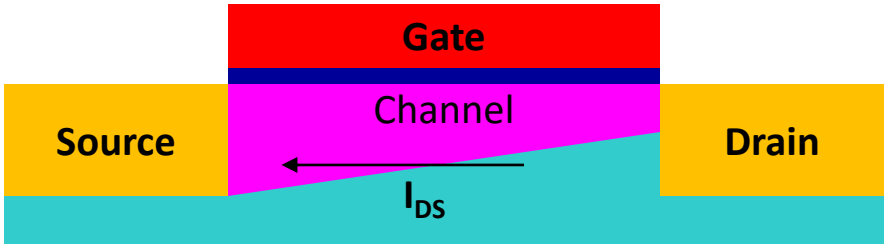
Case-II: $0<V_{GS}$, $V_{GS} \geq V_T$ and $V_{DS}=0$



- The channel forms but still no current flows in the channel.
- The transistor in such a situation behaves as a V_{GS} controlled resistor $\leftrightarrow$ Increase in $V_{GS}-V_T$ results in the increase of channel conductivity and hence reduction in the resistance value.

This process, of increasing the induced channel conductivity by increasing the excess gate voltage, is otherwise known as **channel enhancement**. This is where the **enhancement** MOSFET gets its name!

Case-III: $0<V_{GS}$, $V_{GS} \geq V_T$ and $0<V_{DS}<V_{GS} - V_T$ $\quad V_{DS} < V_{GS} - V_T$



- The transistor operates in **triode mode or linear mode**
- A current proportional to V_{DS} starts to flow from D to S
- The transistor in this state behaves as a voltage controlled resistance
  - Here it has been assumed that $V_{GS} - V_T$ **is constant** and V_{DS} **is varied**

Q: Current! I thought current could **not** flow because of the two p-n junctions in the NMOS device!

A: Remember, that was **before** we applied a sufficient **gate voltage**. With this voltage applied, an n-type channel is **induced,** forming a **conducting channel** from drain to source!

Case-III: $0<V_{GS}$, $V_{GS} \geq V_T$ and $0<V_{DS}<V_{GS}-V_T$

- Recall that because of the SiO_2 layer, the gate current is **zero** (i.e., $I_G = 0$).
- Thus, all current **entering the drain** will **exit the source**. We therefore conclude that: $I_D = I_S$.
- As a result, we refer to the channel current for NMOS devices as simply the **drain current** I_D.

- For small V_{DS} (we will see how small later), the drain current will be **directly proportional** to the V_{DS}:

$$I_D \propto V_{DS}$$

- In other words, if V_{DS} is **zero**, the drain current I_D is **zero**. Or, if the voltage V_{DS} **increases** by 10%, the drain current will likewise **increase** by 10%. Note this is **just like a resistor**!

$$I = \frac{V}{R}$$

$$\therefore I \propto V$$

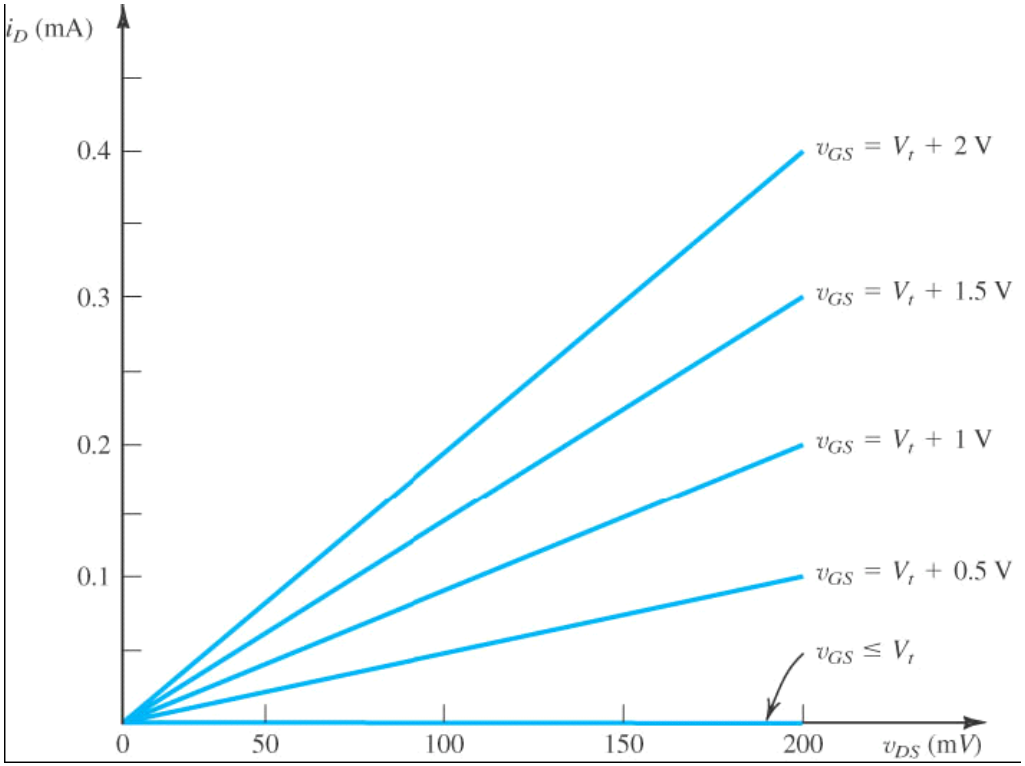
- In other words, we can (for small values of V_{DS}), define a **channel resistance** R_{DS} :

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Case-III: $0<V_{GS}$, $V_{GS} \geq V_T$ and $0<V_{DS}<V_{GS} - V_T$

- Note that this resistance value depends on the **conductivity** of the induced channel—which in turn is dependent on the $\boldsymbol{V_{GS} - V_T}$.
- In other words, the channel behaves like a **voltage controlled resistor** (provided V_{DS} is **small**):

$$R_{DS} = f(V_{GS} - V_T)$$



Q: Yawn! It is apparent that an NMOS transistor is so **simple** that virtually any intergalactic traveler should be able to design **resistor**—right? to understand it. It's just a **voltage controlled resistor**—right?

A: WRONG! Remember, channel resistance R_{DS} **only** has meaning if V_{DS} is **small**—and most often V_{DS} will **not** be small!

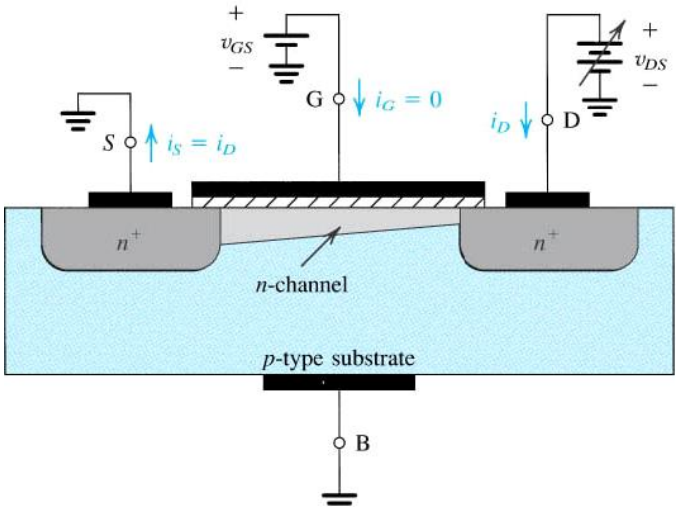
→ As V_{DS} **increases** from our presumably small value, we find that **strange things** start to happen in our **channel**!

Recall that primarily, the **free-electrons** in our inversion layer (the induced channel) were attracted to the **gate** from the heavily doped **n+ drain** and **source**.

→ But the **gate** now has **competition** in attracting these free electrons!

- It was "easy" to attract free electrons to the gate when the **gate voltage** was much **larger** than both the drain and source voltage (i.e., when $\boldsymbol{V_{GS} \gg V_{DS}}$). But as the **drain** voltage increases, it begins to attract **free electrons** of its **own**!

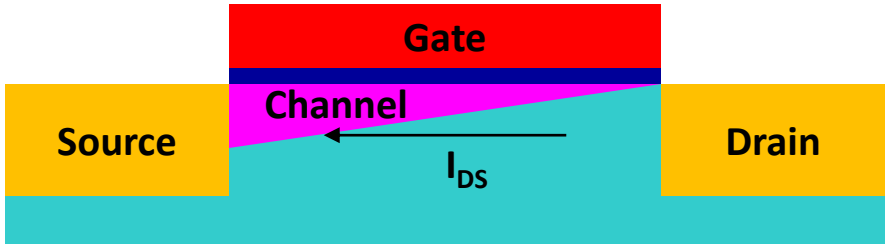
- Recall that **positive current entering** the drain will actually consist mainly of **free electrons exiting** the drain! As a result, the **concentration** of free-electrons in inversion layer will begin to **decrease** in the vicinity of the **drain**.



In other words, **increasing** V_{DS} will result in **decreasing** channel **conductivity**!

Case-IV: $V_{GS} \geq V_T$, $V_{DS} = V_{D(SAT)}$

$$V_{DS} = V_{GS} - V_T$$

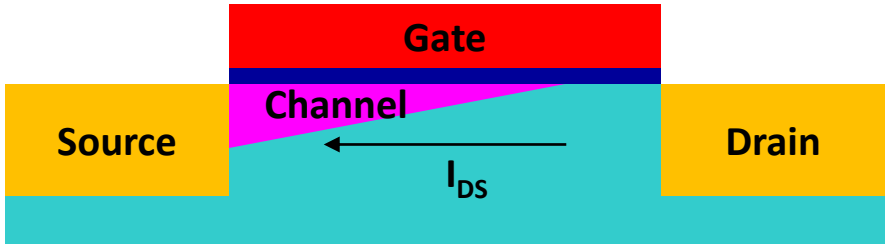


- The channel just reaches the drain
- The channel is reduced to zero inversion charge at the drain
- Drifting of electrons through the depletion region between the channel and drain begins
- This stage is known as **pinch-off**

At pinch-off: there is **no more** increase in drain current as V_{DS} increases.

Case-V: $V_{GS} \geq V_T$, $V_{DS} \geq V_{D(SAT)}$

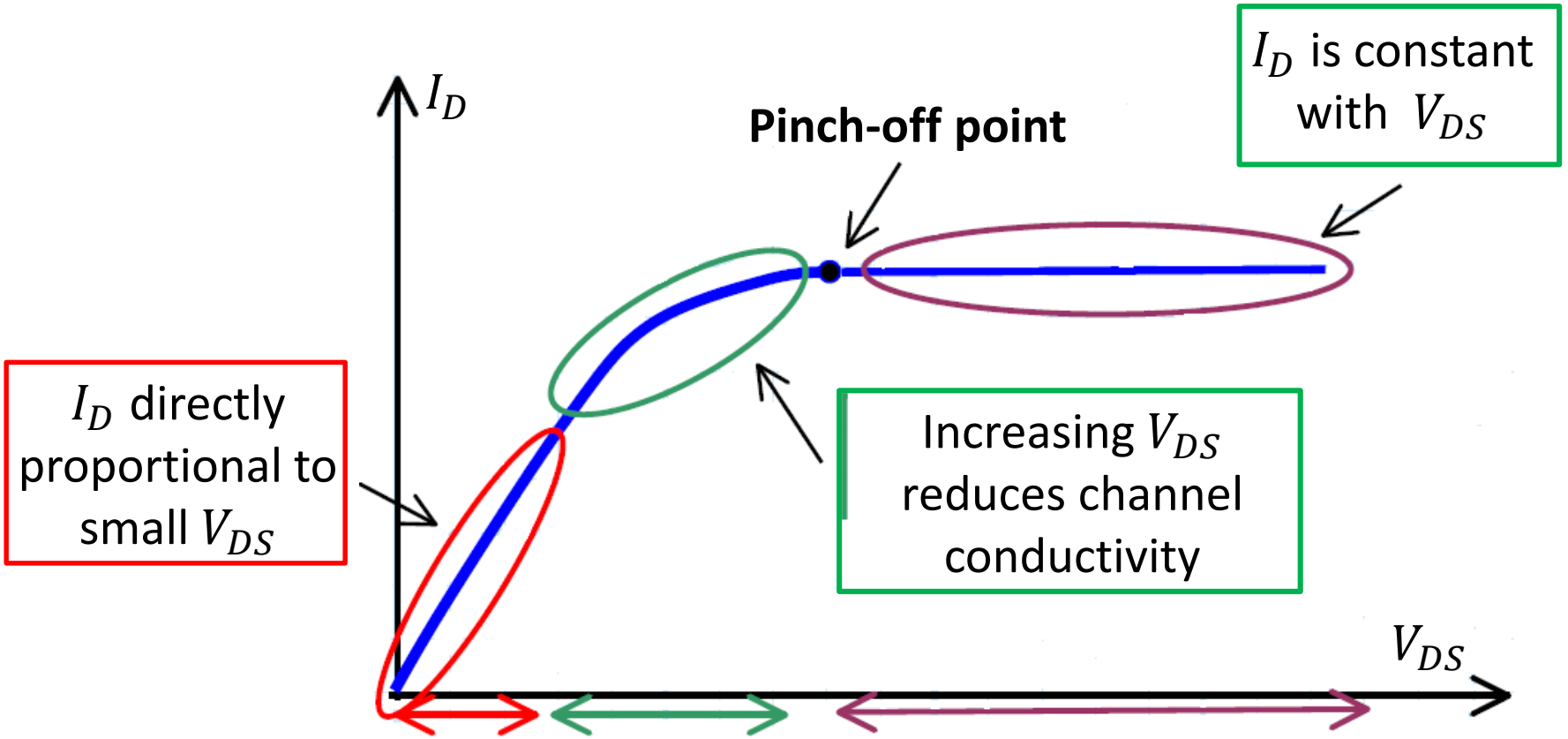
$$V_{DS} > V_{GS} - V_T$$



Q: So, if we **continue** to increase V_{DS} after the channel is "**pinched-off**", does the drain current actually begin to **decrease**?

A: NO! An **interesting** thing happens when the channel is in pinch-off. As we further increase V_{DS}, the drain current I_D will remain **unchanged** (approximately)! That is, the drain current will be a **constant** (approximately) with respect to V_{DS}.

$V_{GS} \geq V_{T,}$ Dependence on V_{DS}:



Summary :

The NMOS characteristic curve has three distinct operation modes:

1. Cutoff - When $\boldsymbol{V_{GS} - V_T < 0}$, **no** channel is induced (no inversion layer is created), and so $I_D = 0$. We call this mode **CUTOFF**.

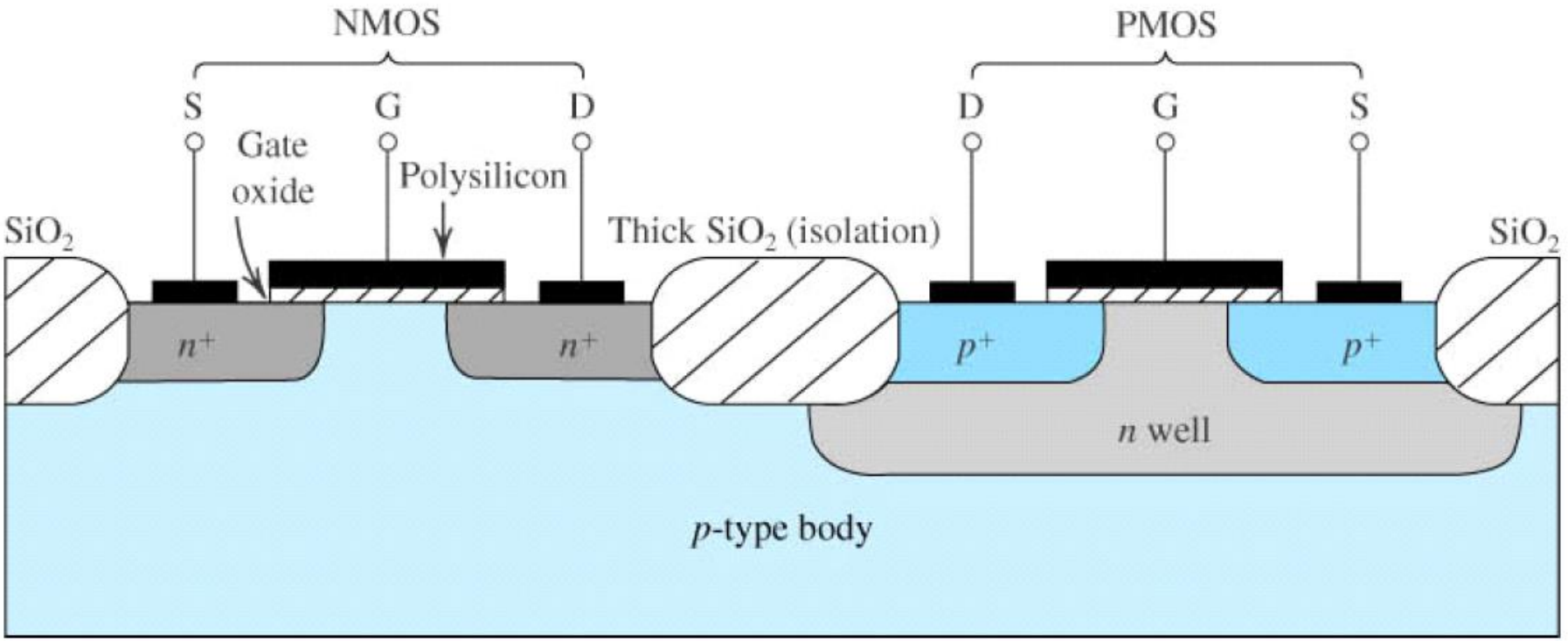
2. Triode - When an induced channel **is** present (i.e., $\boldsymbol{V_{GS} - V_T > 0}$), but the value of V_{DS} is **not** large enough to pinch-off this channel, the NMOS is said to be in **TRIODE** mode.

3. Saturation - When an induced channel **is** present (i.e., $\boldsymbol{V_{GS} - V_T > 0}$), and the value of V_{DS} **is** large enough to pinch-off this channel, the NMOS is said to be in **SATURATION** mode.

PMOS and CMOS

- In addition to an n-channel MOSFET device (i.e., NMOS), we can build p-channel MOSFET (i.e., **PMOS**) device.
- The structure of a PMOS device is essentially the same as an NMOS transistor, except that wherever there **was n-type** Silicon there is **now p-type** Silicon—and wherever there **was p-type** Silicon there is **now n-type** Silicon!
- Specifically, the PMOS channel is part of a **n-type substrate** lying between two heavily doped **p+ wells** beneath the source and drain electrodes.
- Generally speaking, a PMOS transistor is only constructed in **consort** with an NMOS transistor. This “pair” of NMOS and PMOS transistors is known as **C**omplementary **MOS**FETs—**CMOS** for short!

PMOS and CMOS (contd.)



The operation of a PMOS transistor is in many ways **similar** to that of the NMOS device, but in many ways they are also **quite different**!

For a **PMOS** device:

- To create an inversion layer in the **n-type** substrate, we must attract **holes** to the gate → as a result, a **p-type** channel will be induced, connecting the p+ wells at the drain and the source.
- However, to attract **holes** toward the gate, the voltage $\boldsymbol{V_{GS}}$ must be sufficiently **negative**! For PMOS, the threshold voltage $\boldsymbol{V_T}$ is a **negative** value, so that a channel is induced only if $\boldsymbol{V_{GS} < V_T}$ (i.e., $\boldsymbol{V_{GS}}$ is more **negative** than $\boldsymbol{V_T}$) → a channel is induced in a **PMOS** device **only** if $\boldsymbol{V_{GS} - V_T}$ is **negative** (i.e., $\boldsymbol{V_{GS} - V_T < 0}$).
- Similarly, we typically get current to flow through this channel by making the voltage $\boldsymbol{V_{DS}}$ **negative**. If we make the voltage $\boldsymbol{V_{DS}}$ sufficiently **negative**, the **p-type** induced channel will **pinch-off**.
- Note that when $\boldsymbol{V_{DS}}$ is **negative**, the drain current will flow **from** the PMOS **source, to** the PMOS **drain** (i.e., exactly **opposite** that of the NMOS device with a positive $\boldsymbol{V_{DS}}$).

PMOS: I_D *vs* V_{DS} **curve:**