Lecture – 12

Date: 26.09.2016

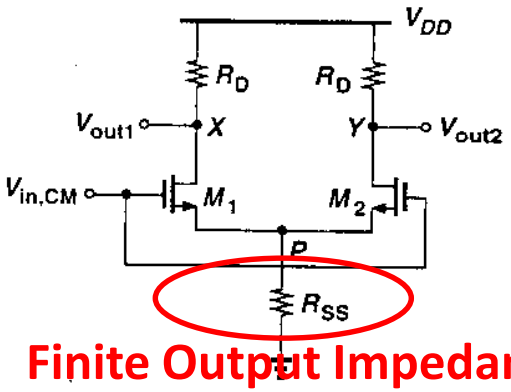
- Differential Pair with Common Mode Input
- Examples
- Common Mode Rejection Ratio

MOS Differential Pair – Common Mode Response

Quantitative Analysis

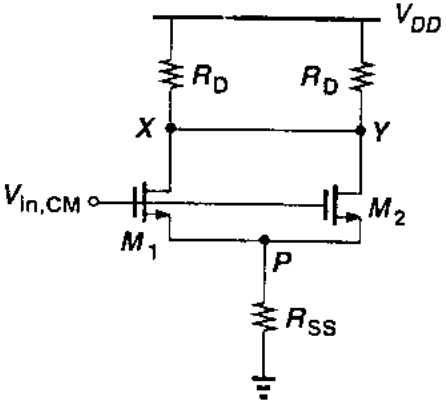
- In ideal condition, differential pair has the ability to suppress variations in the common-mode voltage
- However, in practical scenarios there is always some CM output

Case-I: differential pair is symmetric but the current source has finite output impedance.

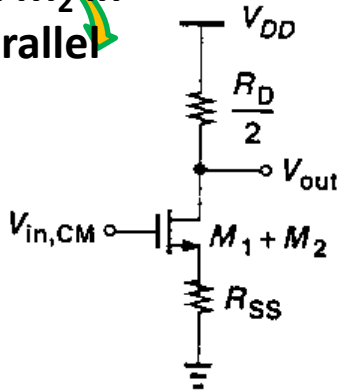


Finite Output Impedance

Symmetry allows shorting of node X and Y as $V_X = V_Y$



It brings M_1 and M_2 in parallel



The CM gain is then: $A_{v,CM} = \dfrac{V_{out}}{V_{in,CM}} = -\dfrac{R_D/2}{1/(2g_m) + R_{SS}}$

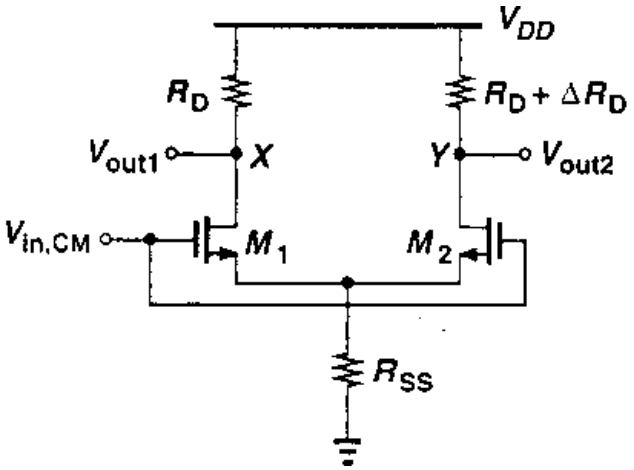
This shows that in a symmetric differential pair, input CM variations disturb the bias points altering the gain

MOS Differential Pair – Common Mode Response (contd.)

Thus the finite output impedance of the tail current source results in some common-mode gain in a symmetric differential pair

In addition, input CM variations also limit the output voltage swings

Case-II: Effect of input common-mode variation when there is mismatch in R_D and the differential pair suffers from finite output impedance of current source.



- What happens to V_X and V_Y as $V_{in,CM}$ increases?
- Since M_1 and M_2 are symmetric → I_{D1} and I_{D2} increases by same amount:

$$\Delta I_D = \frac{g_m}{1+2g_m R_{SS}} \Delta V_{in,CM}$$

- The respective change in V_X and V_Y are given by:

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} \left(R_D + \Delta R_D\right)$$

MOS Differential Pair – Common Mode Response (contd.)

- The differential output due to mis-matched R_D is:

$$\Delta V_X - \Delta V_Y = -\Delta V_{in,CM}\left[\frac{g_m}{1+2g_mR_{SS}}R_D - \frac{g_m}{1+2g_mR_{SS}}R_D - \frac{g_m}{1+2g_mR_{SS}}\Delta R_D\right]$$

$$\therefore \Delta V_X - \Delta V_Y = \left(\frac{g_m}{1+2g_mR_{SS}}\Delta R_D\right)\Delta V_{in,CM}$$

- It is apparent that a small common-mode input can generate a differential mode output → usually denoted by a metric called $A_{CM\text{-}DM}$

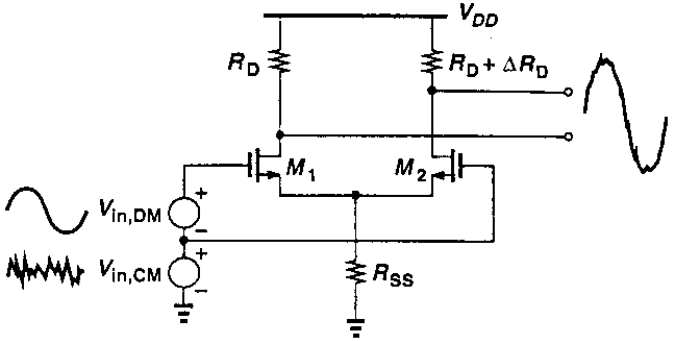
$$A_{CM-DM} = \frac{\Delta V_X - \Delta V_Y}{\Delta V_{in,CM}} = \frac{g_m}{1+2g_mR_{SS}}\Delta R_D$$

Thus a common-mode input introduces a differential component, when the load is mis-matched, at the output

circuit exhibits common-mode to differential conversion

if the input of a differential pair includes both a differential signal and common-mode noise, the output is corrupted version of the input

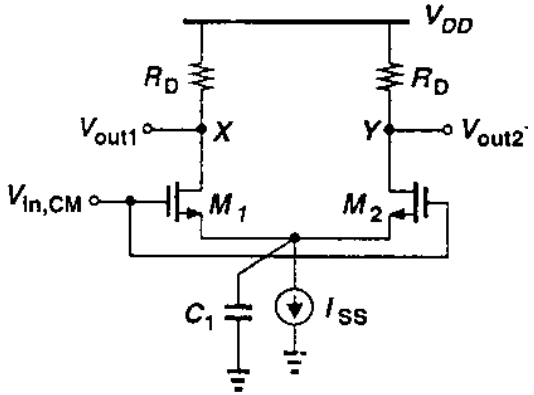
MOS Differential Pair – Common Mode Response (contd.)



Big concern for Analog Circuits

Impact of common-mode to differential conversion

- With the increase in frequency of operation, the total capacitance (arising from the parasitics of the current source and the source-bulk junctions of M_1 and M_2) shunting the tail current source introduces larger tail current variations → **This large variation causes substantial common-mode to differential conversion even for very high output impedance of current source**



Furthermore, The asymmetry due to load impedance mismatch (and hence the resulting common-mode to differential conversion) corrupts the amplified differential output

Common-Mode Response (contd.)

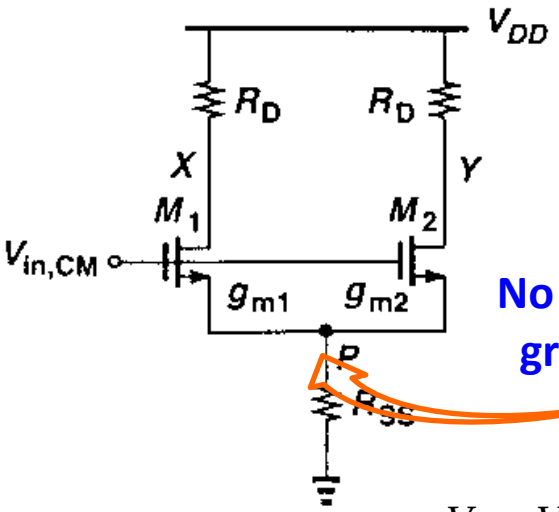
Impact of common-mode to differential conversion

- Summary: the common mode response of differential pairs depend on the output impedance of the tail current and the asymmetries in the circuit → manifestation of two effects
  - Variation of the output CM level (in the absence of mismatches)
  - Shifting of input common-mode variations to higher level at the output
- How about presence of mismatches?
  - Mismatches in R_D and mismatches in transistors (i.e, mismatches in transconductance)
  - The impact of transconductance mismatch on common-mode to differential conversion is more significant

Case-III: Effect of mismatches between M_1 and M_2 (dimension and V_T mismatches)

The asymmetry due to mismatch in the transistors generates slightly different currents in the two paths → leads to unequal transconductance

Common-Mode Response (contd.)



$$I_{D1} = g_{m1}\left(V_{in,CM} - V_P\right) \qquad I_{D2} = g_{m2}\left(V_{in,CM} - V_P\right)$$

$$V_P = \left(I_{D1} + I_{D2}\right)R_{SS}$$

$$\Rightarrow V_P = \frac{\left(g_{m1} + g_{m2}\right)R_{SS}}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1} V_{in,CM}$$

No more AC grounded

$$\Rightarrow V_X = V_{DD} - \frac{g_{m1}}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1} R_D V_{in,CM} \qquad \Rightarrow V_Y = V_{DD} - \frac{g_{m2}}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1} R_D V_{in,CM}$$

$$\therefore V_X - V_Y = -\frac{g_{m1} - g_{m2}}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1} R_D V_{in,CM}$$

- The mismatch in the transistors convert the input CM variations to a differential error by a factor:

$$A_{CM-DM} = \frac{V_X - V_Y}{V_{in,CM}} = -\frac{\Delta g_m R_D}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1}$$

Unwanted

Common-Mode Response (contd.)

- Ideally, this unwanted $A_{CM\text{-}DM}$ is normalized to the wanted A_{DM} → the normalization factor is called CMRR

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

- For a differential pair with mis-matched transistor but operating at equilibrium, the differential gain is:

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}}$$

$$\Rightarrow CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| = \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} = \frac{g_m}{\Delta g_m}(1 + 2g_m R_{SS})$$

- Where, $g_m = (g_{m1} + g_{m2})/2$

Example – 1

- **In the following circuit,** $(W/L)_{1,2} = 50/0.5$, $(W/L)_{3,4} = 10/0.5$ and $I_{SS} = 0.5mA$. Also, I_{SS} is implemented with an NMOS having $(W/L)_{SS} = 50/0.5$ while V_{DD} =3V.
  - **What are the minimum and maximum allowable input CM levels if the differential swings at the input and output are small.**

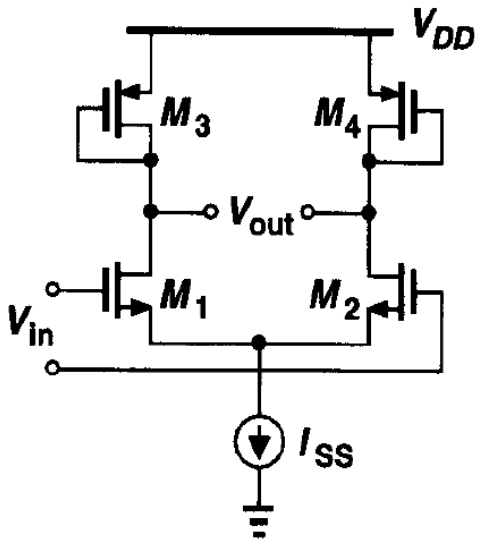


Table 2.1 Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

Example – 1 (contd.)

$$\left(\frac{W}{L}\right)_{SS} = \frac{50}{0.5} \qquad I_{SS} = 05mA \qquad \Rightarrow \qquad (V_{OV})_{SS} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{SS}}} = 0.273V$$

$$I_{D1} = \frac{I_{SS}}{2} = 0.25mA \qquad \Rightarrow \qquad (V_{OV})_1 = 0.193V$$

$$\left(V_{in,CM}\right)_{\min} = V_{GS1} + (V_{OV})_{SS} = 0.7 + 0.193 + 0.273 = 1.17V$$

$$\Rightarrow \qquad \left(V_{in,CM}\right)_{\max} = V_{DD} - |V_{GS3}| + V_{TN} \qquad |V_{GS3}| = |V_{TP}| + \sqrt{\frac{2I_{D3}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3}} = 1.61V$$

$$\therefore \left(V_{in,CM}\right)_{\max} = 3 - 1.61 + 0.7 = 2.09V$$

Example – 2

- **In the following circuit,** $(W/L)_{1,2} = 50/0.5$ and $R_D = 2k\Omega$. Suppose R_{SS} represents the output impedance on an NMOS current source with $(W/L)_{SS} = 50/0.5$ and a drain current of 1mA. The input signal consists of $V_{in,DM} = 1.5V + V_n(t)$, where $V_n(t)$ denotes noise with a peak-to-peak amplitude of 100mV. Assume $\Delta R/R = 0.5\%$.
  - **Calculate CMRR**