Assignment #4

Group strength : 2 (maximum)
Process Technology =65nm

1. Design a cascode (CS-CG) amplifier having a gain of at least 15dB. (Make a design on cadence and other on eldo)

1) Using Resistive load
2) Using Active Load

Constraints for question 1:

1) Vdd <= 1.2 Volt
2) Power <= 0.5m W
3) Length <= 0.5 um

Write each and every step of your designing procedure in the documentation.

2. Design a NMOS-input & PMOS current mirror connected differential amplifier with following specification (implement on cadence or ELDO).

1) Slew Rate >= 12v/ µsec.
2) GB = 10M
3) Load capacitor = 8pf
4) ICMR = 4.5 -1.5

Write all the steps of your designing procedure in the documentation part.
(GB= Gain-bandwidth product and ICMR = input common mode range).