ASSIGNMENT #1

Analog CMOS Circuit Design
(ECE315 /ECE515)

All the simulation must be carried out in Cadence 180nm.

Submission Deadline: 21 August 2016.

1. A three terminal Non linear device shown in Figure - 1 exhibits definite I_1 *vs* V_1, I_1 *vs* V_2, I_2 *vs* V_2 and I_2 *vs* V_1characteristics.

Assume that the Non Linear Device shown in Figure (1) can be modelledas,

$I_1 = f(V_1, V_2)$

$I_2 = g(V_1, V_2)$

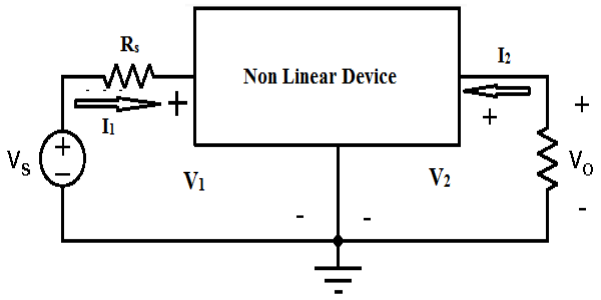

Figure1

Now answer the following Questions (Your Answers must be Qualitative. An intuitive answer leads blunders)

a. Figure (2) shown below depicts I_1 *vs* V_1 characteristics of two Non Linear devices (Device (i) and Device (ii)). Assume that the characteristics I_1 *vs* V_2, I_2 *vs* V_2 and I_2 *vs* V_1 are identical for both the amplifiers. Find out which of the Non Linear devices will yield maximum gain atthe given operating point shown in the figure (**GreenCircle**).

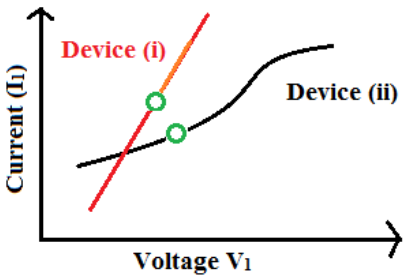

Figure2

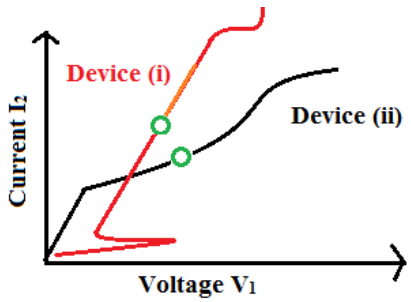

Figure3

b. Figure (3) shown below depicts I_2 *vs* V_1 characteristics of two Non Linear devices (Device (i) and Device (ii)). Assume that the characteristics I_1 *vs* V_2, I_2 *vs* V_2 and I_1 *vs* V_1 are identical for both the amplifiers. Find out which of the Non Linear devices will yield maximum gain atthe given operating point shown in the figure (**Green Circle**).

2. For the circuit shown in **Figure 4:** ***(R_s = 50KΩ, R_g = 50MΩ, R_L = 100KΩ, I = 128 µA, Vt=1V. $\mu C_{ox}(W/L)$ =100µA/V^2)***

a. For the same circuit an Input signal is applied with a frequency of 10 KHz. Find the values of C_1 and C_2.

b. Implement the same using Cadence simulator for the values you got in ***Part a*** and compare the gain of the amplifier with theoretical gain.

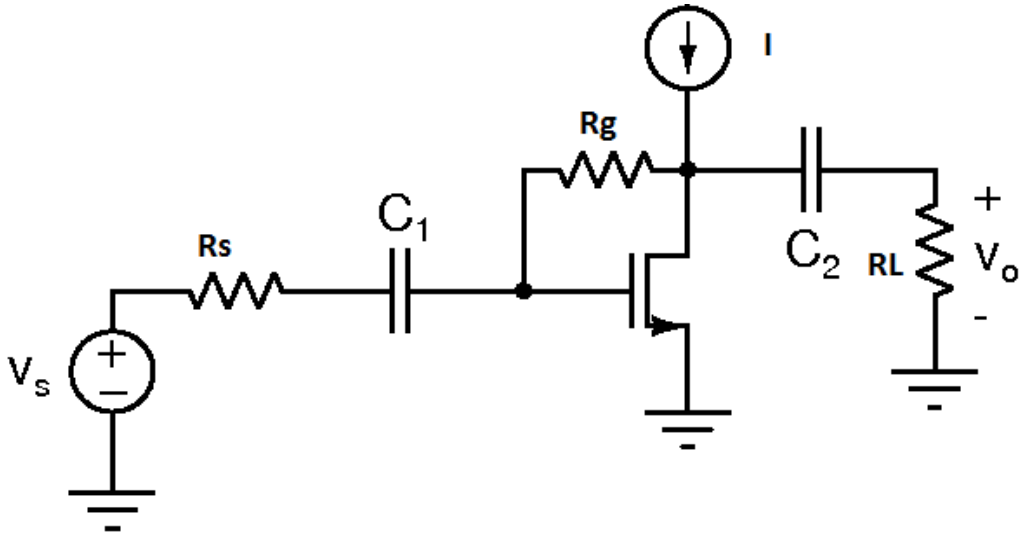

Figure 4

3. Sketch I_x versus V_x for each of the composite structure shown in **Figure 5** with V_G as a parameter. Also , sketch the equivalent transconductance. Assume ƛ= 0. Maximum value of Vx voltage is 3 Volt.

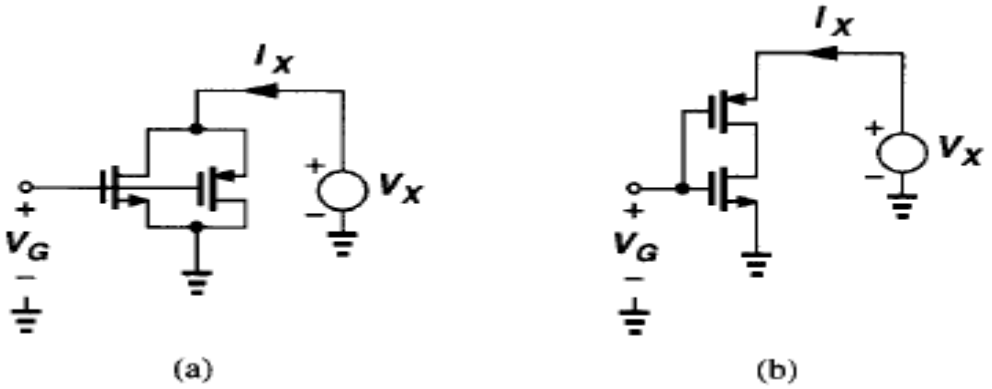

Figure 5

4. Sketch V_x as a function of time for each circuit in the **Figure 6**.

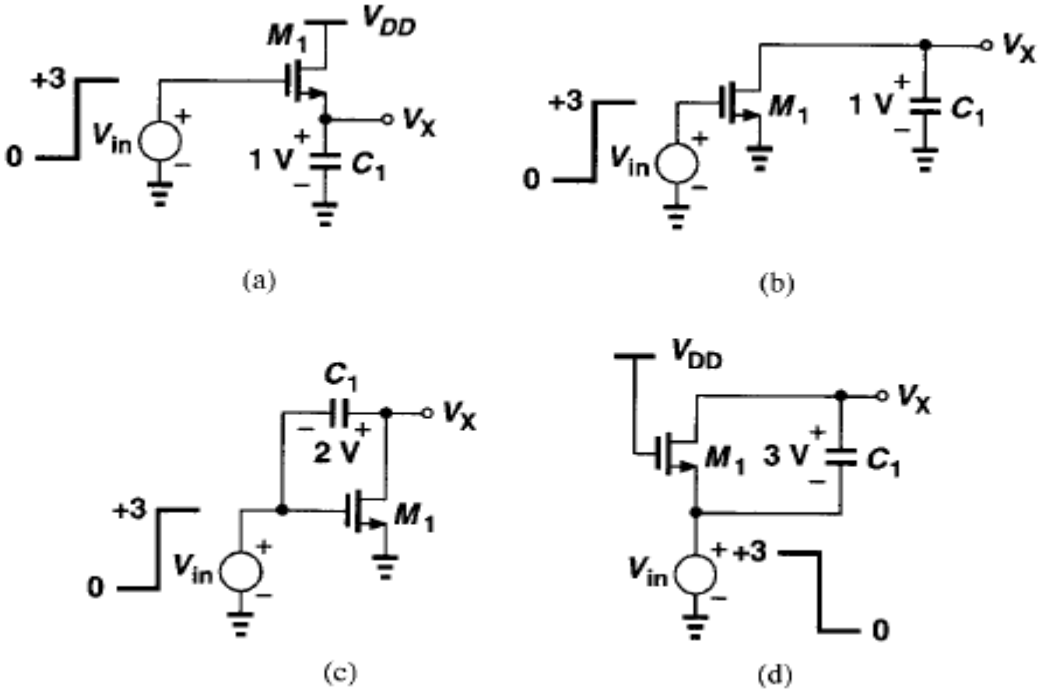

Figure 6