Lecture-3 **Date: 10.08.2015**

- MOSFET – Second Order Effect (contd.)
- Steps for DC Analysis of MOSFET Circuits

Second Order Effect – Body Effect

- In discrete circuit usually there is no body effect as the body is connected to the source terminal.
- In integrated circuit, there are thousands or millions of MOSFET **source terminals** and there is only one Body (B) – the silicon Substrate.
- Thus, if we were to tie (connect) **all** the MOSFET source terminals to the single body terminal, we would be connecting **all** the MOSFET source terminals to each other!

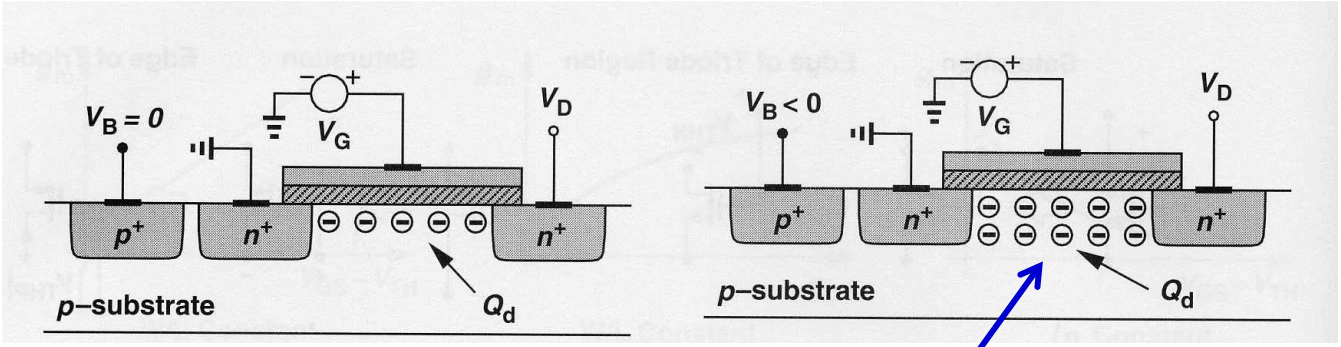
→ This would almost certainly result in a **useless** circuit!

Therefore, for integrated circuits, the MOSFET source terminals are **not** connected to the substrate body.

- Actually, the substrate is connected to the most negative power supply for NMOS circuit for achieving the desired functionality from the device.
- In such a scenario, what happens if the bulk voltage drops below the source voltage?

Second Order Effect – Body Effect

- Now the voltage V_{SB}(voltage source-to-body) is **not** necessarily equal to zero (i.e., $V_{SB} \neq 0$). Thus, we are back to a **four-terminal** MOSFET device.
- There are **many** ramifications of this body effect; perhaps the most significant is with regard to the **threshold voltage** V_T.
- To understand, let us assume $V_S = V_D = V_B = 0$, and V_G is somewhat less than V_T. A depletion region forms but no inversion layer exists.
- As V_B becomes negative, more holes get attracted to the substrate which leaves a larger negative charge behind and as a result the depletion region becomes wider.



Wider depletion region

Second Order Effect – Body Effect

- The wider depletion region leads to increase in threshold voltage given by:

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

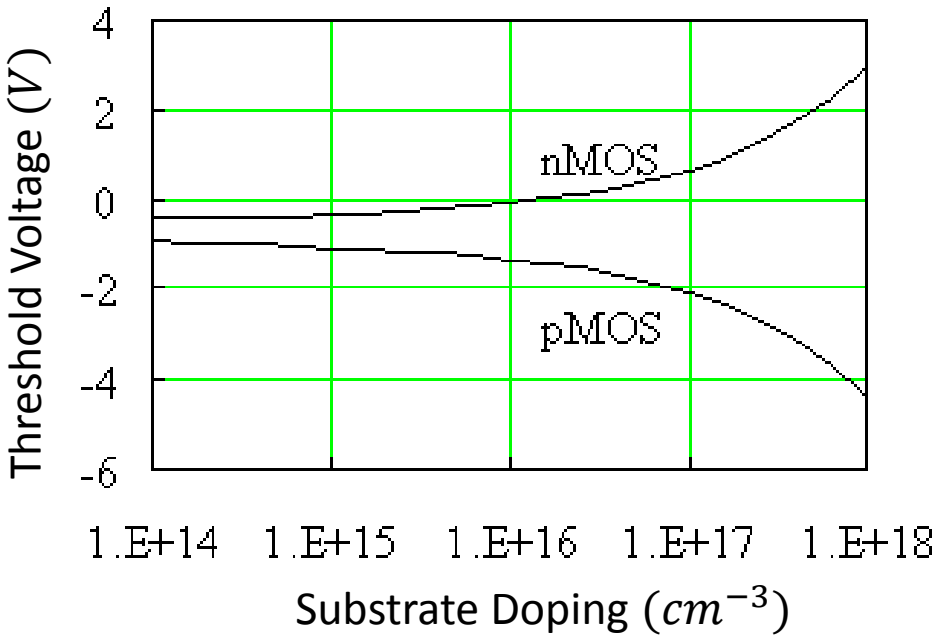
where γ and Φ_F are MOSFET **device parameters** and are essentially process dependent.

- Note the value V_{T0} is the value of the threshold voltage **when** $V_{SB} = 0$ ↔ the value V_{T0} is simply the value of the device parameter V_T that we have been calling the threshold voltage up till now, i.e., without body effect.
- It is thus evident that the term $\gamma\left(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}\right)$ simply expresses an **extra** value added to the "ideal" threshold voltage V_{T0} when $V_{SB} \neq 0$.

Questions

- **Can a circuit designer control threshold voltage?**
- **Body effect is desirable or undesirable?**

Second Order Effect – Body Effect



Second Order Effect – Body Effect (contd.)

- Effect of body effect on Transconductance (g_m).
- Let us check the sensitivity of I_{DS} to V_{SB}

g_m

Simplification Yields:

$$g_{mb} = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{T0})\left(-\frac{\partial V_T}{\partial V_{BS}}\right)$$

$$\left(\frac{\partial V_T}{\partial V_{BS}}\right) = -\left(\frac{\partial V_T}{\partial V_{SB}}\right) = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-\frac{1}{2}}$$

$$\Rightarrow g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m$$

$\eta = g_{mb}/g_m$

η=1/3 to 1/4, bias dependent

Thus, body effect has potential to alter (reduce) transconductance and therefore can impact device performance adversely

Second Order Effect – Body Effect

For many cases, we find that this Body Effect is relatively insignificant, so we will (unless **otherwise** stated) **ignore the Body Effect**.

However, do **not** conclude that the Body Effect is **always** insignificant—it can in some cases have a tremendous impact on MOSFET circuit performance!

Second Order Effect – Subthreshold Conduction

- For $V_{GS} \approx V_T$, a "week" inversion layer still exists and some current flows from D to S.
- Even for $V_{GS}<V_T$, I_D is finite → subthreshold conduction
- For V_{DS} greater than roughly 200 mV:

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_{TM}}$$

$V_{TM} = kT/q$

Nonideality Factor

- When V_{GS} is brought to zero, there will be some drain current in the channel. This is clearly unwanted situation as this small current will cause significant power consumption in large circuits

Second Order Effect – Voltage Limitations

- Various breakdown occurs if their terminal voltage differences exceed certain limits
- At high V_{GS}, the gate oxide breaks down irreversibly
- In short-channel devices, an excessively large V_{DS} can widen the depletion region around the drain so much that it touches that around the source, creating a very large drain current → punch through

Question

- Can channel length modulation affect NMOS/PMOS performance in linear/triode operation mode?

DC Analysis of MOSFET Circuits

- To analyze MOSFET circuit with D.C. sources, we **must** follow these **five steps**:

1. ASSUME an operating mode
2. ENFORCE the equality conditions of that mode.
3. ANALYZE the circuit with the enforced conditions.
4. CHECK the inequality conditions of the mode for consistency with original assumption. If consistent, the analysis is complete; if inconsistent, go to step 5.
5. MODIFY your original assumption and repeat all steps

1. ASSUME

Here we have **three** choices—cutoff, triode, or saturation. You can make an "**educated guess**" here, but remember, until you CHECK, it's just a guess!

2. ENFORCE

For all three operating regions, we must ENFORCE just **one equality**.

- **Cutoff:** Since **no** channel is induced, we **ENFORCE**: $I_D = 0$

- **Triode:** Since the conducting channel **is** induced but **not** in pinch-off, we **ENFORCE**:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right]$$

- **Saturation:** Since the conducting channel **is** induced but **is** in pinch-off, we **ENFORCE**:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_T\right)^2$$

3. ANALYZE

The task in D.C. analysis of a MOSFET circuit is to find **one current** and **two voltages**!

a) Since the gate current I_G is zero ($I_G = 0$) for all MOSFETS in all modes, we need **only** to find the **drain current** $\boldsymbol{I_D}$ - this current value must be **positive** (or zero).

b) We also need to find **two** of the three **voltages** associated with the MOSFET. Typically, these two voltages are V_{GS} and V_{DS}, but given any two voltages, we can find the third using KVL:

$$V_{DS} = V_{DG} + V_{GS}$$

Some hints for MOSFET DC analysis:

1. Gate current $I_G = 0$ **always** !!!
2. Equations sometimes have **two** solutions! Choose solution that is **consistent** with the original ASSUMPTION.

4. CHECK

You do not know if your D.C. analysis is correct unless you CHECK to see if it is consistent with your original assumption!

Q: What exactly do we CHECK?

A: We ENFORCED the mode **equalities**, we CHECK the mode **inequalities.**

We must CHECK **two** separate inequalities after analyzing a MOSFET circuit. Essentially, we check if we have/have not induced a conducting channel, and then we check if we have/have not pinched-off the channel (if it is conducting).

Cutoff

We must only CHECK to see if the MOSFET has a **conducting channel**. If **not**, the MOSFET is indeed in **cutoff**. We therefore CHECK to see if:

$V_{GS} < V_T$ (NMOS) $V_{GS} > V_T$ (PMOS)

Triode

- Here we must first CHECK to see **if** a channel has been induced:

$V_{GS} > V_T$ (NMOS) $V_{GS} < V_T$ (PMOS)

- Likewise, we must CHECK to see if the channel has reached **pinch off**. If **not**, the MOSFET is indeed in the **triode** region. We therefore CHECK to see if:

$V_{DS} < V_{GS} - V_T$ (NMOS) $V_{DS} > V_{GS} - V_T$ (PMOS)

Saturation

- Here we must first CHECK to see **if** a channel has been induced:

$V_{GS} > V_T$ (NMOS) $V_{GS} < V_T$ (PMOS)

- Likewise, we must CHECK to see if the channel has reached **pinch off**. If it **has**, the MOSFET is indeed in the **saturation** region and we need to CHECK:

$V_{DS} > V_{GS} - V_T$ (NMOS) $V_{DS} < V_{GS} - V_T$ (PMOS)

- If the results of our analysis are consistent with **each** of these inequalities, then we have made the **correct** assumption! The **numeric** results of our analysis are then likewise **correct**. We can **stop** working!

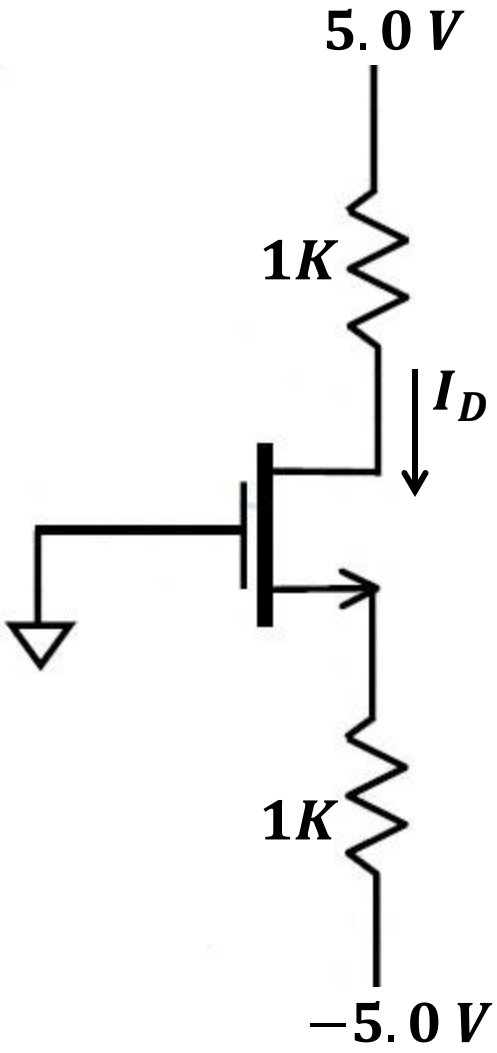
- However, if **even one** of the results of our analysis is **inconsistent** with our ASSUMPTION, then we have made the **wrong** assumption → Time to move to step 5.

5. MODIFY

If **one or more** of the circuit MOSFETSs are **not** in their ASSUMED mode, we must change our assumptions and start **completely** over!

In general, **all** of the results of our previous analysis are incorrect, and thus must be **completely** scraped!

Example – 1



$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right) = K = 0.4mA/V^2$$

$$V_T = 2.0V$$

ASSUME: the NMOS device is in saturation.

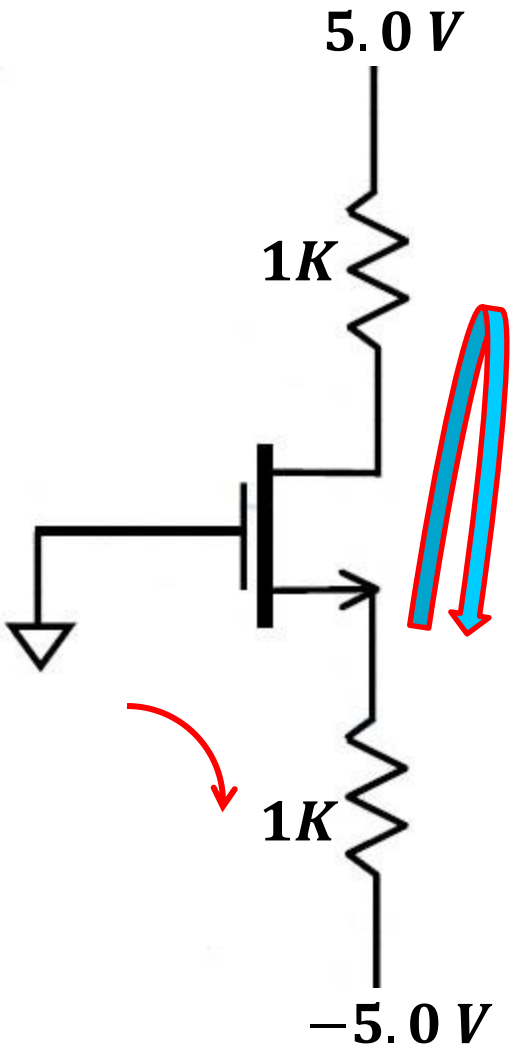
- Thus, we must ENFORCE the condition that:

$$I_D = K\left(V_{GS} - V_T\right)^2$$

- Now we must **ANALYZE** the circuit.

Q: What now? How do we proceed with this analysis?

Example – 1 (contd.)



A: It's certainly not clear. Let's write the circuit equations and see what happens.

- **From the Gate-Source loop KVL:**

$$0 - V_{GS} - 1 \times 10^3 (I_D) = -5.0$$

- **Therefore, rearranging:**

$$I_D = (5.0 - V_{GS})/10^3$$

- **And from the Drain-Source loop KVL:**

$$5 - 1 \times 10^3 (I_D) - V_{DS} - 1 \times 10^3 (I_D) = -5.0$$

- **Therefore, rearranging:**

$$V_{DS} = 10.0 - 2 \times 10^3 (I_D)$$

Example – 1 (contd.)

$$I_D = (5.0 - V_{GS})/10^3 \quad = \boldsymbol{K(V_{GS} - V_T)^2}$$

$$\longrightarrow \quad 0.4mA/V^2\left[V_{GS} - 2\right]^2 = \frac{5 - V_{GS}}{10^3}$$

$$\boldsymbol{V_{GS} = 3.76V}$$

$$\boldsymbol{V_{GS} = -2.26V}$$

- We **assumed** saturation. If the NMOS is in saturation, we know that:

$$V_{GS} > V_T = 2.0V \qquad \boldsymbol{\therefore V_{GS} = 3.76V}$$

- Inserting this voltage into the Gate-Source KVL equation, we find that the drain current is:

$$I_D = (5.0 - 3.76)/10^3 \longrightarrow \boldsymbol{\therefore I_D = 1.24\ mA}$$

- And using the Drain-Source KVL, we find the remaining voltage:

$$V_{DS} = 10.0 - 2 \times 10^3 \times 1.24 \times 10^{-3} \longrightarrow \boldsymbol{\therefore V_{DS} = 7.52\ V}$$

Example – 1 (contd.)

- Even though we have answers (one current and two voltages), we still are not finished, as we now must **CHECK** our solution to see if it is consistent with the saturation mode inequalities.

$$3.76 = V_{GS} > V_T = 2.0$$ ✓

$$7.52 = V_{DS} > V_{GS} - V_T = 1.76$$ ✓

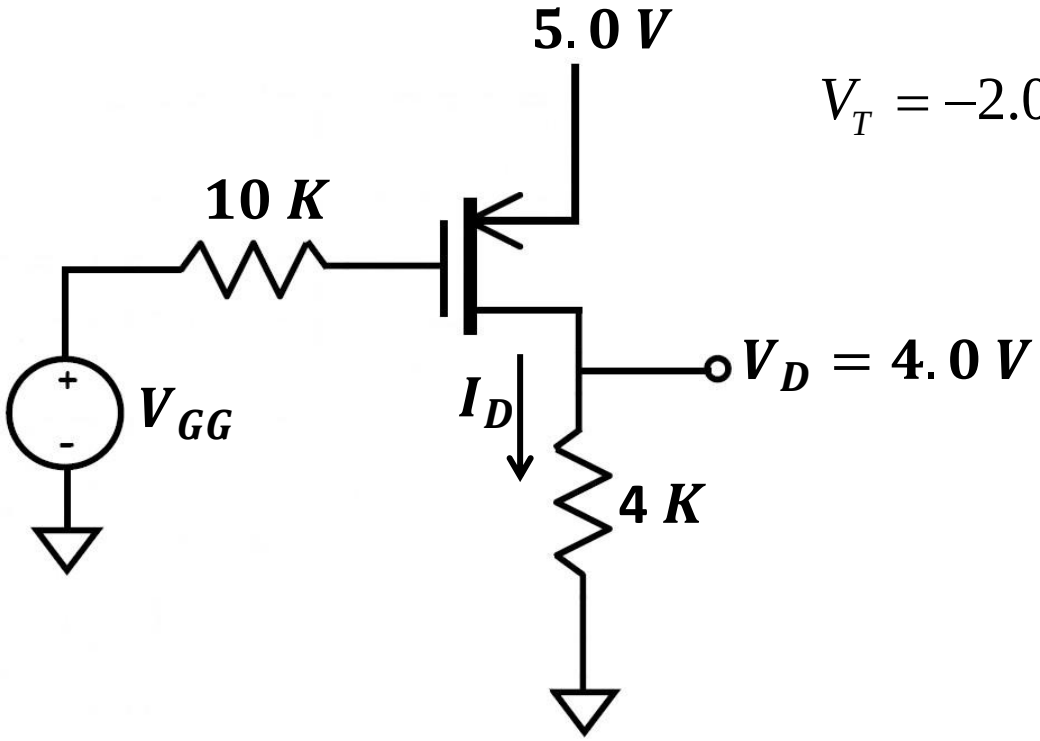
Both answers are consistent! Our solutions are correct!

Example – 2

$$K = 0.2mA/V^2$$

$$V_T = -2.0V$$

Find V_{GG}



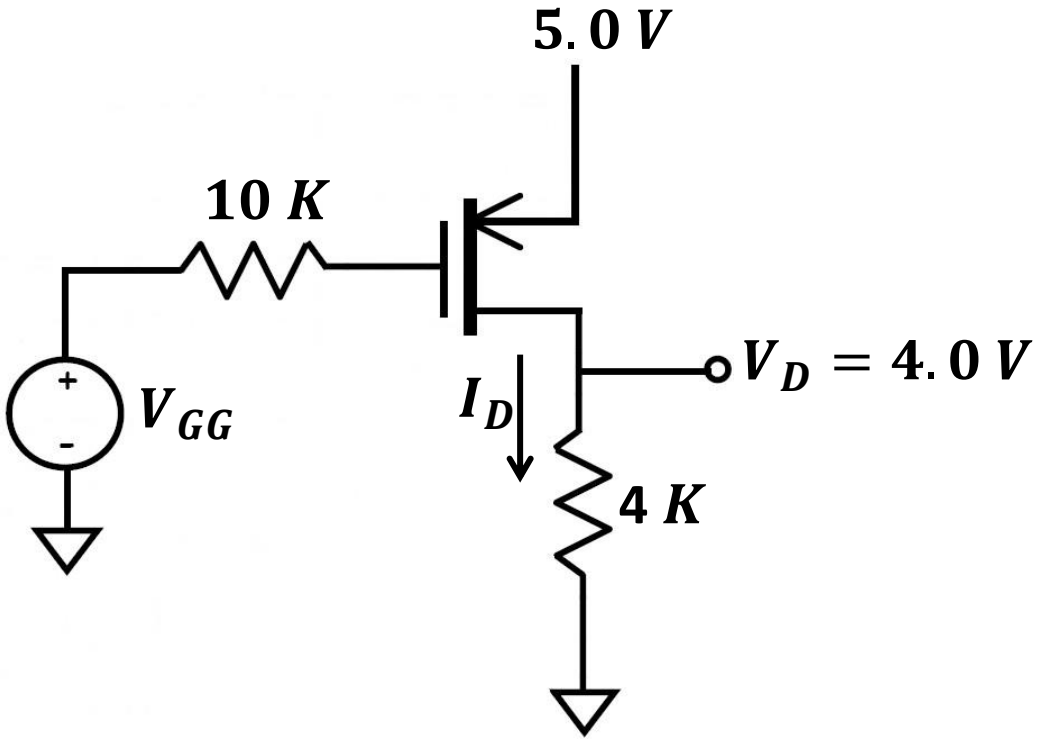
- let's ASSUME that the PMOS is in **saturation** mode.
- Therefore, we ENFORCE the **saturation** drain current equation:

$$I_D = K\left(V_{GS} - V_T\right)^2$$

Example – 2 (contd.)

Q: Yikes! Where do we start ?

A: The best way to start is by "**picking the low-hanging fruit**". In other words, determine the **obvious** and easy values. **Don't** ask, "What is $\mathbf{V_{GG}}$?", but **instead** ask, "What **do** I know?" !



$$I_G = 0.0\ mA \qquad V_S = 5.0\ V$$

$$I_D = \frac{V_D - 0.0}{4\times10^3} = \frac{4}{4\times10^3} = 1mA$$

$$V_G = V_{GG} - 10\times10^3 \times I_G = V_{GG}$$

$$V_{DS} = V_D - V_S = 4 - 5 = -1\ \text{V}$$

$$V_{GS} = V_G - V_S = V_{GG} - 5 \quad \text{V}$$

Example – 2 (contd.)

- We can now relate these values using PMOS **drain current equation**.

$$I_D = K\left(V_{GS} - V_T\right)^2 \quad \Rightarrow \quad 1\times10^{-3} = 0.2\times10^{-3}\times\left(V_{GS} - \left(-2.0\right)\right)^2$$

$$V_{GS} = 0.24 \text{ V} \qquad V_{GS} = -4.23 \text{ V}$$

- For this example, we have ASSUMED that the PMOS device is in **saturation.** Therefore, the gate-to-source voltage must be **less** (remember, it's a **PMOS** device!) than the **threshold voltage**:

$$V_{GS} < V_T$$

$$\therefore V_{GS} = -4.23\ V$$

Q: Does this mean our saturation ASSUMPTION is **correct**?

A: **NO!** It merely means that our saturation ASSUMPTION **might** be correct! We need to CHECK the other inequalities to know for **sure**.

Example – 2 (contd.)

- Now, returning to our circuit **analysis**, we can quickly determine the **unknown** value of $\mathbf{V_{GG}}$. Recall that we **earlier** determined that:

$$V_{GS} = V_G - V_S = V_{GG} - 5\,\text{V} \Rightarrow -4.23 = V_{GG} - 5\,\text{V} \Rightarrow \therefore V_{GG} = 0.77\,\text{V}$$

This solution ($V_{GG} = 0.77V$) is of course true **only if** our original ASSUMPTION was correct. Thus, we must CHECK to see if our **inequalities** are valid.

- We of course already know that the **first** inequality is true—a p-type channel is induced:

$$\boldsymbol{V_{GS} = -4.23V < V_T = -2.0V}$$

- However:

$$V_{DS} = -1.0V \not< V_{GS} - V_T = -2.23\text{V}$$

shows us that our ASSUMPTION was **incorrect**!

Example – 2 (contd.)

→ Time to make a **new** ASSUMPTION and **start over**!

- So, let's **now** ASSUME the PMOS device is in **triode** region. Therefore ENFORCE the drain current equation:

$$I_D = K\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]$$

- Note that most of our **original** analysis was **independent** of our PMOS mode ASSUMPTION. Thus, we **again** conclude that:

$$I_G = 0.0\ mA \qquad V_S = 5.0\ V \qquad I_D = \frac{V_D - 0.0}{4\times10^3} = \frac{4}{4\times10^3} = 1mA$$

$$I_D = \frac{V_D - 0.0}{4\times10^3} = \frac{4}{4\times10^3} = 1mA \qquad V_G = V_{GG} - 10\times10^3 \times I_G = V_{GG}$$

$$V_{DS} = V_D - V_S = 4 - 5 = -1\ \text{V} \qquad V_{GS} = V_G - V_S = V_{GG} - 5\ \text{V}$$

Example – 2 (contd.)

- Now, inserting these values in the **triode drain current equation**:

$$1\times10^{-3} = 0.2\times10^{-3}\times\left[2\left(V_{GS}-\left(-2.0\right)\right)\left(-1.0\right)-\left(-1.0\right)^{2}\right]$$

- Solving for V_{GS} we find: $V_{GS} = -5.0V$

- Therefore: $V_{GG} = V_{GS} + 5.0 = -5.0 + 5.0 = 0$

The voltage source $\boldsymbol{V_{GG}}$ is equal to **zero**—provided that our triode ASSUMPTION was **correct**.

- First, we CHECK to see if a channel has indeed been **induced.**

$$\boldsymbol{V_{GS} = -5.0V < V_T = -2.0V}$$

Example – 2 (contd.)

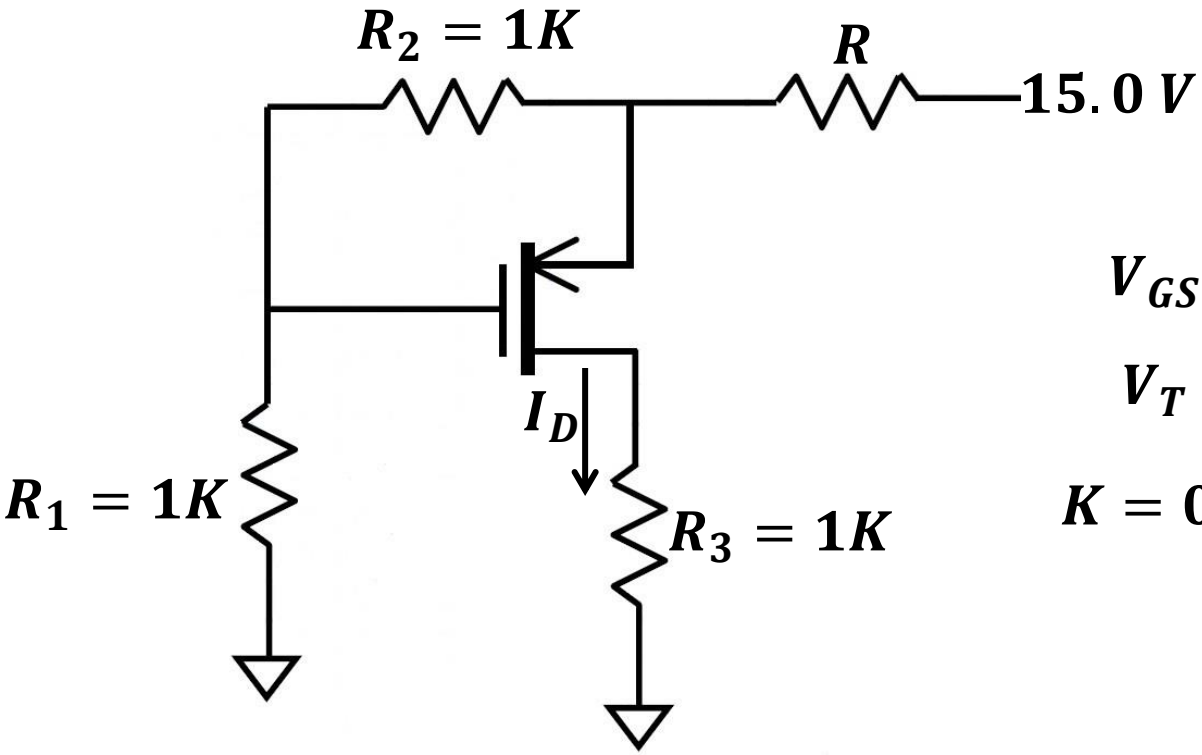
- Next, we CHECK to make sure that our channel is **not** in pinch off.

$$V_{DS} = -1.0V > V_{GS} - V_T = -3.0\text{V}$$

Our **triode** ASSUMPTION is **correct**! Thus, the voltage source $\boldsymbol{V_{GG} = 0.0\ V}$.

Example – 3

- Consider the **PMOS** circuit below, find the value of unknown of resistor R.



$$V_{GS} = -4.0\ V$$

$$V_T = -2.0\ V$$

$$K = 0.75\ {}^{mA}/_{V^2}$$