Lecture-14

Date: 08.10.2015

- MOS Differential Pair – Small Signal Analysis
- Differential Pair with Common Mode Input
- Examples

Lecture 13 - Review

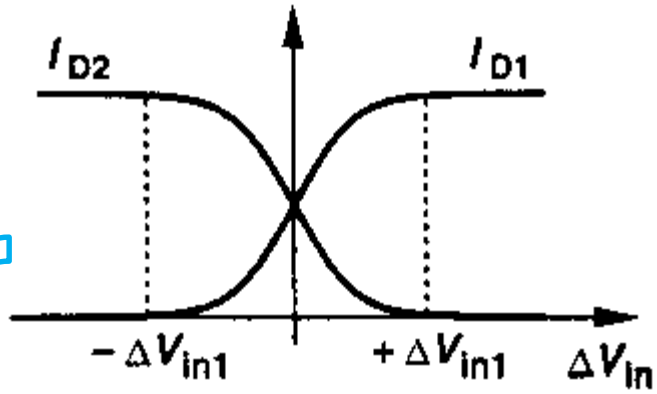
Quantitative Analysis – differential input

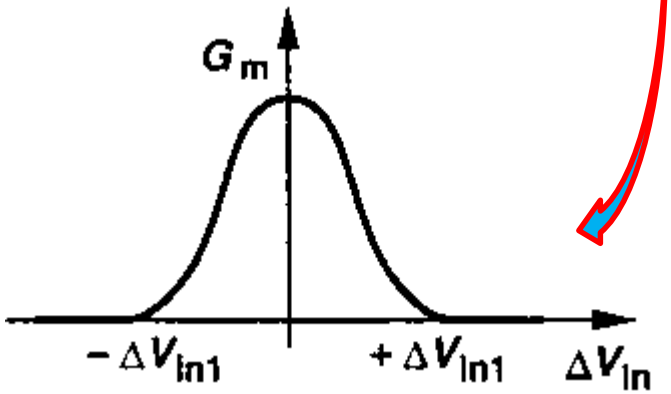
$$G_m = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\frac{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

G_m falls to zero for

$$\Delta V_{in} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

ΔV_{in1} represents the maximum differential signal a differential pair can handle.

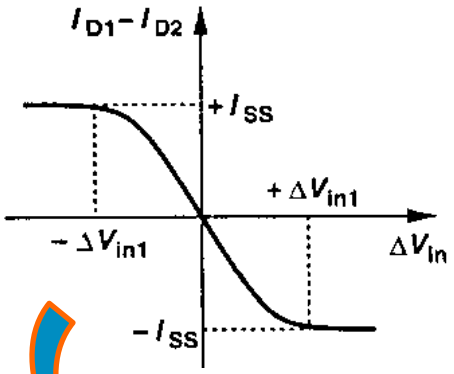




Beyond $|\Delta V_{in1}|$, only one transistor is ON and therefore draws all of the I_{SS}

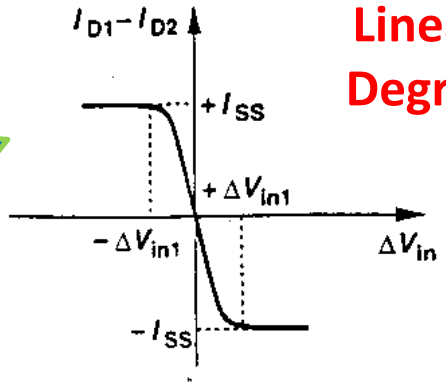
Lecture 13 - Review

Quantitative Analysis – differential input



I_{SS} Constant

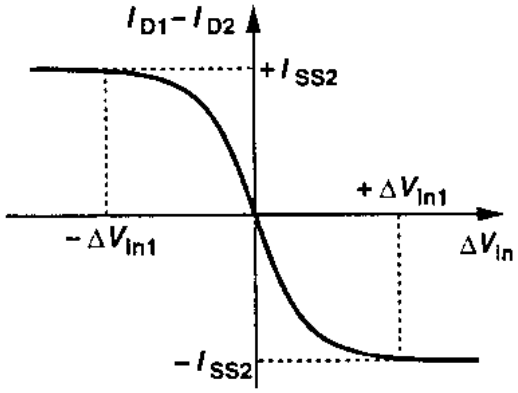
Reduce ΔV_{in1} → by increasing W/L



Linearity Degrades

W/L Constant

Increase ΔV_{in1} → by increasing I_{SS}



Linearity Improves

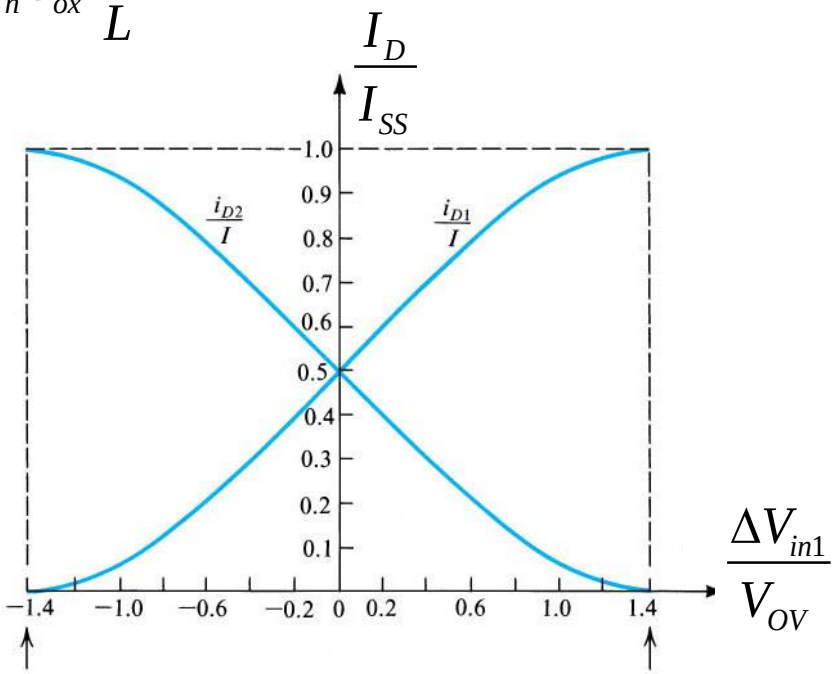
Linearity of a differential pair can be improved by decreasing W/L and/or increasing I_{SS}

Lecture 13 - Review

Quantitative Analysis – differential input

- The equilibrium overdrive (i.e, when M_1 and M_2 are drawing equal portion of I_{SS}) is given by:

$$(V_{GS}-V_T)_{1,2}=\sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} \quad \Rightarrow \quad (V_{OV})_{1,2}=\frac{\Delta V_{in1}}{\sqrt{2}}$$



$$-\Delta V_{in1}=-\sqrt{2}V_{OV} \qquad \Delta V_{in1}=\sqrt{2}V_{OV}$$

MOS Differential Pair – small signal analysis

Quantitative Analysis – differential input

- From large signal analysis we achieved:

$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} R_D$$

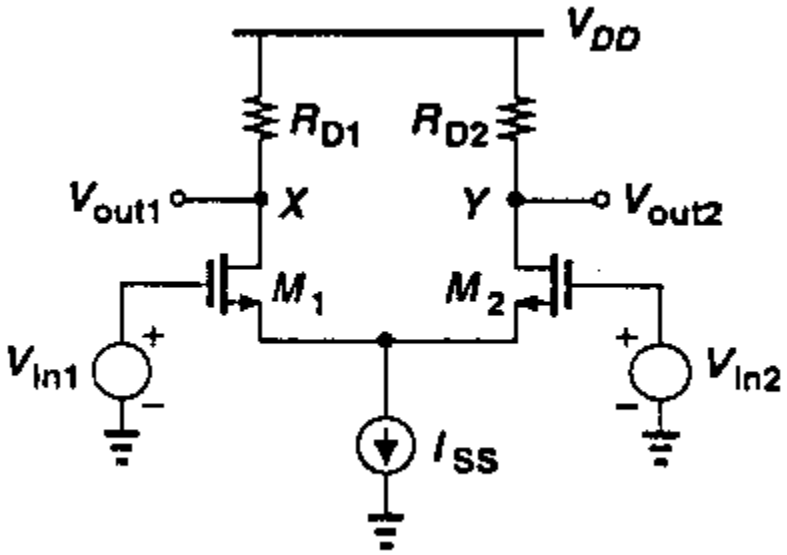
$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = g_m R_D$$

At equilibrium, this is g_m

- How to arrive at this result using small signal analysis?
  - Two techniques
    - Superposition method
    - Half-circuit concept

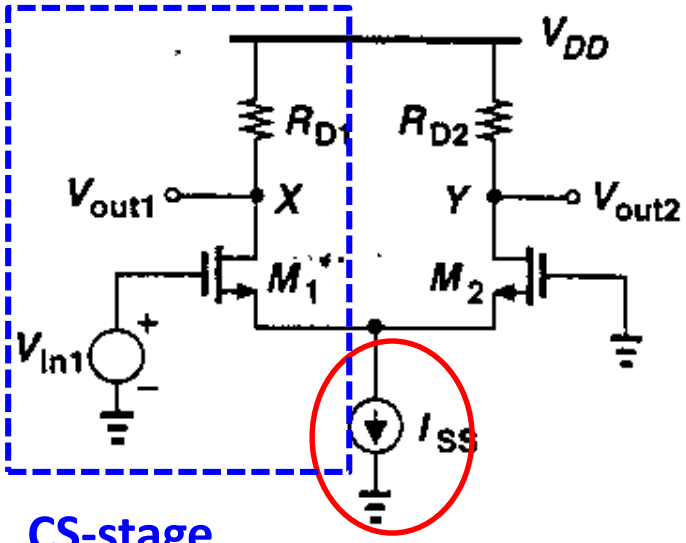
MOS Differential Pair – small signal analysis

- We apply small signals to V_{in1} and V_{in2} and assume M_1 and M_2 are already operating in saturation.



MOS Differential Pair – small signal analysis

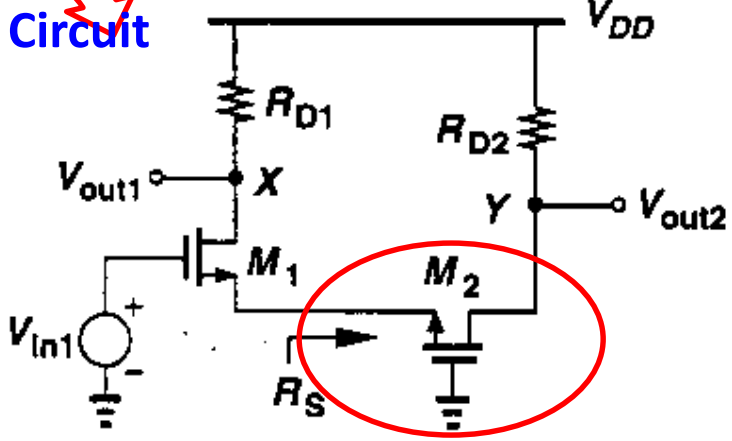
- **Method-I:** Superposition technique – in this the idea is to see the effect of V_{in1} and V_{in2} on the overall output and then combine them to get the differential small signal voltage gain
- First set, $V_{in2} = 0$
- Then let us calculate V_X/V_{in1}



CS-stage

This is open for small signal analysis

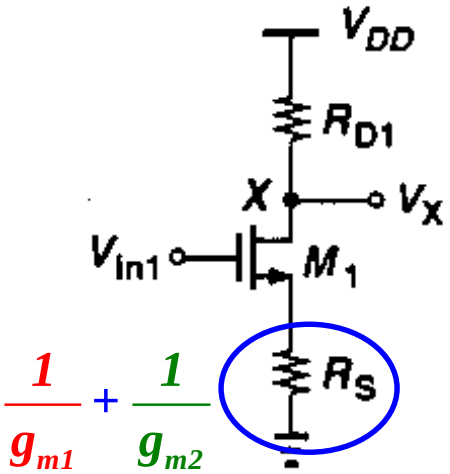
Simplified Circuit



Input impedance of M_2 Provides degeneration resistance to CS-stage of M_1

MOS Differential Pair – small signal analysis

- **Superposition technique**



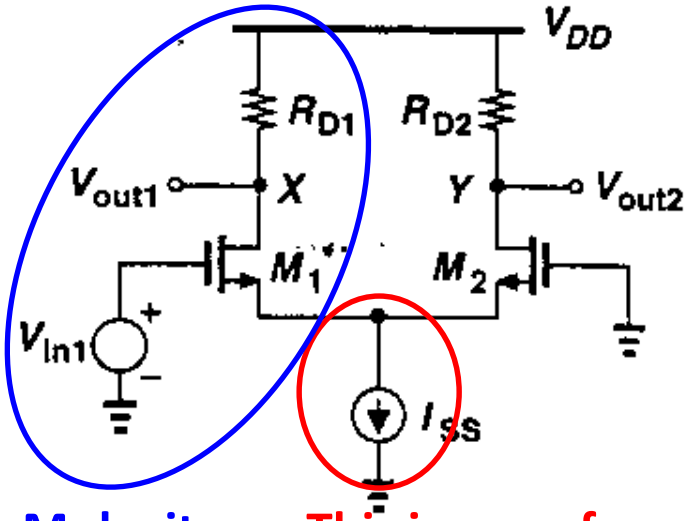
Apply the CS-stage formulation

$$\frac{V_X}{V_{in1}} = \frac{-R_{D1}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

$$\therefore \frac{V_X}{V_{in1}} = \frac{-R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

MOS Differential Pair – small signal analysis

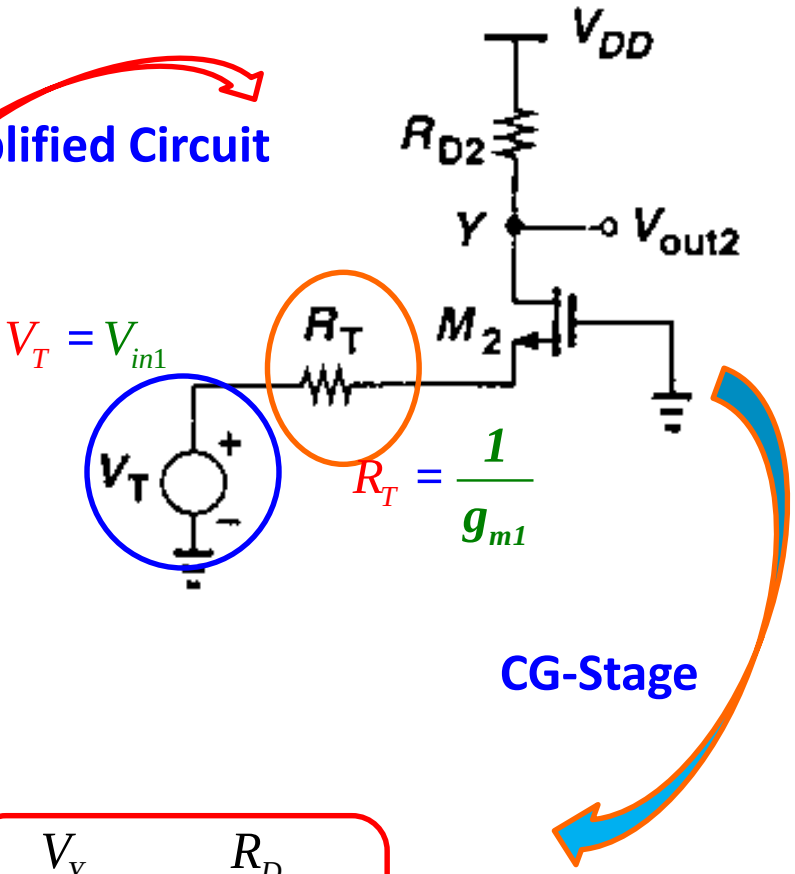
- **Superposition technique**
  - **Now calculate V_Y/V_{in1}**



Replace M_1 by its Thevenin Equivalent Circuit

This is open for small signal analysis

Simplified Circuit



CG-Stage

$$\therefore \frac{V_Y}{V_{in1}} = \frac{R_D}{\frac{1}{g_{m2}} + \frac{1}{g_{m1}}}$$

MOS Differential Pair – small signal analysis

- **Superposition technique**
  - **Now combine the expressions to calculate small signal voltage only due to V_{in1}**

$$\frac{(V_X - V_Y)|_{due\_to\_V_{in1}}}{V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

For matched transistors

$$(V_X - V_Y)|_{due\_to\_V_{in1}} = -g_m R_D V_{in1}$$

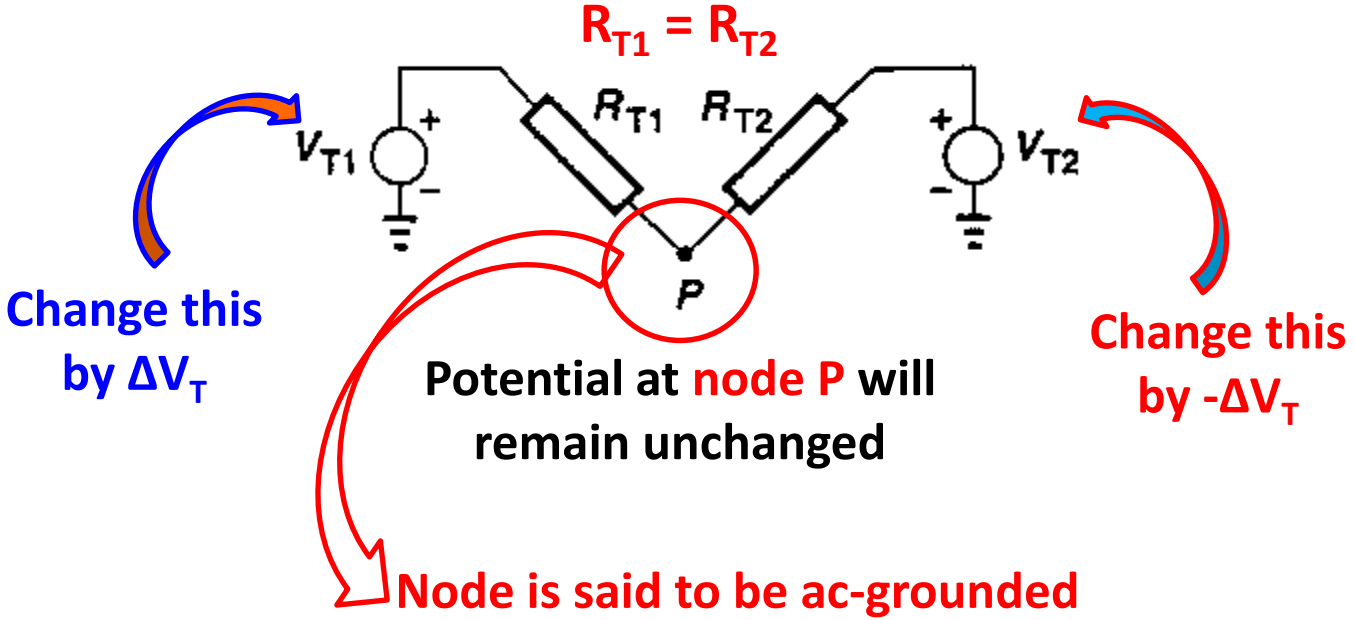
- **Similarly:** $(V_X - V_Y)|_{due\_to\_V_{in2}} = g_m R_D V_{in2}$

- **Superposition gives:** $A_v = \frac{(V_X - V_Y)_{total}}{V_{in2} - V_{in1}} = -g_m R_D$

- **The magnitude of differential gain is $g_m R_D$ regardless of how the inputs are applied**
- **The gain will be halved if single ended output is considered**

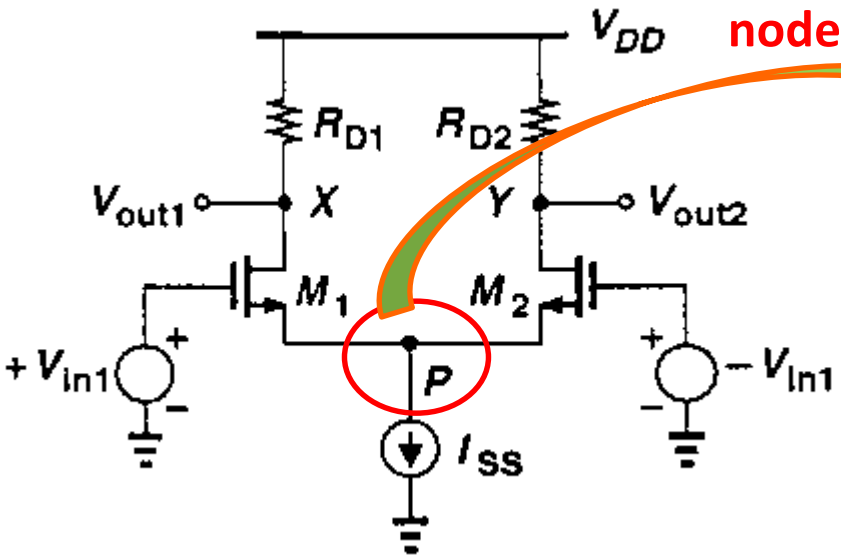
MOS Differential Pair – small signal analysis

- **Half Circuit Approach**
  - If a fully symmetric differential pair senses differential inputs (i.e, the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of half circuit can be applied.

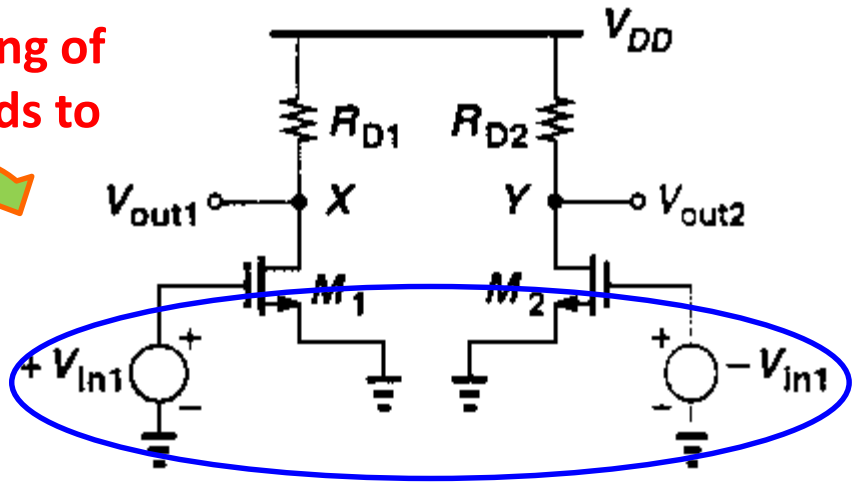


MOS Differential Pair – small signal analysis

- **Half Circuit Approach**



Ac grounding of node P leads to



V_{in1} and $-V_{in1}$ are the change in input voltage at each side

We can write:

$$\frac{V_X}{V_{in1}} = -g_m R_D \qquad \frac{V_Y}{-V_{in1}} = -g_m R_D$$

Therefore the differential output can be expressed as:

$$V_X - V_Y = 2V_{in1}\left(-g_m R_D\right)$$

Thus the small signal voltage given is:

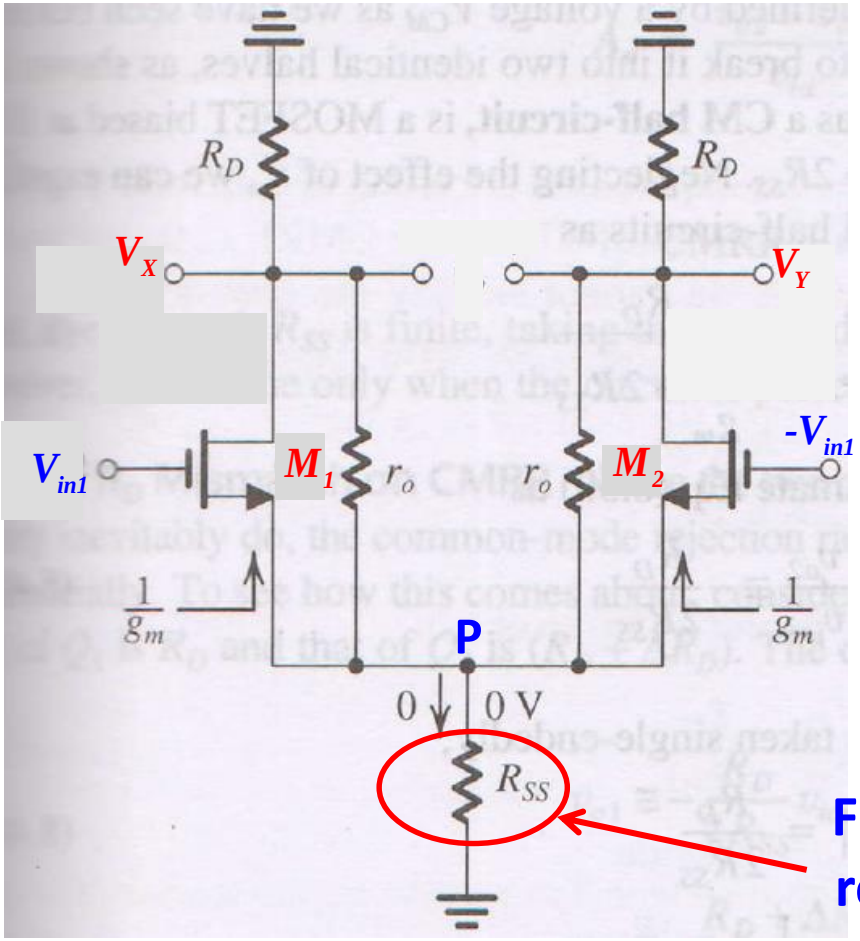
$$A_v = \frac{V_X - V_Y}{2V_{in1}} = -g_m R_D$$

MOS Differential Pair – small signal analysis

- How does the gain of a differential amplifier compare with a CS stage?
  - For a given total bias current I_{SS}, the value of equivalent g_m of a differential pair is $1/\sqrt{2}$ times that of g_m of a single transistor biased at the I_{SS} with the same dimensions. Thus the total gain is proportionally less.
  - Equivalently, for given device dimensions and load impedance, a differential pair achieves the same gain as a CS stage at the cost of twice the bias current.
- What is the advantage of differential stage then?
  - Definitely the noise suppression capability. Right?

MOS Differential Pair – small signal analysis

- How is gain affected if channel length modulation is considered?



- Effect of r_0 on the gain

→ the circuit is still symmetric → the voltage at node P will be zero

↓

No current through R_{SS}

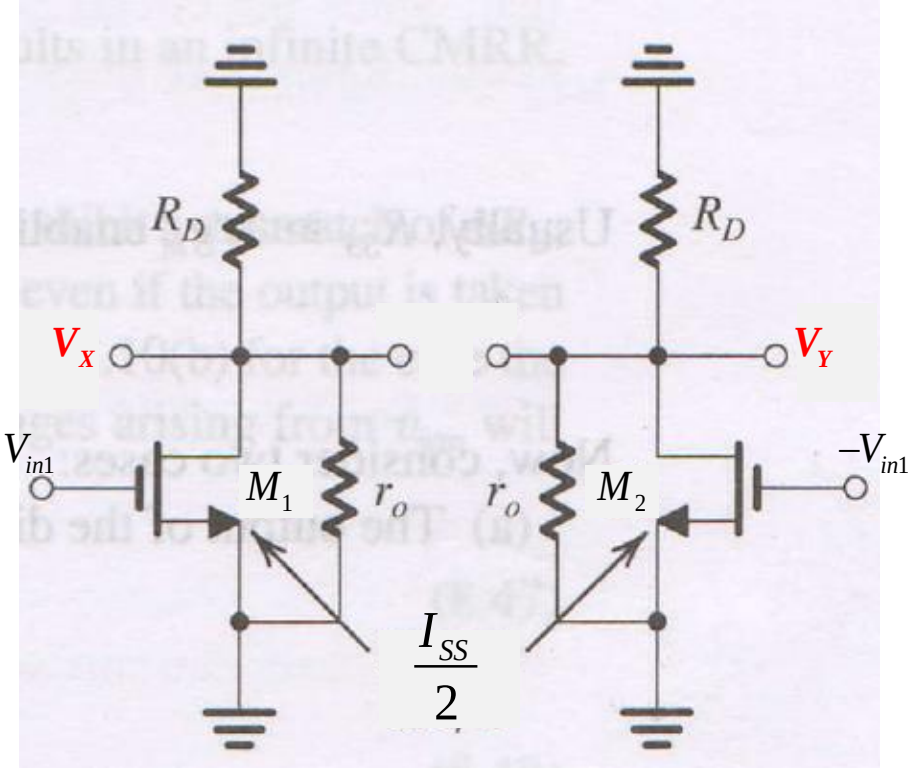
↓

R_{SS} plays no role in differential gain

Finite output resistance of current source

MOS Differential Pair – small signal analysis

- **The virtual ground on the source allows division of two identical CS amplifiers: → differential half circuits**



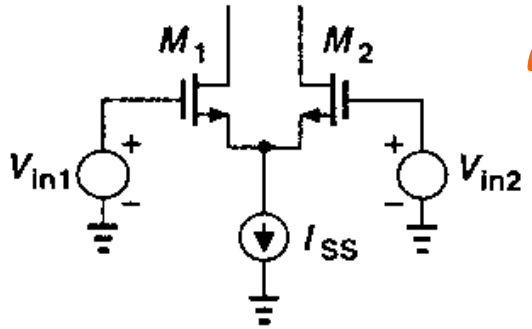
$$V_X = -g_m V_{in1}\left(R_D \| r_o\right)$$

$$V_Y = g_m V_{in1}\left(R_D \| r_o\right)$$

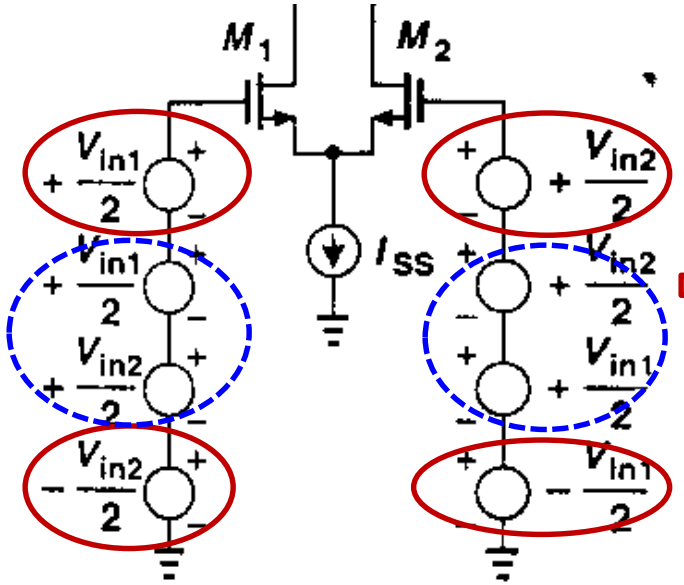
$$\Rightarrow V_X - V_Y = -g_m\left(2V_{in1}\right)\left(R_D \| r_o\right)$$

$$\therefore A_v = \frac{V_X - V_Y}{2V_{in1}} = -g_m\left(R_D \| r_o\right)$$

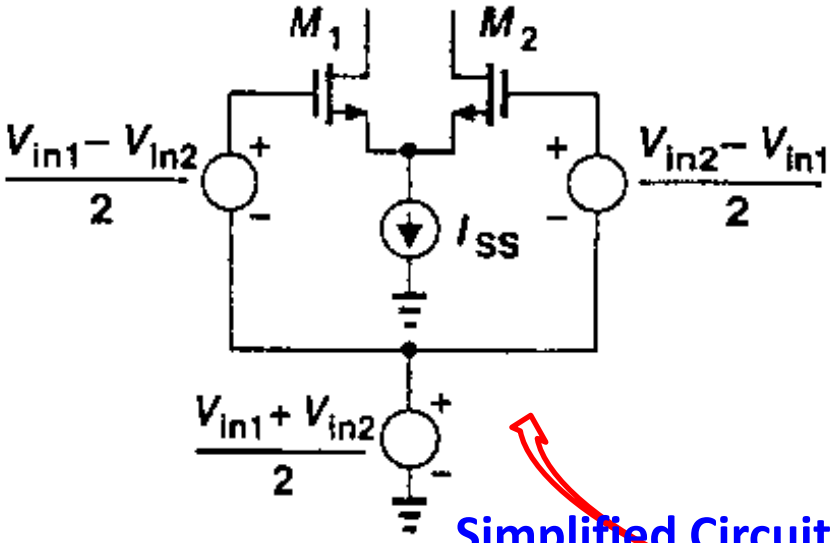
Small signal analysis – asymmetric inputs



Transform the inputs as

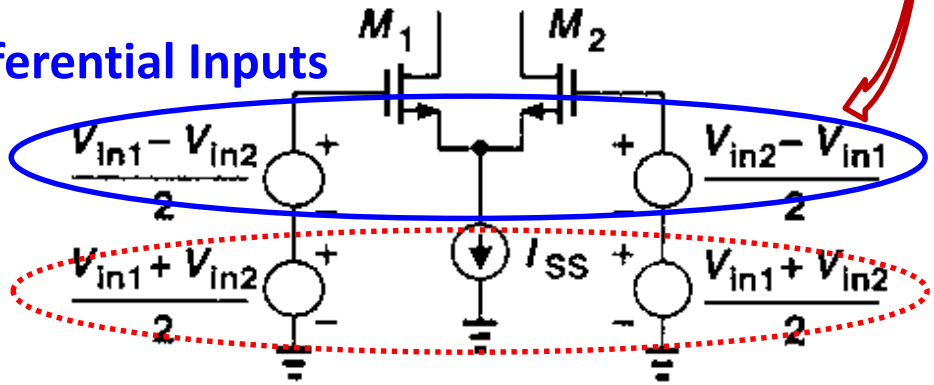


Simplify



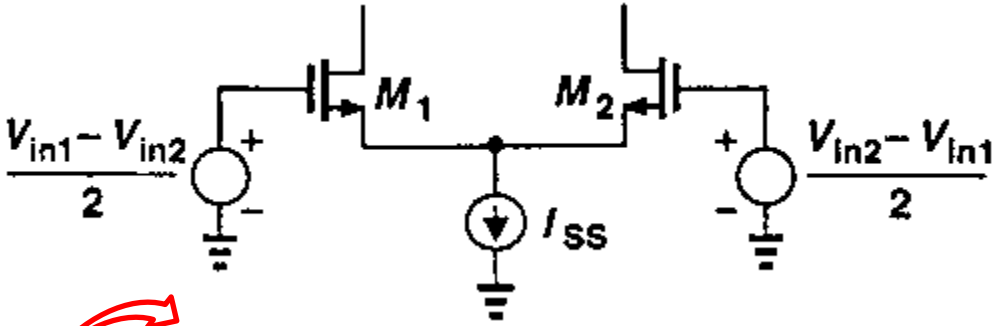
Simplified Circuit

Differential Inputs



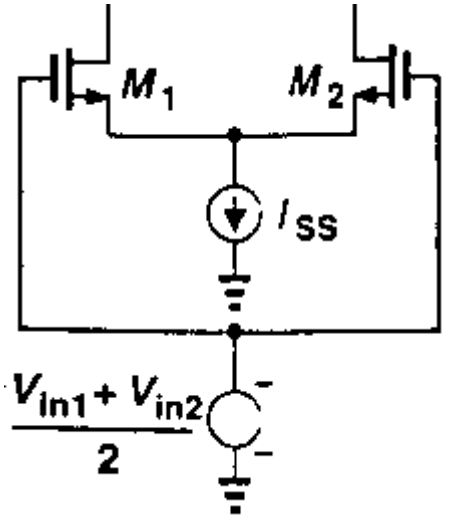
Common Mode Inputs

Small signal analysis – asymmetric inputs



Circuit for Differential Mode

$$V_X - V_Y = -g_m\left(R_D \parallel r_o\right)\left(V_{in1} - V_{in2}\right)$$



Circuit for Common Mode

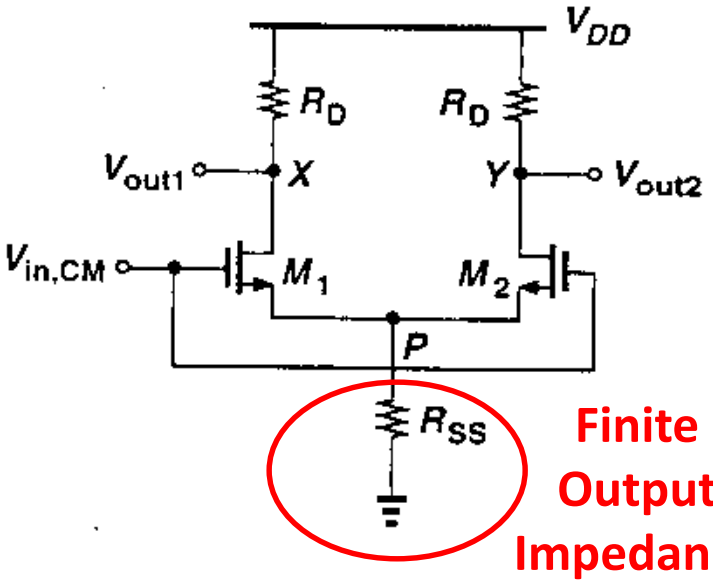
If the circuit is fully symmetric and I_{SS} is ideal current source, then M_1 and M_2 draws half of I_{SS} and is independent of $V_{in,CM}$. The V_X and V_Y experience no change as $V_{in,CM}$ varies. In essence, the circuit simply amplifies the difference between V_{in1} and V_{in2} while eliminating the effect of $V_{in,CM}$.

MOS Differential Pair – Common Mode Response

Quantitative Analysis

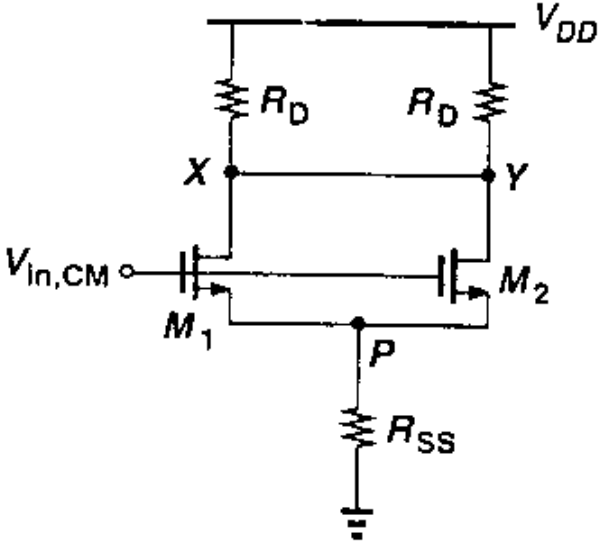
- In ideal condition, differential pair has the ability to suppress variations in the common-mode voltage
- However, in practical scenarios there is always some CM output

Case-I: differential pair is symmetric but the current source has finite output impedance.



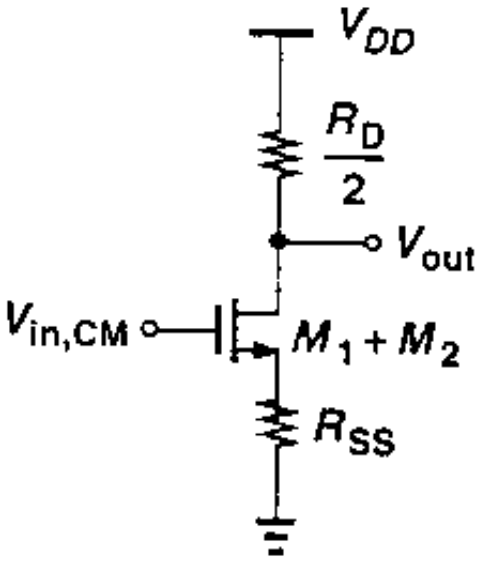
Finite Output Impedance

Symmetry allows shorting of node X and Y as $V_X = V_Y$



MOS Differential Pair – Common Mode Response (contd.)

- Shorting of X and Y brings M_1 and M_2 in parallel → they share all of their respective terminals



The CM gain is then:

$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = -\frac{R_D / 2}{1/(2g_m) + R_{SS}}$$

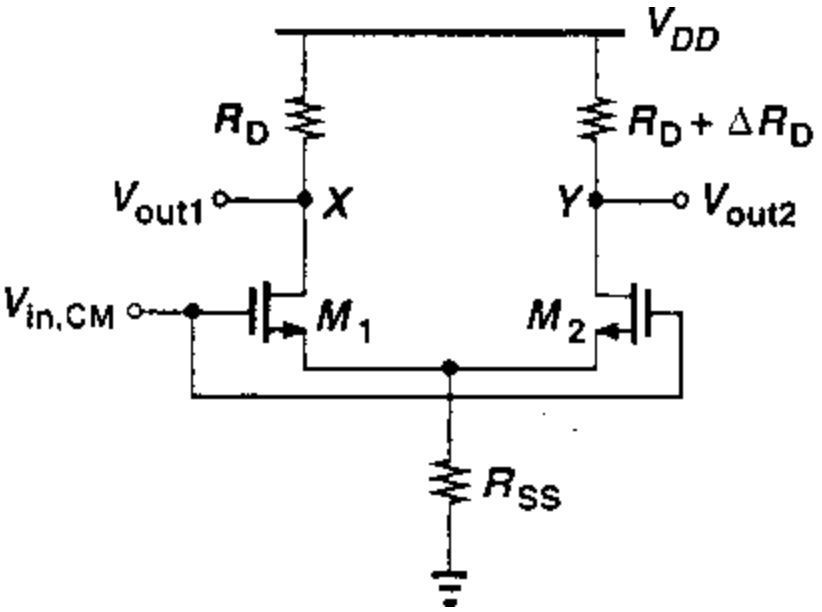
This shows that in a symmetric differential pair, input CM variations disturb the bias points altering the gain

Thus the finite output impedance of the tail current source results in some common-mode gain in a symmetric differential pair

In addition, input CM variations also limit the output voltage swings

MOS Differential Pair – Common Mode Response (contd.)

Case-II: Effect of input common-mode variation when there is mismatch in R_D and the differential pair suffers from finite output impedance of current source.



- What happens to V_X and V_Y as $V_{in,CM}$ increases?
- Since M_1 and M_2 are symmetric → I_{D1} and I_{D2} increases by same amount:

$$\Delta I_D = \frac{g_m}{1+2g_m R_{SS}} \Delta V_{in,CM}$$

- The respective change in V_X and V_Y are given by:

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} R_D$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1+2g_m R_{SS}} \left(R_D + \Delta R_D\right)$$

MOS Differential Pair – Common Mode Response (contd.)

- Therefore the differential output due to mis-matched R_D is:

$$\Rightarrow \Delta V_X - \Delta V_Y = -\Delta V_{in,CM}\left[\frac{g_m}{1+2g_mR_{SS}}R_D - \frac{g_m}{1+2g_mR_{SS}}R_D - \frac{g_m}{1+2g_mR_{SS}}\Delta R_D\right]$$

$$\therefore \Delta V_X - \Delta V_Y = \left(\frac{g_m}{1+2g_mR_{SS}}\Delta R_D\right)\Delta V_{in,CM}$$

- It is apparent that a small common-mode input can generate a differential mode output → usually denoted by a metric called $A_{CM\text{-}DM}$

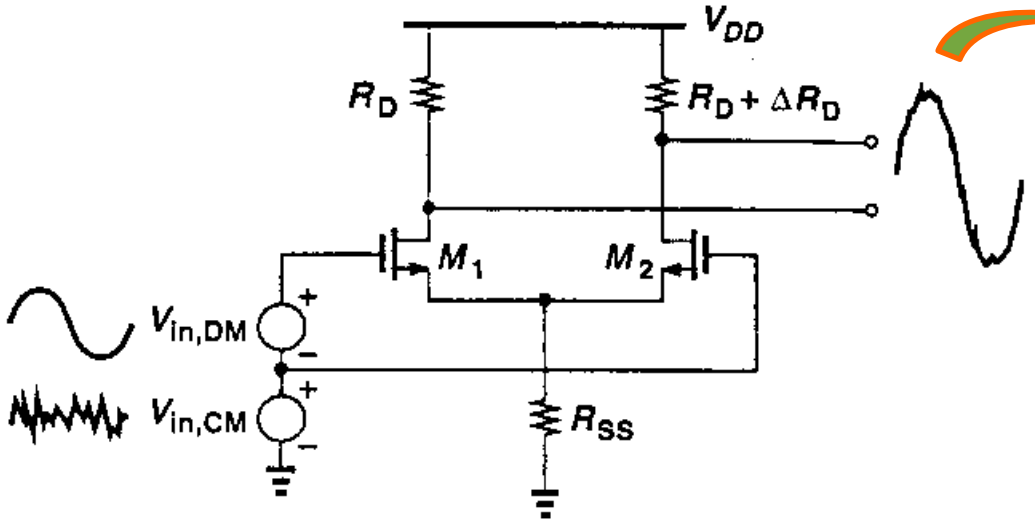
$$A_{CM-DM} = \frac{\Delta V_X - \Delta V_Y}{\Delta V_{in,CM}} = \frac{g_m}{1+2g_mR_{SS}}\Delta R_D$$

MOS Differential Pair – Common Mode Response (contd.)

Thus a common-mode input introduces a differential component, when the load is mis-matched, at the output

circuit exhibits common-mode to differential conversion

if the input of a differential pair includes both a differential signal and common-mode noise, the output is corrupted version of the input

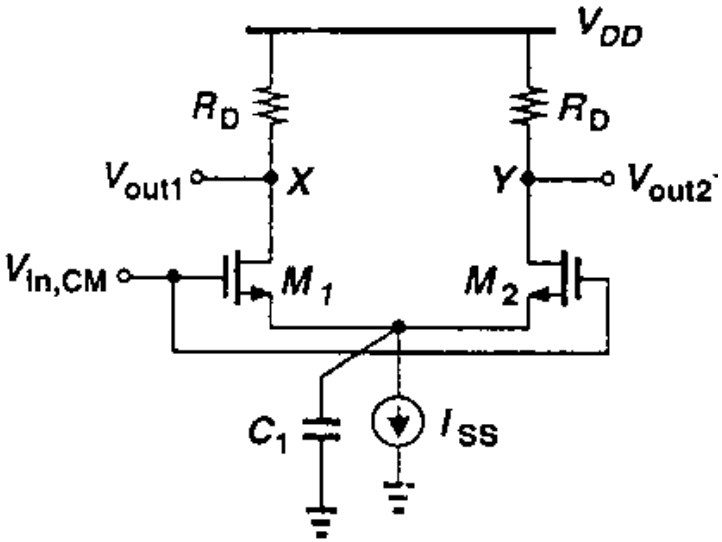


Big concern for Analog Circuits

Common-Mode Response (contd.)

Impact of common-mode to differential conversion

- With the increase in frequency of operation, the total capacitance (arising from the parasitics of the current source and the source-bulk junctions of M_1 and M_2) shunting the tail current source introduces larger tail current variations → **This large variation causes substantial common-mode to differential conversion even for very high output impedance of current source**



Furthermore, The asymmetry due to load impedance mismatch (and hence the resulting common-mode to differential conversion) corrupts the amplified differential output

Common-Mode Response (contd.)

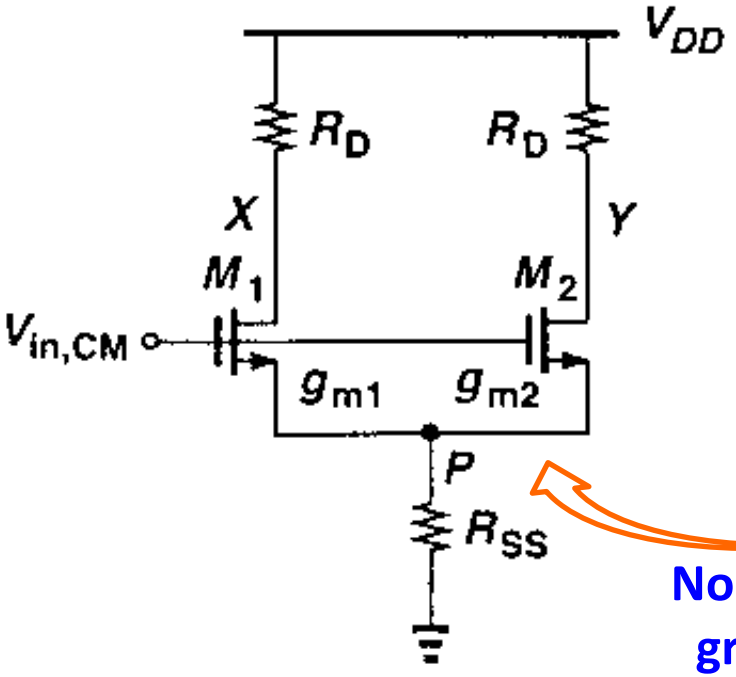
Impact of common-mode to differential conversion

- Summary: the common mode response of differential pairs depend on the output impedance of the tail current and the asymmetries in the circuit → manifestation of two effects
  - Variation of the output CM level (in the absence of mismatches)
  - Shifting of input common-mode variations to higher level at the output
- How about presence of mismatches?
  - Mismatches in R_D and mismatches in transistors (i.e, mismatches in transconductance)
  - The impact of transconductance mismatch on common-mode to differential conversion is more significant

Common-Mode Response (contd.)

Case-III: Effect of mismatches between M_1 and M_2 (V_T mismatches)

The asymmetry due to mismatch in the transistors generates slightly different currents in the two paths → leads to unequal transconductance



$$I_{D1} = g_{m1}\left(V_{in,CM} - V_P\right)$$

$$I_{D2} = g_{m2}\left(V_{in,CM} - V_P\right)$$

$$V_P = \left(I_{D1} + I_{D2}\right)R_{SS}$$

No more AC grounded

$$\Rightarrow V_P = \frac{\left(g_{m1} + g_{m2}\right)R_{SS}}{\left(g_{m1} + g_{m2}\right)R_{SS} + 1}V_{in,CM}$$

Common-Mode Response (contd.)

$$V_X = V_{DD} - I_{D1}R_D = V_{DD} - g_{m1}\left(V_{in,CM} - V_P\right)R_D$$

$$\Rightarrow V_X = V_{DD} - \frac{g_{m1}}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}R_D V_{in,CM}$$

$$\Rightarrow V_Y = V_{DD} - \frac{g_{m2}}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}R_D V_{in,CM}$$

$$\therefore V_X - V_Y = -\frac{g_{m1}-g_{m2}}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}R_D V_{in,CM}$$

- **The mismatch in the transistors convert the input CM variations to a differential error by a factor:**

$$A_{CM-DM} = \frac{V_X - V_Y}{V_{in,CM}} = -\frac{\Delta g_m R_D}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}$$

Unwanted

Common-Mode Response (contd.)

- Ideally, this unwanted $A_{CM\text{-}DM}$ is normalized to the wanted A_{DM} → the normalization factor is called CMRR

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

- For a differential pair with mis-matched transistor but operating at equilibrium, the differential gain is given by:

$$\left| A_{DM} \right| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{1 + \left(g_{m1} + g_{m2} \right) R_{SS}}$$

$$\Rightarrow CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| = \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} R_{SS}}{2 \Delta g_m} = \frac{g_m}{\Delta g_m} \left(1 + 2 g_m R_{SS} \right)$$

- Where, $g_m = (g_{m1} + g_{m2}) / 2$

Example – 1

- **In the following circuit,** $(W/L)_{1,2} = 50/0.5$, $(W/L)_{3,4} = 10/0.5$ and $I_{SS} = 0.5mA$. Also, I_{SS} is implemented with an NMOS having $(W/L)_{SS} = 50/0.5$ **while VDD =3V.**
  - **What are the minimum and maximum allowable input CM levels if the differential swings at the input and output are small.**

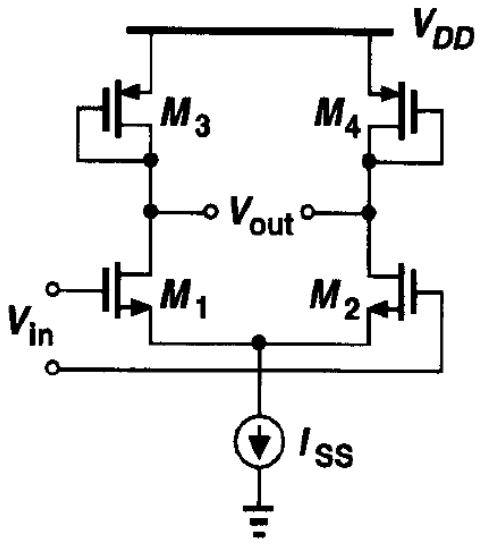


Table 2.1 Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

Example – 1 (contd.)

$$\left(\frac{W}{L}\right)_{SS} = \frac{50}{0.5} \qquad I_{SS} = 05mA \qquad \Rightarrow \qquad (V_{OV})_{SS} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{SS}}} = 0.273V$$

$$I_{D1} = \frac{I_{SS}}{2} = 0.25mA \qquad \Rightarrow \qquad (V_{OV})_1 = 0.193V$$

$$\left(V_{in,CM}\right)_{\min} = V_{GS1} + (V_{OV})_{SS} = 0.7 + 0.193 + 0.273 = 1.17V$$

$$\Rightarrow \qquad \left(V_{in,CM}\right)_{\max} = V_{DD} - |V_{GS3}| + V_{TN} \qquad |V_{GS3}| = |V_{TP}| + \sqrt{\frac{2I_{D3}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3}} = 1.61V$$

$$\therefore \left(V_{in,CM}\right)_{\max} = 3 - 1.61 + 0.7 = 2.09V$$

Example – 2

- **In the following circuit,** $(W/L)_{1,2} = 50/0.5$ and $R_D = 2k\Omega$. Suppose R_{SS} represents the output impedance on an NMOS current source with $(W/L)_{SS} = 50/0.5$ and a drain current of 1mA. The input signal consists of $V_{in,DM} = 1.5V + V_n(t)$, where $V_n(t)$ denotes noise with a peak-to-peak amplitude of 100mV. Assume $\Delta R/R = 0.5\%$.
  - **Calculate CMRR**