Lecture-13 Date: 05.10.2015

- Differential Amplifier (contd.)

Differential Pair (contd.)

Alternative Approach:

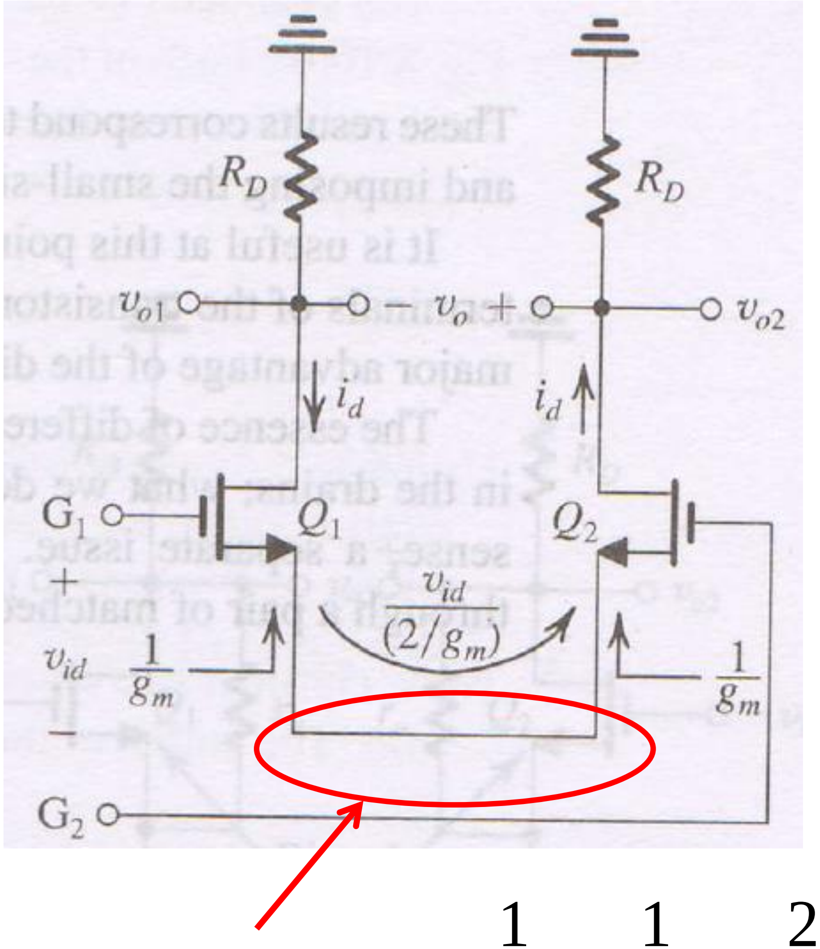
Drain current is given by:

$$i_{d1} = i_{d2} = \frac{v_{id}}{2/g_m}$$

Therefore,

$$v_{o1} = -g_m \frac{v_{id}}{2} R_D \qquad v_{o2} = g_m \frac{v_{id}}{2} R_D$$

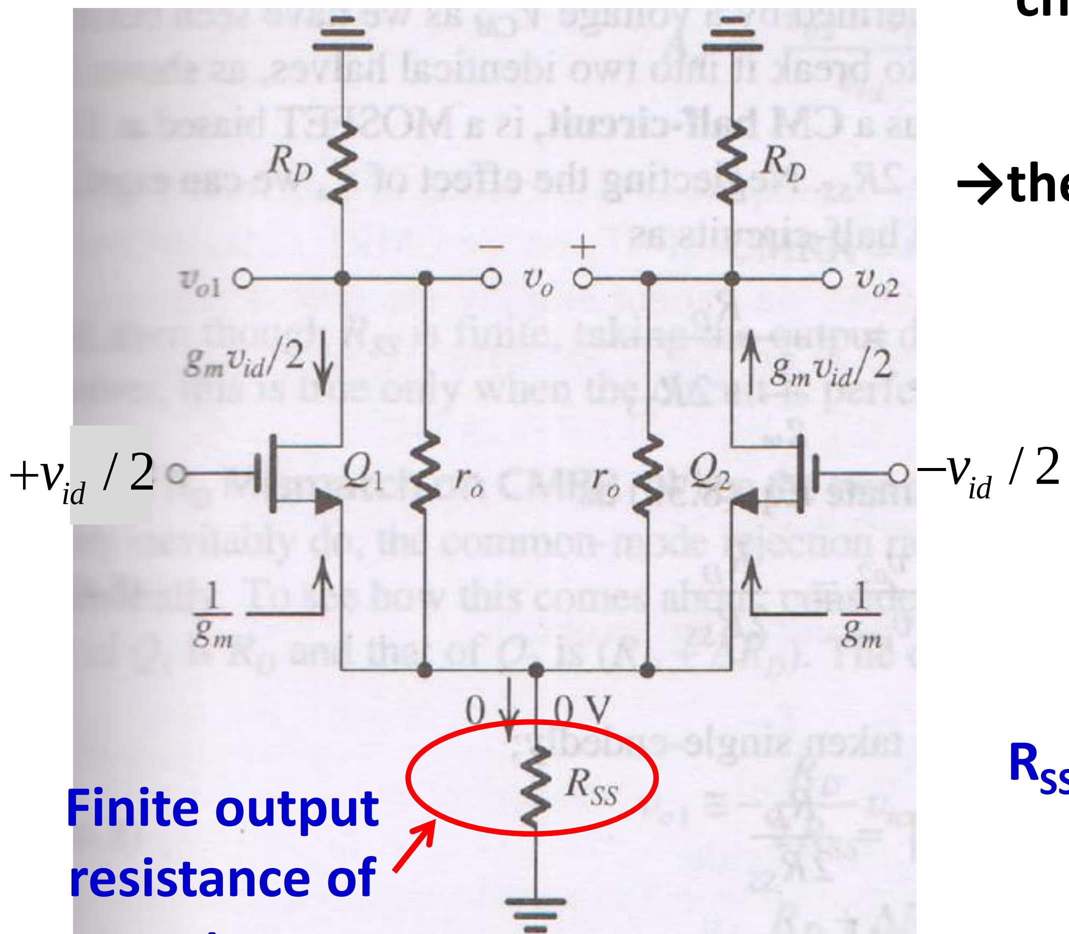
$$\therefore A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$



Total Impedance= $\frac{1}{g_m} + \frac{1}{g_m} = \frac{2}{g_m}$

Differential Pair – Small-Signal Operation (contd.)

- **Effect of r_0 on the gain**



Finite output resistance of current source

How will the gain be affected if channel length modulation is considered?

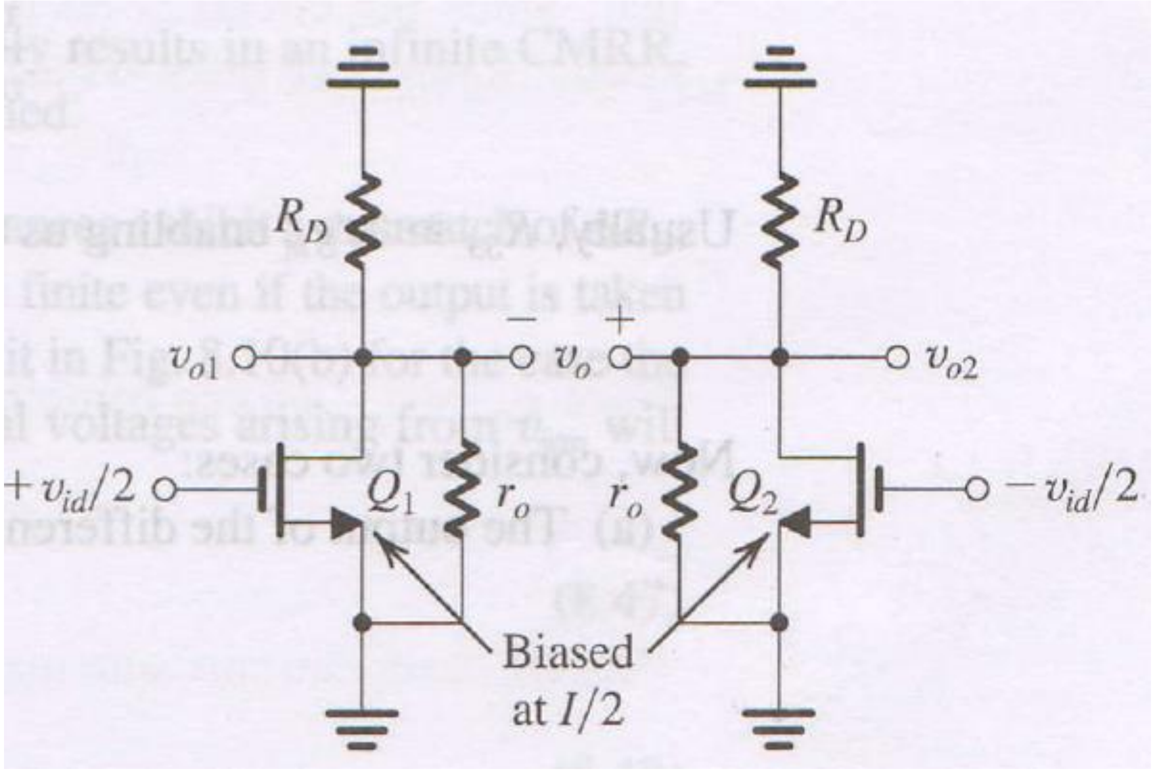
→the circuit is still symmetric → the voltage at common source connection will be zero

NO current through R_{SS}

R_{SS} plays no role in differential gain

Differential Pair – Small-Signal Operation (contd.)

- **The virtual ground on the source allows division of two identical CS amplifiers: →differential half circuits**



$$v_{o1} = -g_m \frac{v_{id}}{2}\left(R_D \,||\, r_o\right)$$

$$v_{o2} = g_m \frac{v_{id}}{2}\left(R_D \,||\, r_o\right)$$

$$\Rightarrow v_o = g_m v_{id}\left(R_D \,||\, r_o\right)$$

$$\therefore A_d = \frac{v_o}{v_{id}} = g_m\left(R_D \,||\, r_o\right)$$

Differential Pair – Small-Signal Operation (contd.)

Question: A MOS differential amplifier is operated at a total bias current of 0.8 mA, using transistors with a W/L ratio of 100, $\mu_n C_{ox}$=0.2mA/V^2, V_A = 20 V, and R_D = 5kΩ. Find V_{OV}, g_m, r_o, and A_d.

$$\frac{I}{2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{OV}^2 \qquad \Rightarrow V_{OV} = 0.2V$$

$$r_o = \frac{V_A}{I_D} = \frac{V_A}{(I/2)} = \frac{20V}{0.4*10^{-3}} = 50k\Omega$$

$$g_m = \frac{2I_D}{V_{OV}}$$

$$\Rightarrow g_m = \frac{I}{V_{OV}} = \frac{0.8*10^{-3}}{0.2}A/V$$

$$\therefore g_m = 4mA/V$$

$$A_d = g_m\left(R_D \,||\, r_o\right) = \left(4mA/V\right)*\left(5k\Omega \,||\, 50k\Omega\right) = 18.18$$

$$\left(A_d\right)_{no\_r_o} = g_m\left(R_D \,||\, r_o\right) = \left(4mA/V\right)*5k\Omega = 20$$

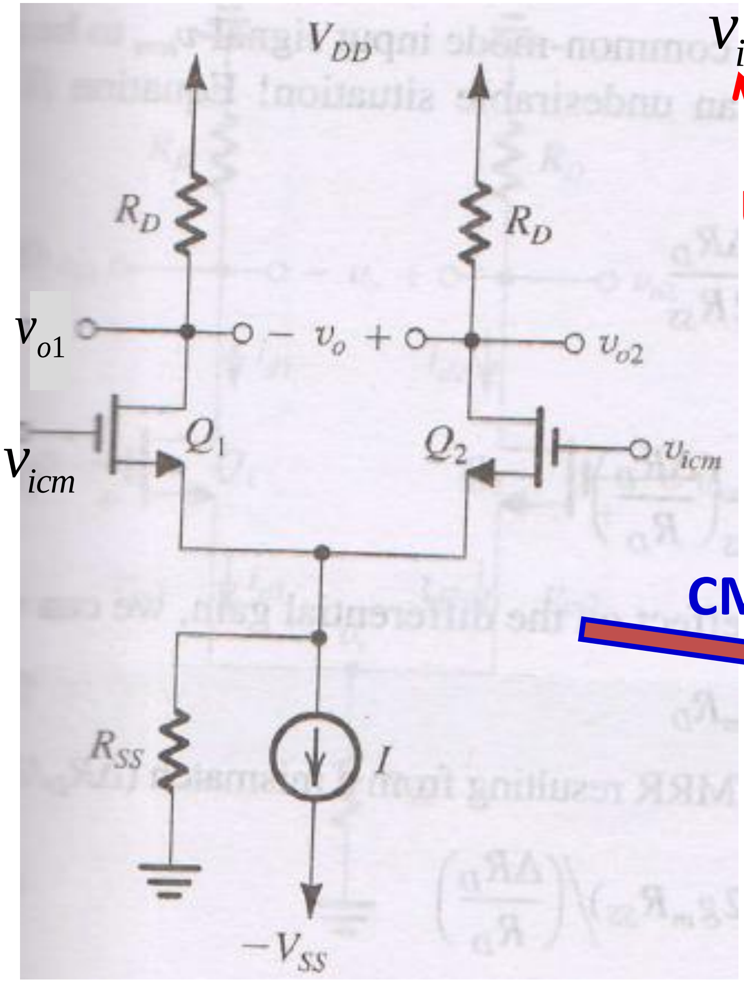
Common-Mode Gain and CMRR

- The objective of differential amplifier is to amplify only the difference between two different potentials regardless of the common-mode value.
- CMRR is the ratio of the magnitude of the differential gain to the common-mode gain.
- The input common mode range (ICMR) specifies over what range of common-mode voltages the differential amplifier continues to sense and amplify the difference signal with the same gain.
- In CMOS differential amplifier, the most serious problem is of offset voltage.
- In theory, the output offset voltage should be zero.
- However, in practical differential amplifier, there is always some output offset voltage due to several constraints.

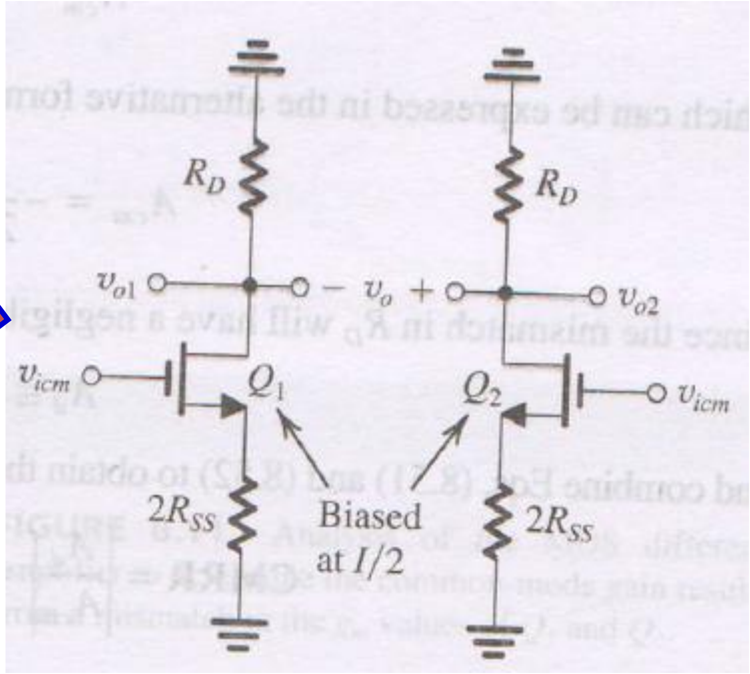
Common-Mode Gain and CMRR (contd.)

V_{icm} : represents a disturbance or interference signal coupled to both the inputs

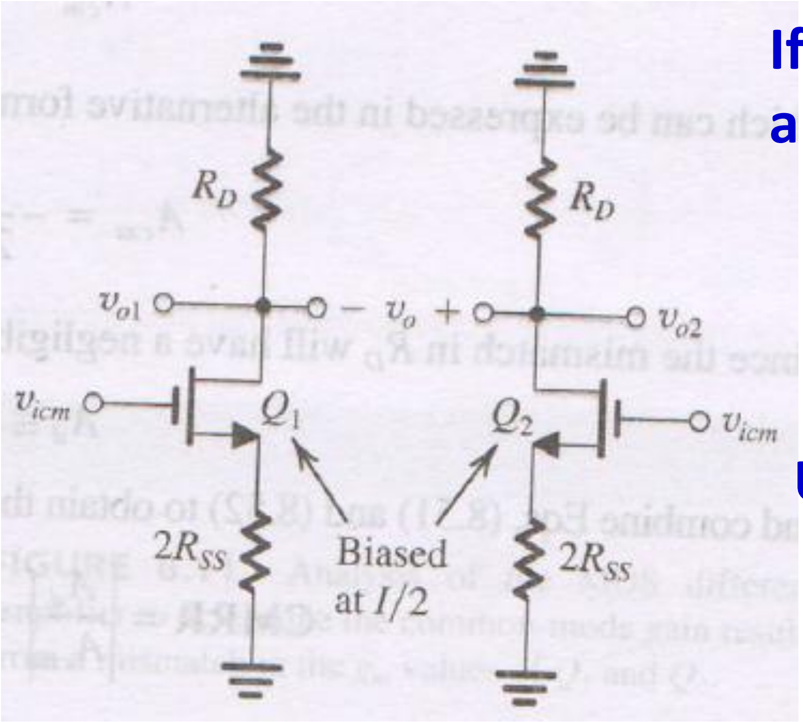
Unrelated to common mode dc level V_{CM}



CM Half-Circuit



Common-Mode Gain and CMRR (contd.)



If r_o is ignored then single ended gains are given by:

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{\frac{1}{g_m} + 2R_{SS}}$$

Usually, $R_{SS} >> 1/g_m$

$$\Rightarrow \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} = -\frac{R_D}{2R_{SS}}$$

If the output is taken single-endedly then: $|A_{cm}| = \frac{R_D}{2R_{SS}}$ and $|A_d| = \frac{1}{2} g_m R_D$

$$\Rightarrow \left|\frac{A_d}{A_{cm}}\right| = g_m R_{SS}$$

Common-Mode Rejection Ratio (CMRR)

Common-Mode Gain and CMRR (contd.)

If the output is taken differentially then: $\left|A_{cm}\right| = \dfrac{v_{o2} - v_{o1}}{v_{icm}} = 0$

and $\left|A_d\right| = \dfrac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$

$$\Rightarrow CMRR = \left|\frac{A_d}{A_{cm}}\right| = \infty$$

CMRR is infinite even for finite R_{SS} → for matched and balanced differential pair

- **Effect of R_D mismatch: suppose the mismatch is to the tune of ΔR_D**

$$v_{o1} = -\frac{R_D}{2R_{SS}} v_{icm} \qquad v_{o2} = -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

Common-Mode Gain and CMRR (contd.)

$$\Rightarrow v_{o2} - v_{o1} = -\frac{\Delta R_D}{2R_{SS}} v_{icm} \qquad \therefore A_{cm} = \frac{v_{o2} - v_{o1}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}}$$

- **The mismatch in R_D will have negligible effect on the differential gain:**

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} \cong -g_m R_D$$

$$\therefore CMRR = \left| \frac{A_d}{A_{cm}} \right| = \frac{g_m R_D}{\left(\Delta R_D / 2R_{SS} \right)}$$

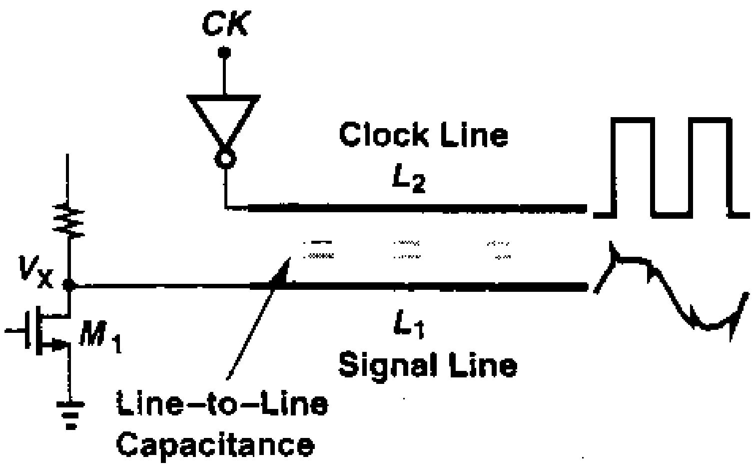
Some finite value → unwanted!

Similarly, mismatch in g_m also affects CMRR

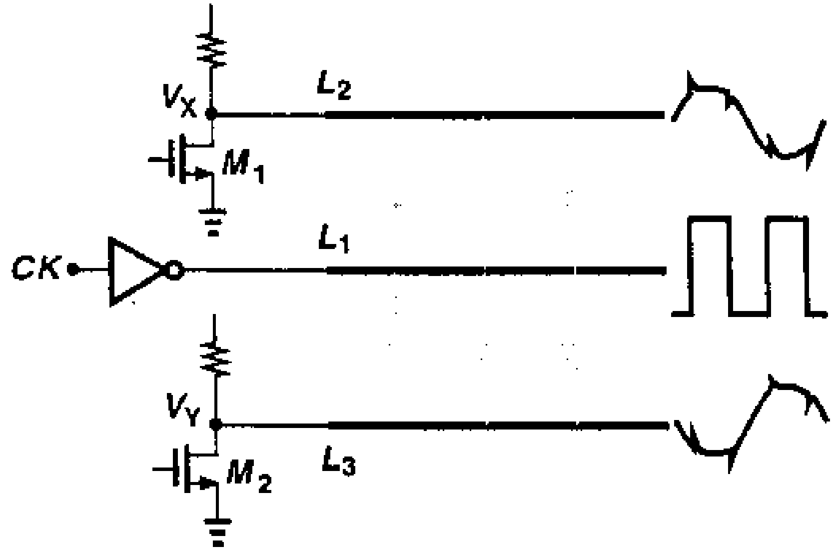
Revisit

Advantages of Differential Signaling

1. Immunity to Environmental Noise



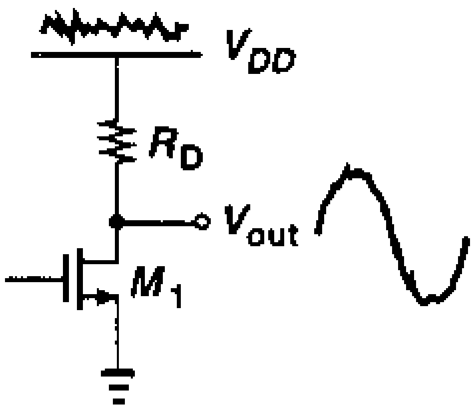
- Line L_1 carries a small and sensitive signal
- Line L_2 carries a large clock waveform
- Due to capacitive coupling between the lines, the transitions on line L_2 corrupt signal on line L_1

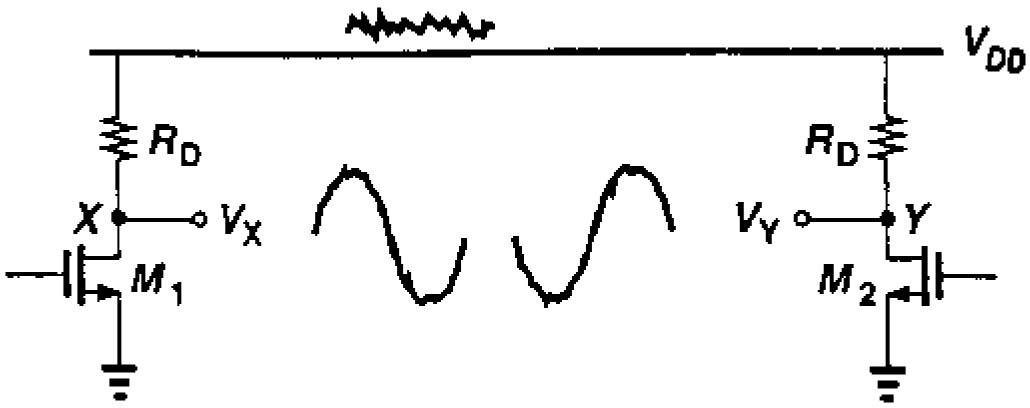


- The small and sensitive signal is distributed as two equal and opposite phases
- The clock signal is placed between the two
- The transition disturb the differential phases by equal amounts, leaving the difference intact

Advantages of Differential Signaling

2. Immunity to Supply Noise





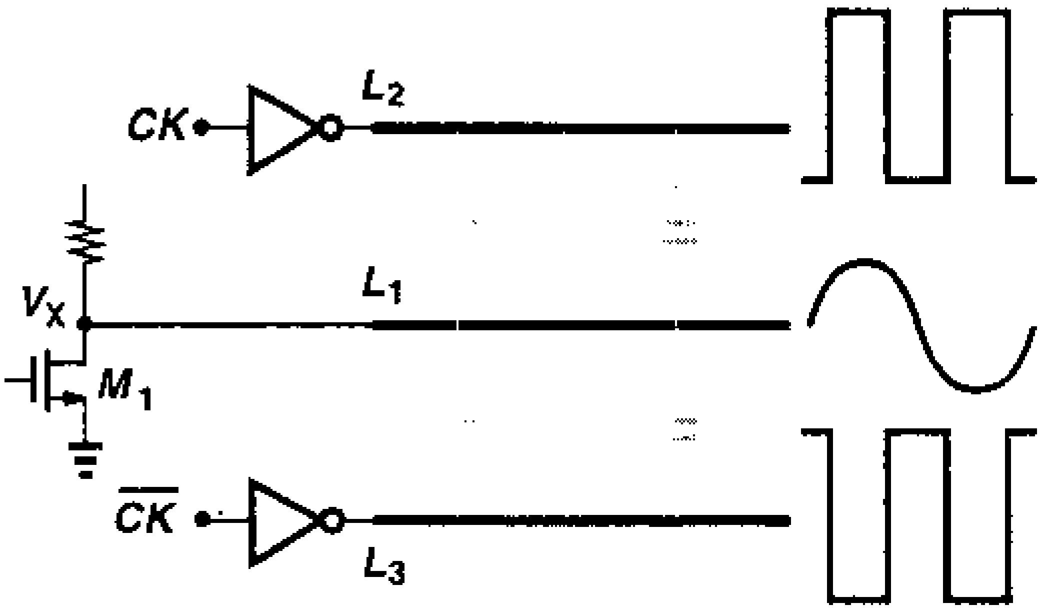
- If V_{DD} changes by ΔV, V_{out} changes by the same amount.

- Noise in V_{DD} affects V_X and V_Y, but not $V_X - V_Y$

Advantages of Differential Signaling

3. Reduction of Coupled Noise

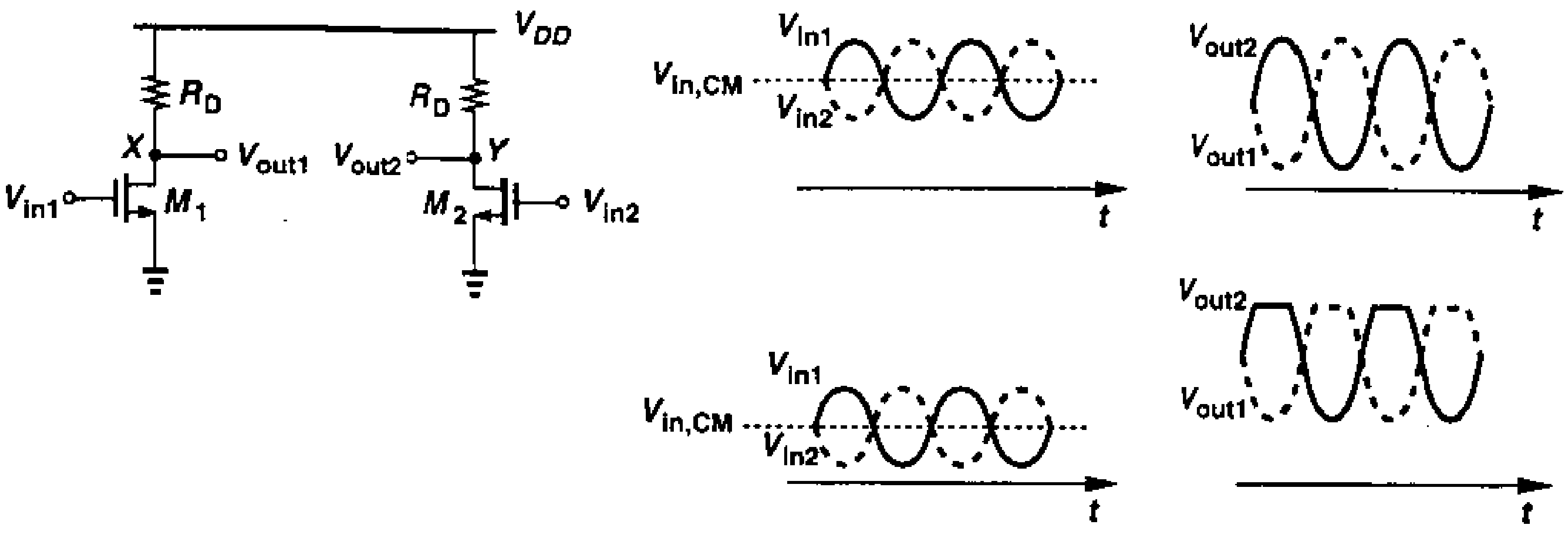
- Differential signaling can also be employed in noisy lines → for example, distributed clock can help in removing noise from signals



Noise coupled from L_3 to L_1 and L_2 to L_1 cancel each other.

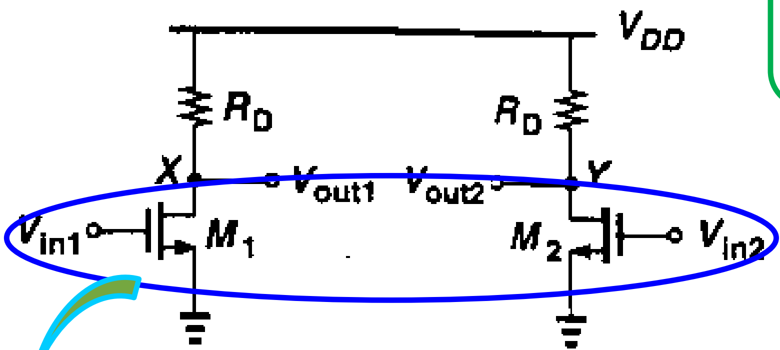
Issues with Differential Signaling

- <u>Sensitivity to the Common Mode Level</u>



- Excessive low $V_{in,CM}$ turns off Devices → leads to clipping at the output
- Solution?

MOS Differential Pair



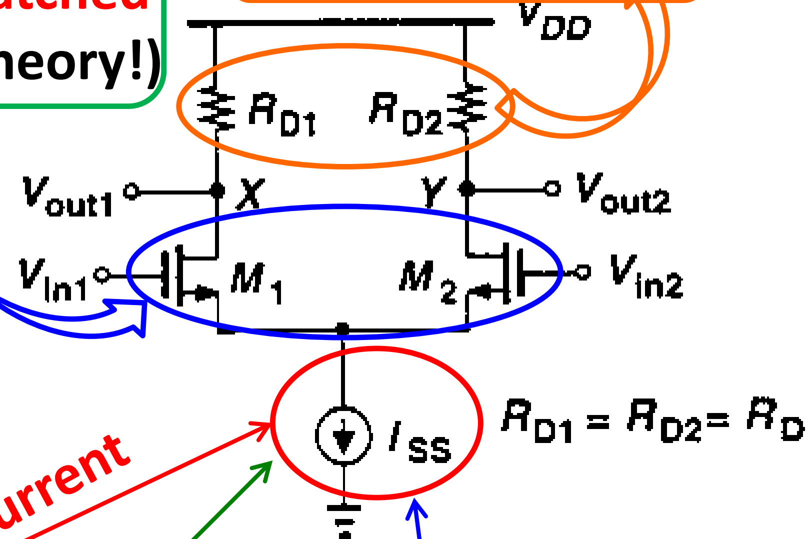
Variation of input CM level regulates the bias currents of M_1 and M_2
→ Undesired!!!

Solution??

Tail Current

M_1 and M_2 are perfectly matched (at least in theory!)

ensures M_1 and M_2 in saturation



$R_{D1} = R_{D2} = R_D$

Current source is ideal: constant current, infinite output impedance

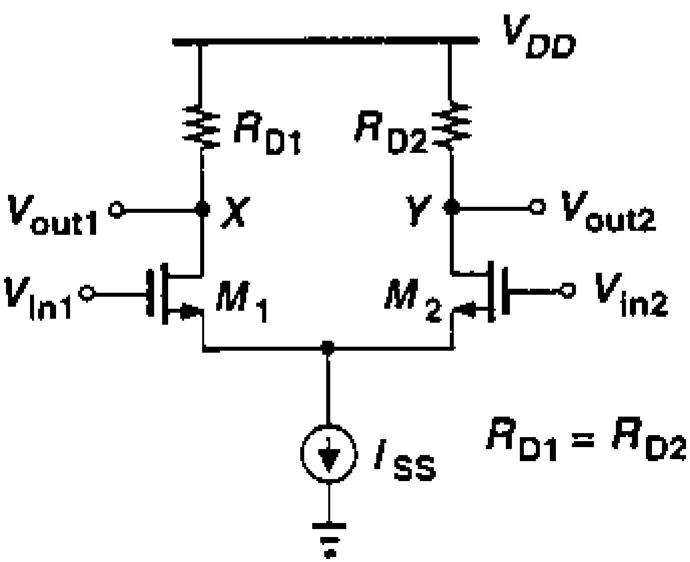
Need?

To overcome the issues emanating from non-ideal CM level

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from $-\infty$ to ∞

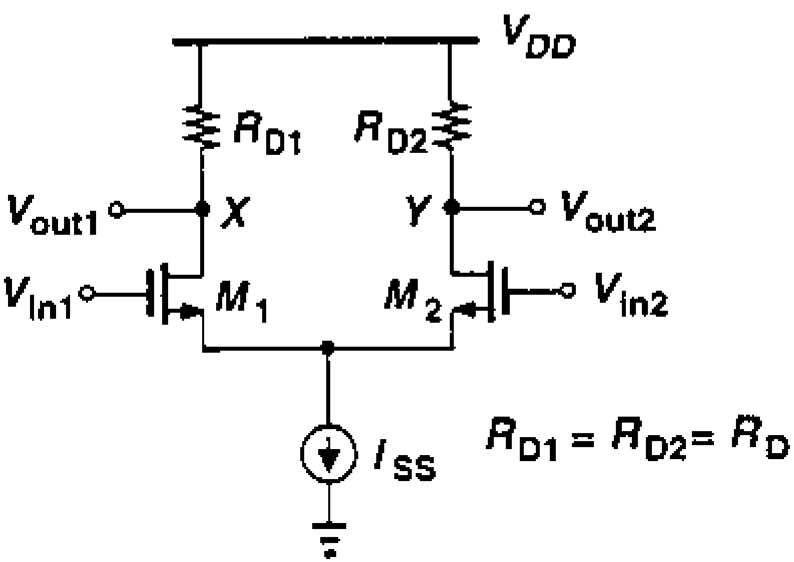


- V_{in1} is much more –ve than V_{in2} then:
  - M_1 if OFF and M_2 is ON
  - $I_{D2} = I_{SS}$
  - $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - I_{SS}R_D$
- V_{in1} is brought closer to V_{in2} then:
  - M_1 gradually turns ON and M_2 is ON
    - Draws a fraction of I_{SS} and lowers V_{out1}
  - I_{D2} decreases and V_{out2} rises
- $V_{in1} = V_{in2}$
  - $V_{out1} = V_{out2} = V_{DD} - I_{SS}R_D/2$

MOS Differential Pair

Qualitative Analysis – differential input

- Let us check the effect of $V_{in1} - V_{in2}$ variation from -∞ to ∞

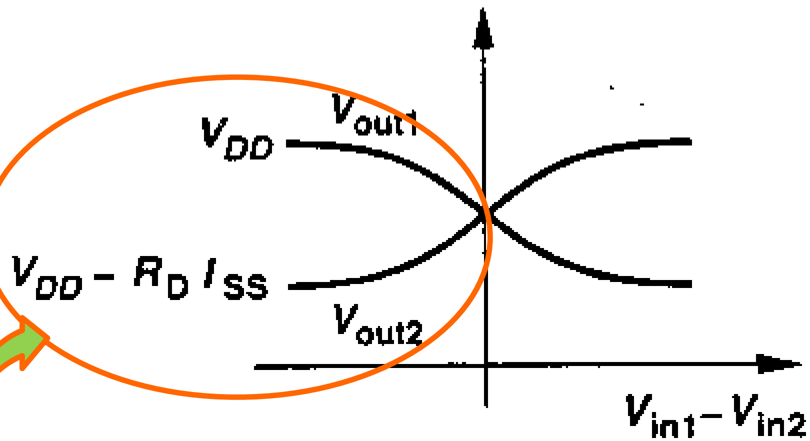


- V_{in1} becomes more +ve than V_{in2} then:
  - M_1 if ON and M_2 is ON
  - M_1 carries greater I_{SS} than M_2
- For sufficiently large $V_{in1} - V_{in2}$:
  - All of the I_{SS} goes through M_1 → M_2 is OFF
  - $V_{out1} = V_{DD} - I_{SS}R_D$ and $V_{out2} = V_{DD}$

MOS Differential Pair

Qualitative Analysis – differential input

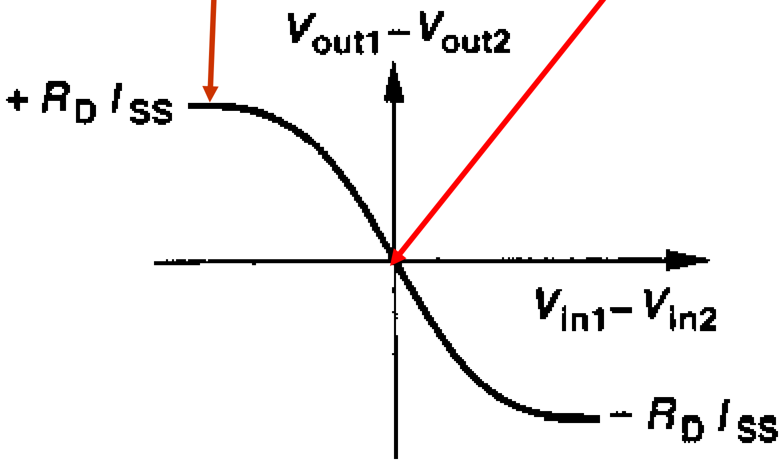
- Plotting $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$



The maximum and minimum levels at the output are well defined and is independent of input CM level ($V_{in,cm}$)

Minimum Slope ↔ Minimum Gain

Maximum Slope ↔Maximum Gain



The circuit becomes more nonlinear as the input voltage swing increases (i.e., $V_{in1} - V_{in2}$ increases) ↔ at $V_{in1} = V_{in2}$, the circuit is said to be in equilibrium

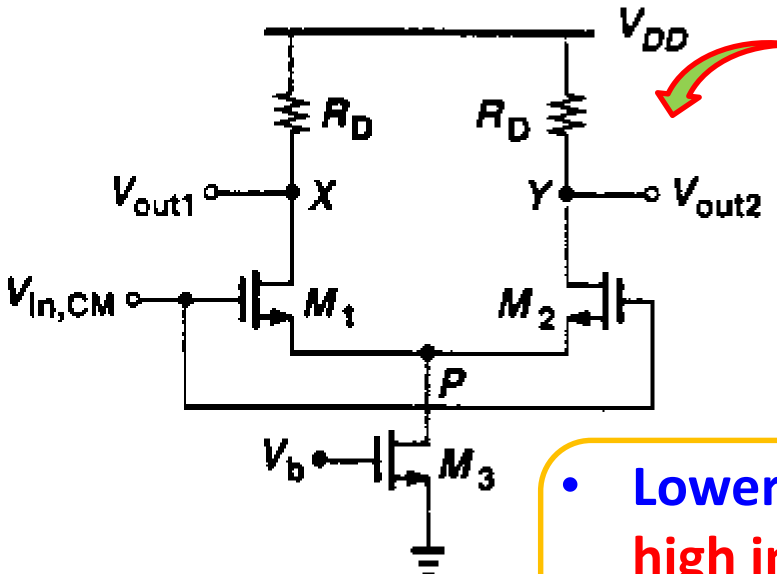
MOS Differential Pair

Qualitative Analysis – common mode input

- Now let us consider the common mode behavior of the circuit

As mentioned, the tail current source is used to suppress the effect of input CM level variation ($V_{in,cm}$)

Does this enable us to set any arbitrary level of input CM ($V_{in,cm}$)



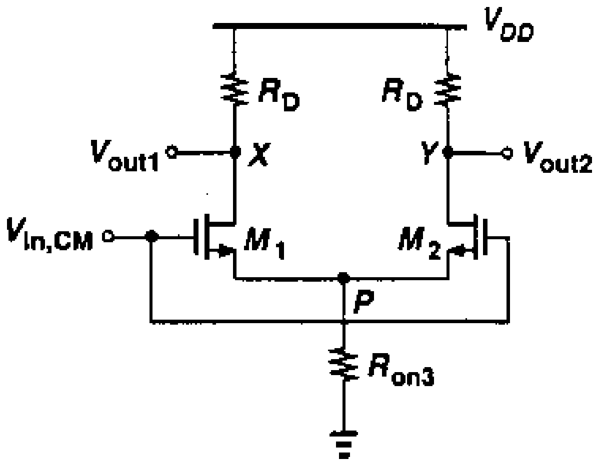
To understand this:

- Set $V_{in1} = V_{in2} = V_{in,CM}$
- Then vary $V_{in,CM}$ from 0 to V_{DD}
- Also implement I_{SS} with an NFET

- Lower bound of $V_{in,cm}$: V_P should be sufficiently high in order for M_3 to act as a current source.
- Upper bound of $V_{in,\ cm}$: M_1 and M_2 need to remain in saturation.

MOS Differential Pair

Qualitative Analysis – common mode input



- What happens when $V_{in,CM} = 0$?
  - M_1 and M_2 will be OFF and M_3 can be in triode for high enough V_b
  - $I_{D1} = I_{D2} = 0$ ← circuit is incapable of amplification

- Now suppose $V_{in,CM}$ becomes more +ve
  - M_1 and M_2 will turn ON if $V_{in,CM}$ exceeds V_T
  - I_{D1} and I_{D2} will continue to rise with the increase in $V_{in,CM}$
  - V_P will track $V_{in,CM}$ as M_1 and M_2 work like a source follower
  - For high enough $V_{in,CM}$, M_3 will be in saturation as well

$$V_{in,CM} \geq V_{GS1,2} + (V_{GS3} - V_{T3})$$

- If $V_{in,CM}$ rises further
  - M_1 and M_2 will remain in saturation if:

$$V_{in,CM} - V_T \leq V_{out1} \quad \Rightarrow \quad V_{in,CM} \leq V_{DD} - \frac{I_{SS}}{2} R_D + V_T$$

MOS Differential Pair

Qualitative Analysis – common mode input

- **Alternatively: the common-mode input range can be identified as:**
- **For M_1 and M_2 to remain in saturation:**

$$V_{GS1,2} - V_T \leq V_{DS1,2}$$

$$\Rightarrow V_{in,CM} - V_T \leq V_{DD} - \frac{I_{SS}}{2} R_D$$

$$\Rightarrow V_{in,CM} \leq V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

$$\therefore (V_{in,CM})_{\max} = V_T + V_{DD} - \frac{I_{SS}}{2} R_D$$

- **The lowest value of $V_{in,CM}$ is determined by the need to keep the constant current source operational:**

$$V_{in,CM} - V_{GS1,2} \geq V_{GS3} - V_T$$

$$\Rightarrow V_{in,CM} \geq V_{GS1,2} + (V_{GS3} - V_{T3})$$

$$V_{GS1,2} + (V_{GS3} - V_T) \leq V_{in,CM} \leq \min\left[V_{DD} - \frac{I_{SS}}{2} R_D + V_T, V_{DD} \right]$$

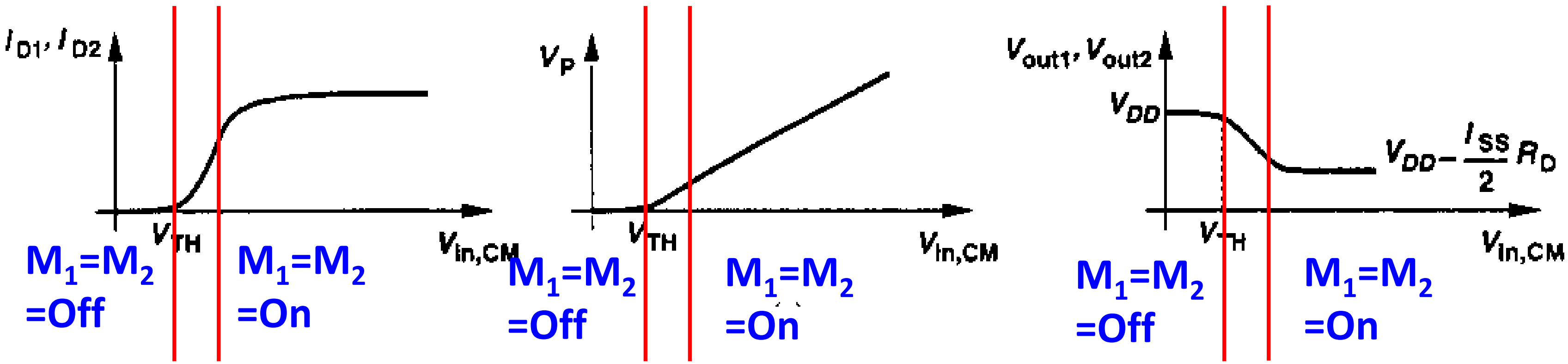
MOS Differential Pair

Qualitative Analysis – common mode input

- **Thus, $V_{in,CM}$ is bounded as:**

$$V_{GS1,2} + (V_{GS3} - V_T) \le V_{in,CM} \le \min\left[V_{DD} - \frac{I_{SS}}{2} R_D + V_T, V_{DD} \right]$$

- **Summary:**

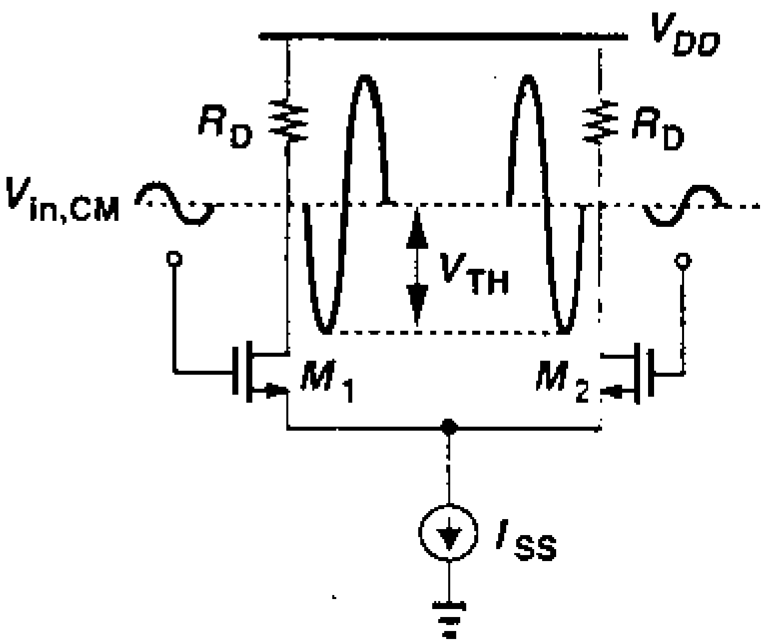


M_3=Linear M_3=Linear M_3=Linear

MOS Differential Pair

Qualitative Analysis – common mode input

- How large can the output voltage swings of a differential pair be?



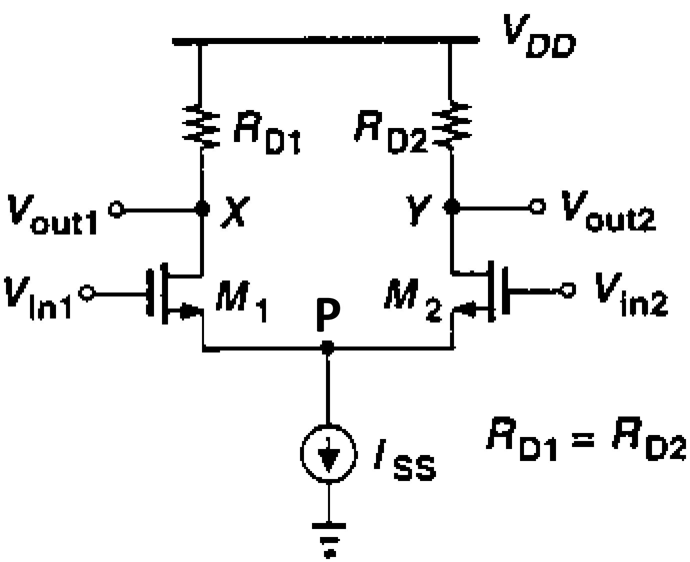
$$V_{out,\max} = V_{DD}$$

$$V_{out,\min} = V_{in,CM} - V_T$$

The higher the input CM level, the smaller the allowable output swings.

MOS Differential Pair

Quantitative Analysis – differential input



$R_{D1} = R_{D2} = R_D$

- For +ve V_{in1} → V_{GS1} is greater than V_{GS2} → I_{D1} will be greater than I_{D2}

$$V_{out2}(=V_{DD} - I_{D2}R_D) > V_{out1}(=V_{DD} - I_{D1}R_D)$$

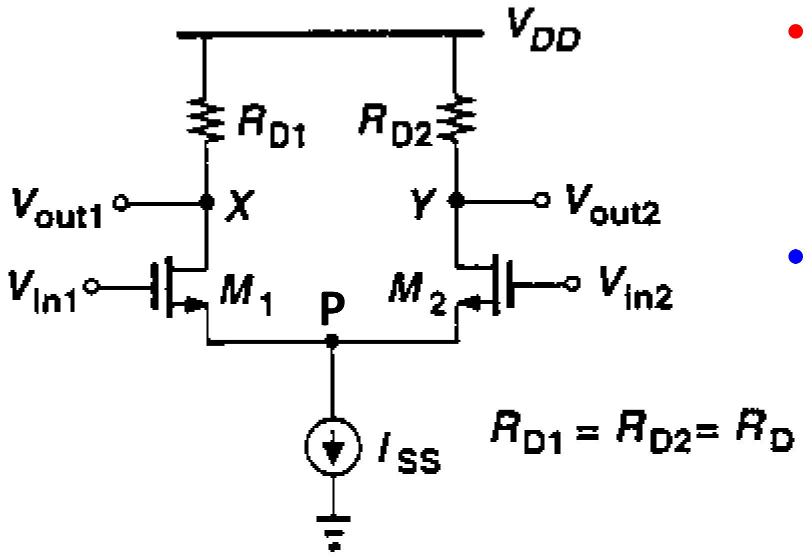
- For +ve V_{in2} → V_{GS2} is greater than V_{GS1} → I_{D2} will be greater than I_{D1}

$$V_{out1}(=V_{DD} - I_{D1}R_D) > V_{out2}(=V_{DD} - I_{D2}R_D)$$

It is thus apparent that the differential pair respond to differential-mode signals → by providing differential output signal between the two drains

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

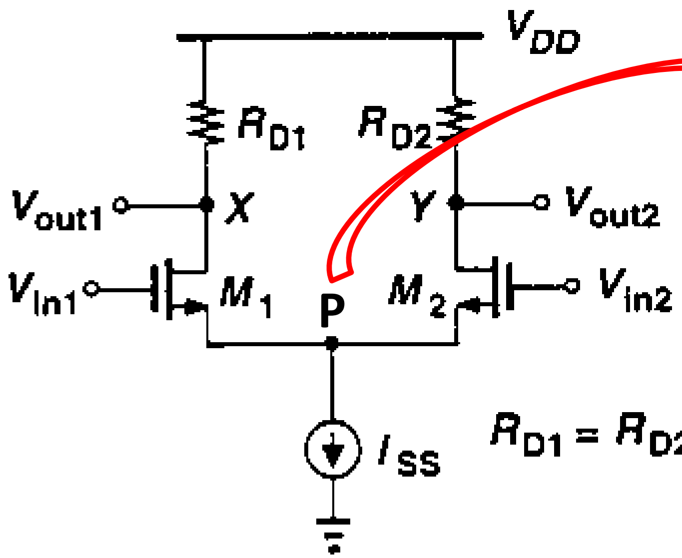


- The idea is to define I_{D1} and I_{D2} in terms of input differential signal $V_{in1} - V_{in2}$
- The circuit doesn't include connection details considering that these drain current equations do not depend on the external circuitries

Assumptions: M_1 and M_2 are always in saturation; differential pair is perfectly matched; channel length modulation is not present

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input



$$V_P = V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

$$\therefore V_{in1} - V_{in2} = V_{GS1} - V_{GS2}$$

We also know:

$R_{D1} = R_{D2} = R_D$

$$(V_{GS} - V_T)^2 = \frac{2I_D}{\mu_n C_{ox} \frac{W}{L}} \quad \Rightarrow V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} + V_T$$

Therefore:

$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox} \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu_n C_{ox} \frac{W}{L}}}$$

Squaring

$$(V_{in1} - V_{in2})^2 = \frac{2}{\mu_n C_{ox} \frac{W}{L}}\left(I_{D1} + I_{D2} - 2\sqrt{I_{D1} I_{D2}}\right)$$

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

$$(V_{in1}-V_{in2})^2=\frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{D1}+I_{D2}-2\sqrt{I_{D1}I_{D2}}\right)$$

$= I_{SS}$

$$\therefore (V_{in1}-V_{in2})^2=\frac{2}{\mu_n C_{ox}\frac{W}{L}}\left(I_{SS}-2\sqrt{I_{D1}I_{D2}}\right)$$

$$\frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)(V_{in1}-V_{in2})^2-I_{SS}=-2\sqrt{I_{D1}I_{D2}}$$

Squaring

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4+I_{SS}^2-I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2=4I_{D1}I_{D2}$$

$$\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2(V_{in1}-V_{in2})^4+I_{SS}^2-I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2=(I_{D1}+I_{D2})^2-(I_{D1}-I_{D2})^2$$

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

$$(I_{D1}-I_{D2})^2 = -\frac{1}{4}\left(\mu_n C_{ox}\frac{W}{L}\right)^2 (V_{in1}-V_{in2})^4 + I_{SS}\mu_n C_{ox}\frac{W}{L}(V_{in1}-V_{in2})^2$$

$$I_{D1}-I_{D2} = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)(V_{in1}-V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}-(V_{in1}-V_{in2})^2}$$

Observations

- $I_{D1} - I_{D2}$ falls to zero for $V_{in1} = V_{in2}$ and $|I_{D1} - I_{D2}|$ increases with increase in $|V_{in1} - V_{in2}|$
- Therefore, $I_{D1} - I_{D2}$ is an odd function of $V_{in1} - V_{in2}$
- Its important to notice that I_{D1} and I_{D2} are even functions of their respective gate-source voltage

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

- Equivalent G_m of M_1 and M_2 → its effectively the slope of the characteristics

Lets denote: $I_{D1} - I_{D2} = \Delta I_D$

$V_{in1} - V_{in2} = \Delta V_{in}$

$$\Delta I_D = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\Delta V_{in}\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}$$

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\frac{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

For $\Delta V_{in} = 0$: $G_m = \frac{\partial \Delta I_D}{\partial \Delta V_{in}} = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}}$

Furthermore: $V_{out1} - V_{out2} = R_D \Delta I = R_D G_m \Delta V_{in}$

$$\therefore |A_v| = \frac{V_{out1} - V_{out2}}{\Delta V_{in}} = \sqrt{\mu_n C_{ox}\frac{W}{L} I_{SS}} R_D$$

Differential Pair – Large Signal Analysis

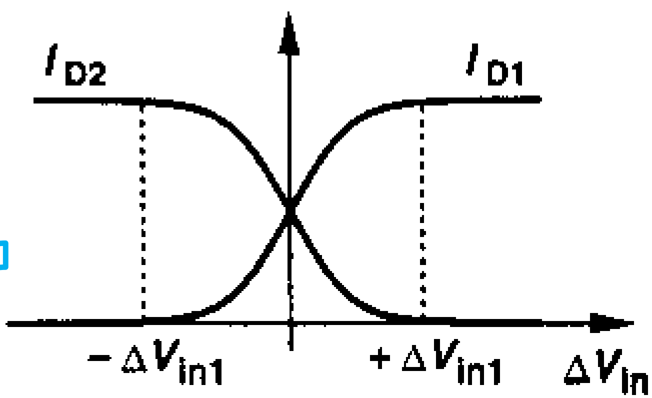
Quantitative Analysis – differential input

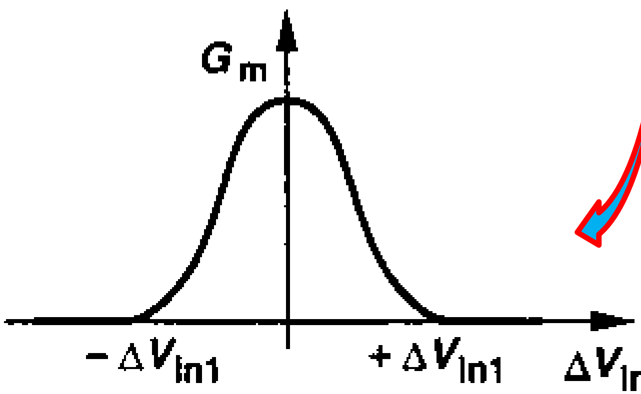
$$G_m = \frac{1}{2}\left(\mu_n C_{ox}\frac{W}{L}\right)\frac{\dfrac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - 2\Delta V_{in}^2}{\sqrt{\dfrac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - \Delta V_{in}^2}}$$

G_m falls to zero for

$$\Delta V_{in} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

ΔV_{in1} represents the maximum differential signal a differential pair can handle.

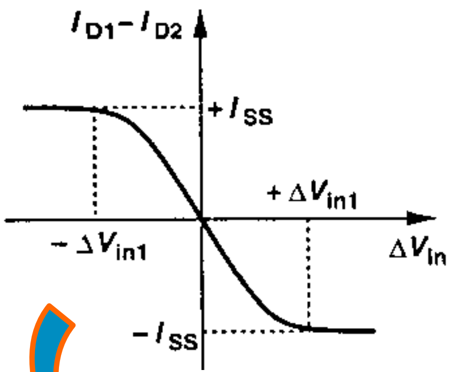




Beyond $|\Delta V_{in1}|$, only one transistor is ON and therefore draws all of the I_{SS}

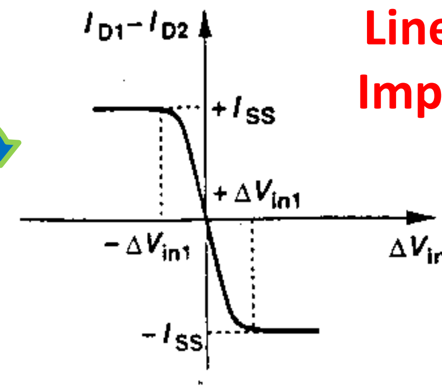
Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input



I_{SS} Constant

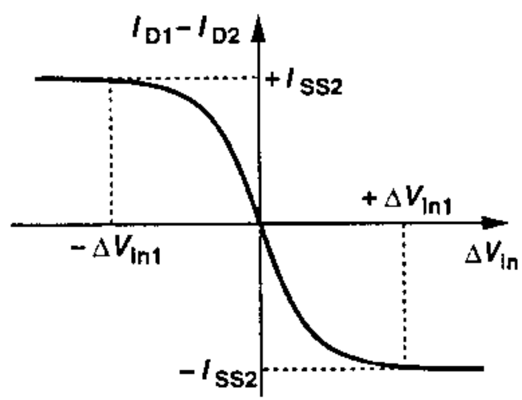
Reduce ΔV_{in1} → by increasing W/L



Linearity Improves

W/L Constant

Increase ΔV_{in1} → by increasing I_{SS}



Linearity Improves

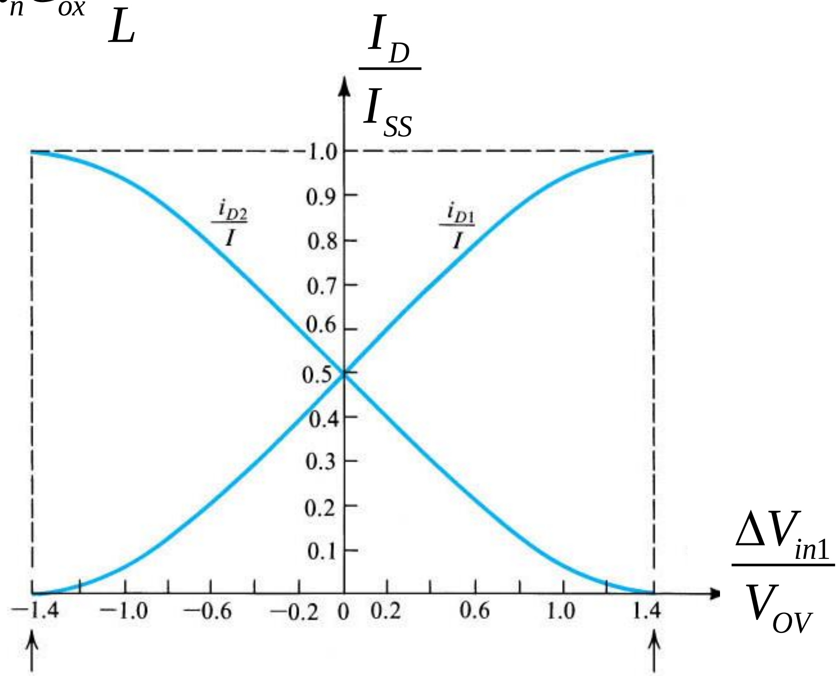
Linearity of a differential pair can be improved by decreasing W/L and/or increasing I_{SS}

Differential Pair – Large Signal Analysis

Quantitative Analysis – differential input

- The equilibrium overdrive (i.e, when M_1 and M_2 are drawing equal portion of I_{SS}) is given by:

$$(V_{GS} - V_T)_{1,2} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \quad \Rightarrow \quad (V_{OV})_{1,2} = \frac{\Delta V_{in1}}{\sqrt{2}}$$



$$-\Delta V_{in1} = -\sqrt{2} V_{OV} \qquad \Delta V_{in1} = \sqrt{2} V_{OV}$$