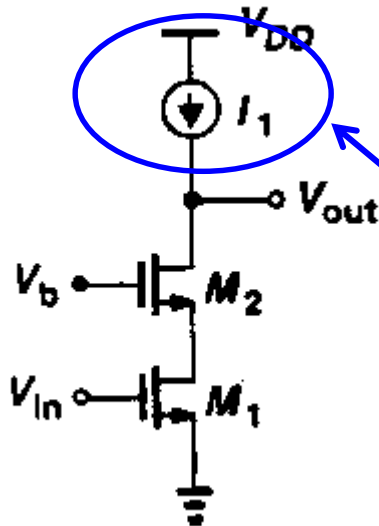## Lecture – 11   Date: 17.09.2015

- Non-idealities in Current Mirror
- Cascode Current Mirror
- Current Mirror Configurations
- Examples

Cascode Amplifier with Current Source Load

We know the gain of Cascode stage is given by:

$$\Rightarrow A_v \approx -\frac{g_{m1}(g_{m2}+g_{mb2})r_{o1}r_{o2}}{\left[R_D+r_{o1}+r_{o2}+(g_{m2}+g_{mb2})r_{o1}r_{o2}\right]}R_D$$

A constant current source possesses very high output impedance ($R_D \rightarrow \infty$), therefore the gain equation changes to:

$$A_v \approx -g_{m1}(g_{m2}+g_{mb2})r_{o1}r_{o2} = -(g_{m1}r_{o1}).(g_{m2}+g_{mb2})r_{o2}$$

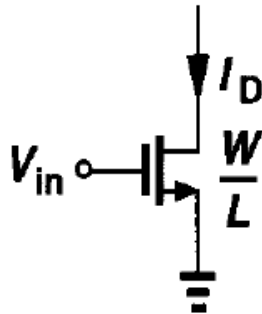**It is apparent that the maximum small-signal voltage gain is the multiplication of gains from CS and CG stages → definitely a big plus!**

$$R_{out} \approx \left(g_{m2}+g_{mb2}\right)r_{o2}r_{o1}$$
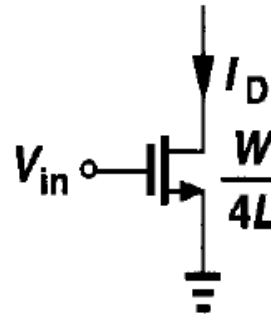
Cascode – Amplifier (contd.)

Discussion with respect to alteration in dimension

What happens if **Length (L)** of the main device is quadrupled while the **Width (W)** remains same?

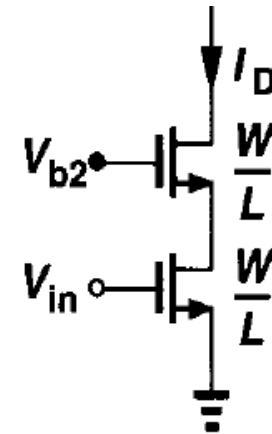$$A_v \approx -g_m r_o = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D \frac{1}{\lambda I_D}}$$

$$A_{v1} = 2A_v$$

$$A_{v2} = (A_v)^2$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$g_{m1} = \frac{g_m}{2}$$
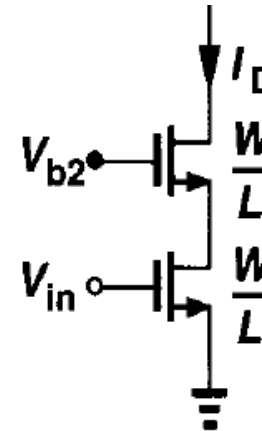
$$g_{m2} = g_m$$

Cascode more suited for noise applications

Cascode – Amplifier (contd.)

Discussion with respect to alteration in dimension
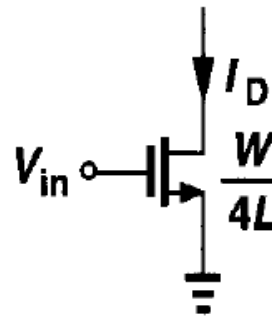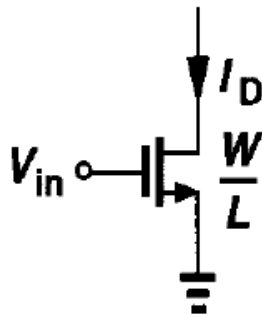
$$\left(V_{GS} - V_{TH}\right)^2 = \frac{2I_D}{\mu_n C_{ox}\left(\dfrac{W}{L}\right)}$$

Quadruppling of **Length (L)** while keeping the **Width (W)** results in doubling of overdrive voltage

For **identical devices**, cascode also exhibits doubling of overdrive voltage

Shielding Property of Cascode

Cascode amplifier and Cascode current source → could be used in applications where the output varies drastically due to any reason! → This variation doesn't affect the subsequent sections greatly → shielding property of Cascode

Example: Two identical NFETs are used to generate constant current sources. However, due to internal circuitry of the system, V_X is higher than V_Y by ΔV.
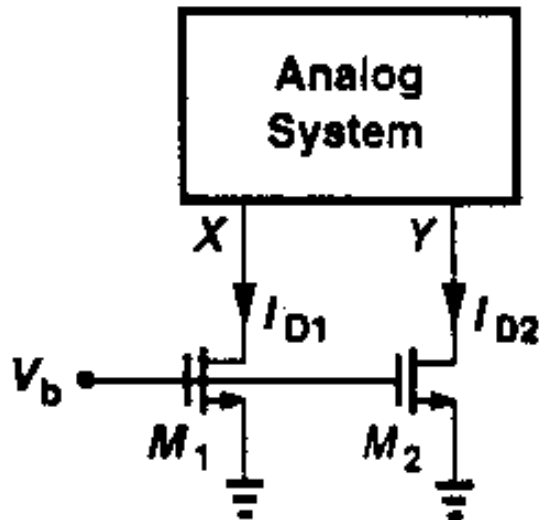
Q: determine the resulting difference between I_{D1} and I_{D2} if $λ ≠ 0$

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(1 + \lambda V_X\right)$$

V_{DS1}

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(1 + \lambda V_Y\right)$$

V_{DS2}

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\lambda \Delta V\right)$$

Shielding Property of Cascode (contd.)

Q: Add Cascode devices to M1 and M2 and then check the difference between I_{D1} and I_{D2} if λ ≠ 0

Cascode devices
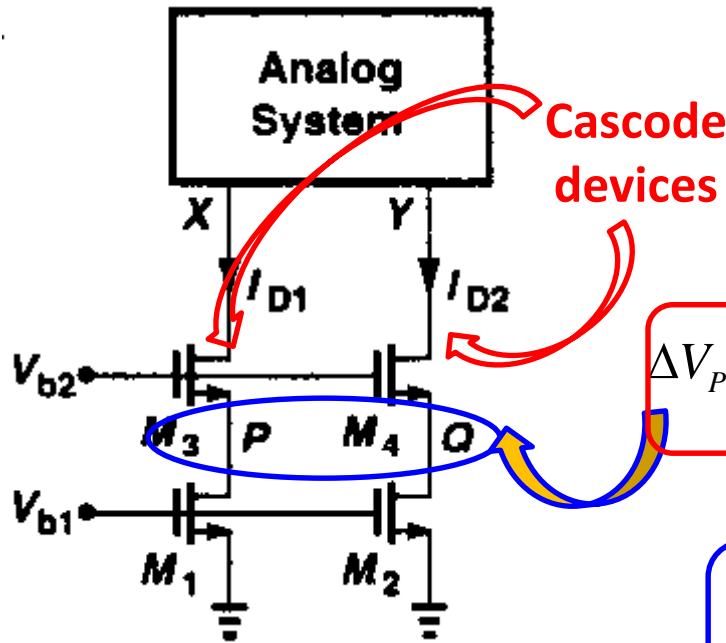
$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\lambda \Delta V_{PQ}\right)$$

$$\Delta V_{PQ} = \Delta V \frac{r_{o1}}{\left[1+\left(g_{m3}+g_{mb3}\right)r_{o3}\right]r_{o1}+r_{o3}} \approx \frac{\Delta V}{\left(g_{m3}+g_{mb3}\right)r_{o3}}$$

$$\therefore I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(V_b - V_T\right)^2\left(\frac{\lambda \Delta V}{\left(g_{m3}+g_{mb3}\right)r_{o3}}\right)$$

This is a large value and thus the Cascode structure gives smaller variation → perfect example of Shielding property!!!

Triple Cascode

- **Cascoding can be extended to three or more devices to achieve higher output impedance**
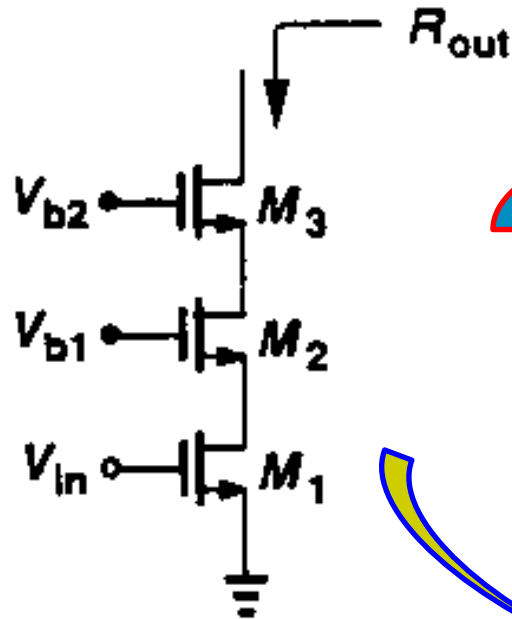
It limits the voltage swing

Here the minimum output voltage equals the sum of three overdrive voltages

Folded Cascode

Self Study

Current Mirror

- **Now let us take the generic equations for the following current mirror:**
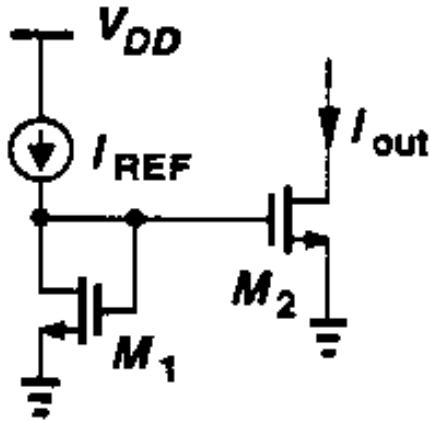
$$I_{REF} = \frac{1}{2}\mu_{n1}C_{ox1}\left(\frac{W}{L}\right)_1(V_{GS1} - V_{T1})^2$$

$$I_{out} = \frac{1}{2}\mu_{n2}C_{ox2}\left(\frac{W}{L}\right)_2(V_{GS2} - V_{T2})^2$$

Even if these transistors are identical and have been fabricated on the same chip [thus practically possessing similar parameters such as V_T, μ_n, C_{ox}], there are three effects that causes current mirror to be different from ideal situation

These effects are: (a) Channel Length Modulation, (b) V_T offset between the two transistors, (c) Imperfect Geometrical Matching

Current Mirror (contd.)

Channel Length Modulation Effect

- **Assuming all other aspects of the transistor are ideal and the ratio of aspect ratios of both the transistors are unity then:**

$$\frac{I_{out}}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

It is assumed that λ is the same for both M_1 and M_2

It is apparent that the difference in V_{DS} causes deviation from the ideal unity current gain or current mirroring

Current Mirror (contd.)

Channel Length Modulation Effect (contd.)
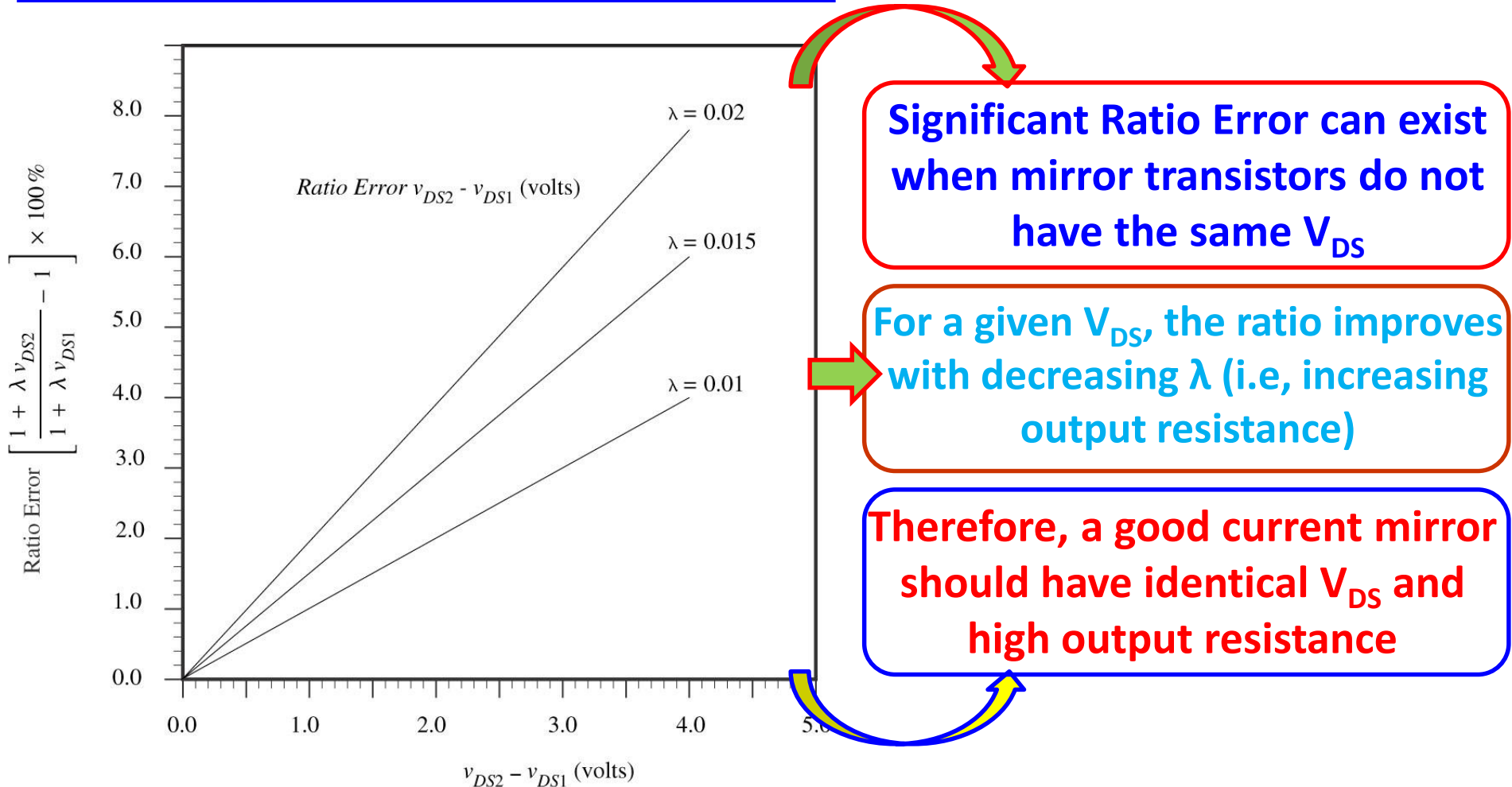
Current Ratio Error vs (V_{DS2} − V_{DS1}) for different values of λ

Significant Ratio Error can exist when mirror transistors do not have the same V_{DS}

For a given V_{DS}, the ratio improves with decreasing λ (i.e, increasing output resistance)

Therefore, a good current mirror should have identical V_{DS} and high output resistance

Current Mirror (contd.)

Channel Length Modulation Effect (contd.)

- **Therefore, the apparent solution seems the use of long channel device**
  - **however this also requires increase in width → results in problems for area and power constraint designs**
  - **furthermore, increase in width also increases the output capacitance → high frequency performance suffers**
  - **short channel devices are commonplace and therefore this solution is not appropriate**

Cascode Current Mirror

- **In order to overcome the error due to channel length modulation, instead of a simple two transistor "current mirror" it is recommended to use "cascode current mirror"**

Cascode Stage
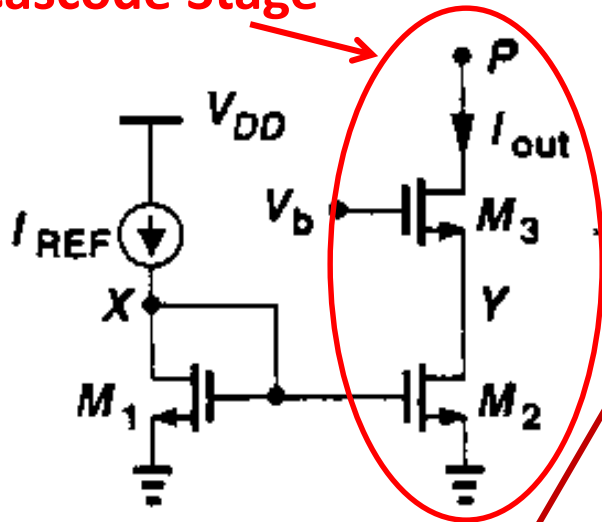
- **In this architecture, small changes in potential at node-P does not have any effect on the potential at node-Y → shielding property of Cascode**

- **Through some technique make $V_Y = V_X$ → then the effect of channel length modulation is insignificant as the mirror equation becomes:**

$$\Delta V_Y = \Delta V_P / [(g_{m3} + g_{mb3})r_{o3}]$$

Once again only dependent on the scaling of devices

$$I_{out} = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

Cascode Current Mirror (contd.)

- **How do we generate the condition: $V_Y = V_X$**

- **For this to happen, we must guarantee $V_b - V_{GS3} = V_X$ → It means one gate-source voltage should be added to achieve this → this is easily achieved by placing a diode-connected device M_0 in series with M_1**

Diode-connected device
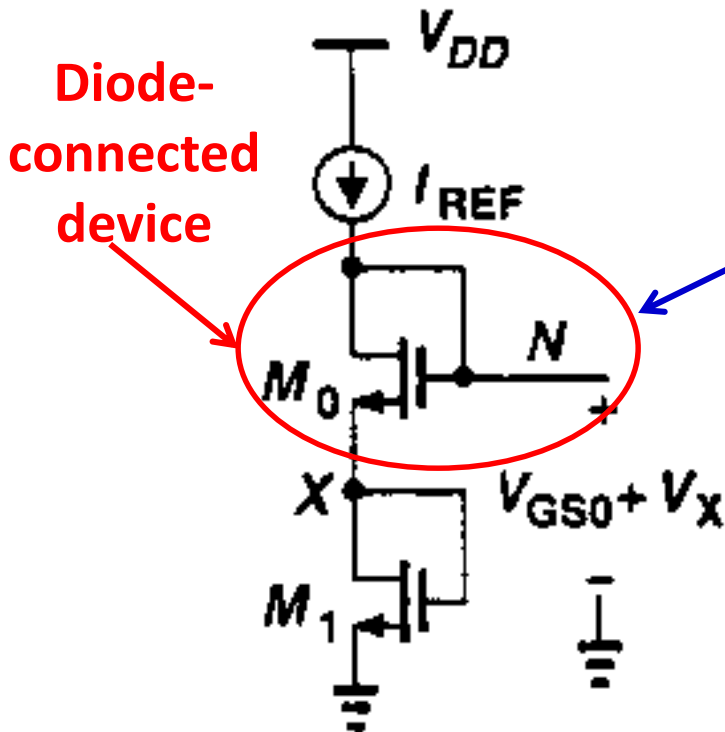
Addition of this device will ensure fulfillment of:
$V_b - V_{GS3} = V_X$

Then proper choice of dimensions of M_0 and M_3 yields $V_{GS0} = V_{GS3}$

Cascode Current Mirror (contd.)

$$V_N = V_{GS0} + V_X$$

The node N is then connected to the gate of cascode device
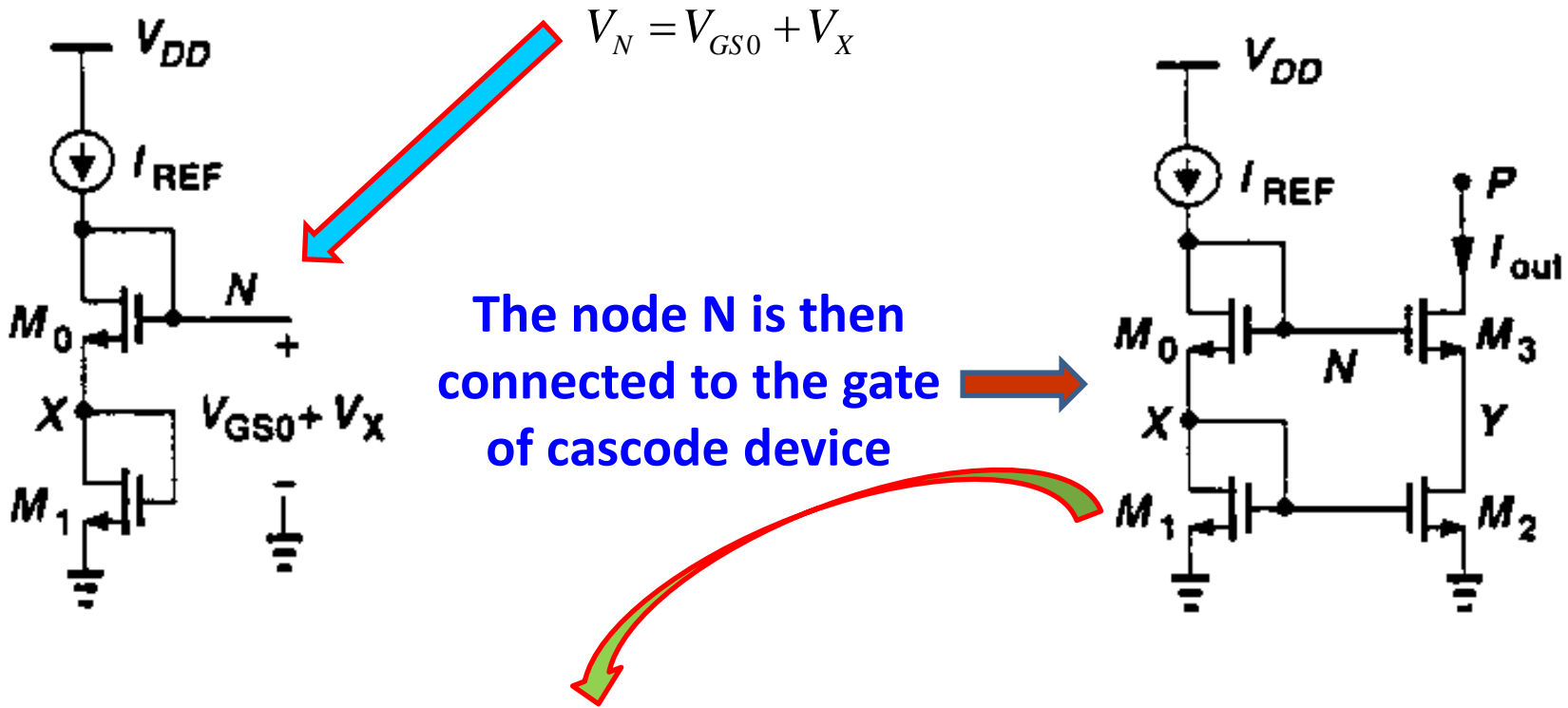
$$V_{GS0} + V_X + V_{GS1} = V_{GS3} + V_Y + V_{GS2}$$

$$\therefore V_{GS0} + V_X = V_{GS3} + V_Y$$

proper choice of dimensions of M_0 and M_3 yields $V_{GS0} = V_{GS3}$

Cascode Current Mirror (contd.)

- **Thus appropriate choices of dimensions of M$_0$ and M$_3$ gives: V$_{GS0}$ = V$_{GS3}$**

- **For this to happen:**

$$\frac{(W/L)_3}{(W/L)_0} = \frac{(W/L)_2}{(W/L)_1}$$

- **Once V$_{GS0}$ = V$_{GS3}$, we get:** $V_X = V_Y$

- **V$_X$ = V$_Y$ leads to the condition: V$_{DS1}$ = V$_{DS2}$ → transforms the mirror equation:**

$$I_{out} = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

Valid even when there exist body effect in transistors M$_0$ and M$_3$

- **Cascode configuration improves the accuracy of current copying capability → but what is the major drawback?**

Cascode Current Mirror (contd.)

- As the cascode current mirror provides a constant current source, it should also possess very high output impedance

- Consider once again the following configuration:
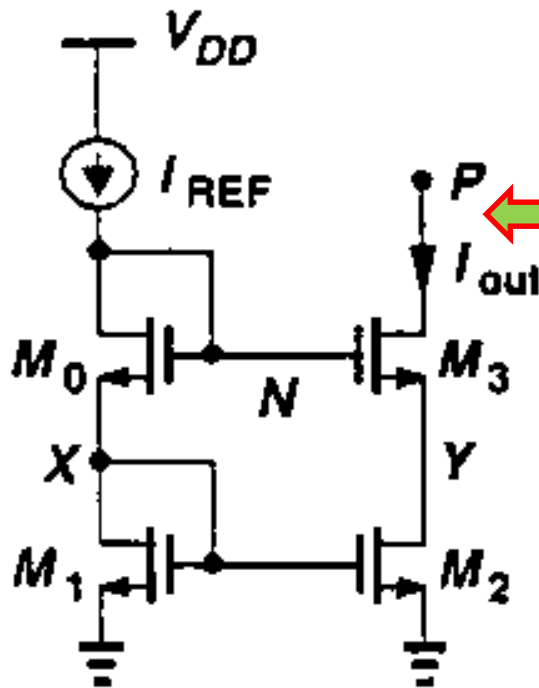
What is R_{out} here?

$$R_{out} \approx g_{m3}r_{o3}r_{o2}$$

Cascode Current Mirror (contd.)
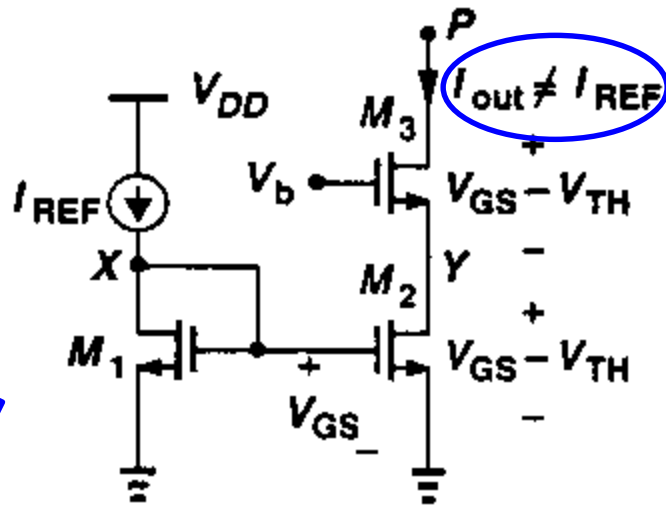
Accuracy and Voltage Swing Trade-off

Standard Cascode Current Mirror

Modified Cascode Current Mirror

- V_b is chosen to allow minimum V_P
- Problem: $V_X \neq V_Y$
- $I_{out} \neq I_{ref}$

- V_b is chosen to allow $V_X = V_Y$
- V_P is not minimum
- However, $I_{out} = I_{ref}$

Current Mirror (contd.)

Threshold Offset Effect

- **The offset between the threshold voltage of two transistors also causes problems in the optimal operation of current mirror**

- **The threshold offset is typically less than 10mV for identical transistors → even this small offset causes substantial error!!!**

- **Let us now consider a current mirror configuration where both have the same V_{DS} and all other aspects of the transistors are equal except V_T. The expression simplifies to:**

$$\frac{I_{out}}{I_{REF}} = \left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}} \right)^2$$

Current Mirror (contd.)

Threshold Offset Effect (contd.)

- **The plot of ratio error between ideal and imperfect current mirroring as a function of $\Delta V_T = V_{T1} - V_{T2}$ results into:**
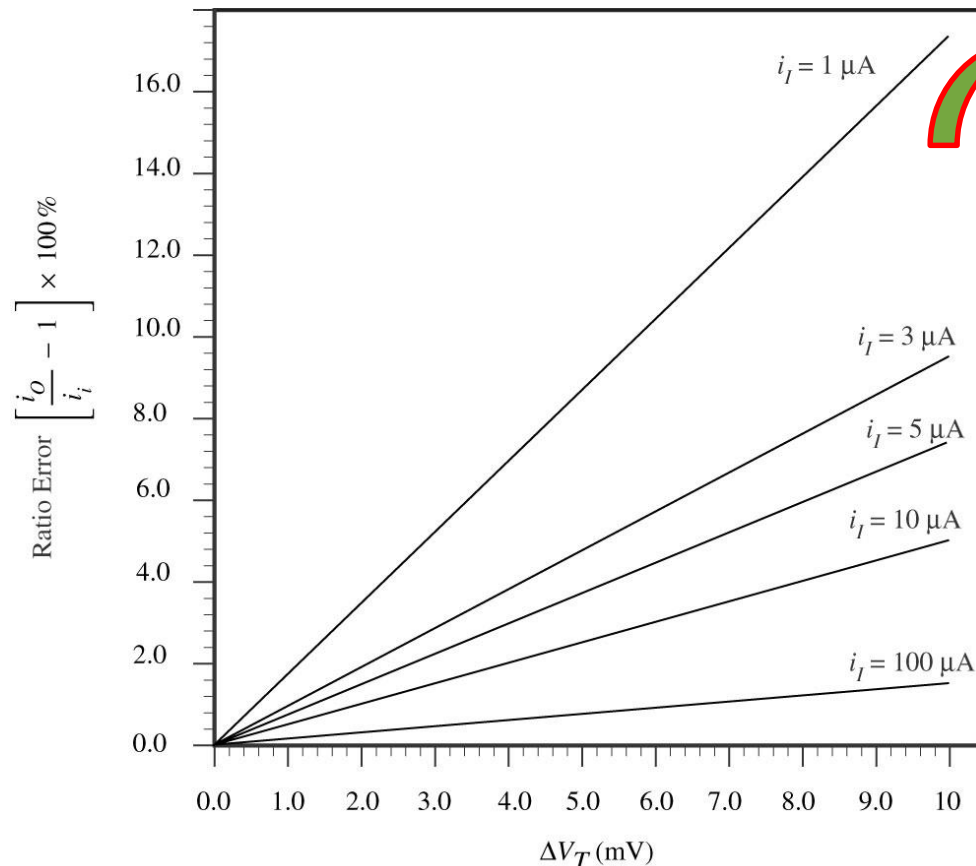
Clearly identifies that better current mirroring is obtained for higher currents

Its due to the fact that V_{GS} is higher for higher currents → ensures that ΔV_T is a smaller percentage of V_{GS}

Current Mirror (contd.)

Threshold Offset Effect (contd.)

- **Sometimes it may happen that the factor $\mu_n C_{ox}$ (let us call it K$'$) is also mismatched alongwith the offset in the threshold.**

- **The current mirror equation then transforms to:**

$$\frac{I_{out}}{I_{REF}} = \frac{K_2^{'}(V_{GS} - V_{T2})^2}{K_1^{'}(V_{GS} - V_{T1})^2}$$

In this case its assumed that the aspect ratio is identical (considering that its designer driven!).

- **Let us define:**

$$\Delta K^{'} = K_2^{'} - K_1^{'} \qquad K^{'} = \frac{1}{2}\left(K_2^{'} + K_1^{'}\right) \qquad V_T = \frac{1}{2}\left(V_{T1} + V_{T2}\right)$$

- **Then:**

$$K_1^{'} = K^{'} - 0.5\Delta K^{'} \qquad K_2^{'} = K^{'} + 0.5\Delta K^{'} \qquad V_{T1} = V_T - 0.5\Delta V_T \qquad V_{T2} = V_T + 0.5\Delta V_T$$

Current Mirror (contd.)

Threshold Offset Effect (contd.)

- **Let us substitute the mirror equation using these assumed parameters:**

$$\frac{I_{out}}{I_{REF}} = \frac{\left(K' + 0.5\Delta K'\right)(V_{GS} - V_T - 0.5\Delta V_T)^2}{\left(K' - 0.5\Delta K'\right)(V_{GS} - V_T + 0.5\Delta V_T)^2}$$

- **Factor out K′ and (V$_{GS}$ – V$_T$) to get:**

$$\frac{I_{out}}{I_{REF}} = \frac{\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2}$$

- **Assuming these quantities to be small, we get:**

$$\frac{I_{out}}{I_{REF}} = \left(1 + \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2\left(1 - \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2$$

Current Mirror (contd.)

Threshold Offset Effect (contd.)

- **Retaining only the first order products gives:**

$$\frac{I_{out}}{I_{REF}} \cong 1 + \frac{\Delta K^{'}}{K^{'}} - \frac{2\Delta V_T}{V_{GS} - V_T}$$

If the percentage change of K' and V_T are known apriori, then this expression can predict the worst-case error in the current mirroring capability of the current mirror

For example, if : $\quad \frac{\Delta K^{'}}{K^{'}} = \pm 5\%$

and: $\quad \frac{\Delta V_T}{V_{GS} - V_T} = \pm 10\%$

then: $\quad \frac{I_{out}}{I_{REF}} \cong 1 \pm 0.05 \pm (-0.2) = 1 \pm (-0.15)$

In this example, the maximum error amounts to 15% provided the tolerances in K' and V_T are correlated
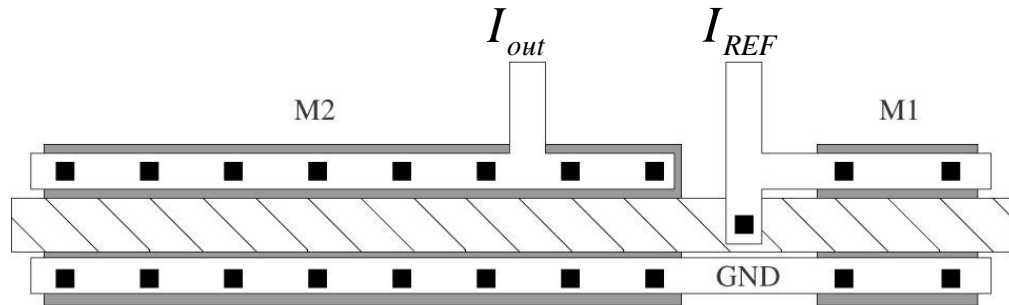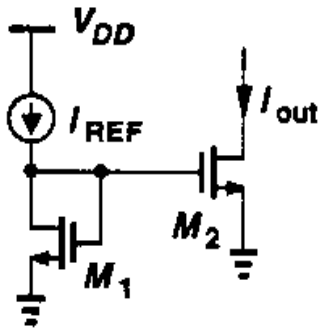
Current Mirror (contd.)

Mismatch in Aspect Ratio

- **mismatches are commonly present even in identical transistors on the same die ← W and L are often mismatched due to mask, photolithography, and diffusion variations → this can be significant even for two transistors placed side by side**

- **One way to overcome these effects is to make transistors much larger than these variations → e.g., for transistors of identical size with W and L greater than $10\mu m$, the errors due to the mismatched aspect ratio will be insignificant ← when compared to errors contributed by offset V_T and Channel Length Modulation**

- **However, many applications (for high current gain applications!) require aspect ratio of transistor (M_2) to be much larger than the aspect ratio of the reference transistor (M_1) ← necessitates creativity in layout techniques !!!**

Current Mirror (contd.)

Mismatch in Aspect Ratio (contd.)

- **Example: we see layout of one-to-four current amplifier below. Its assumed that the lengths are identical ($L_1 = L_2$). Find the ratio error if:**

$$W_1 = 5 \pm 0.1 \mu m \qquad W_2 = 20 \pm 0.1 \mu m$$

$$\frac{I_{out}}{I_{REF}} = \frac{W_2}{W_1} = \frac{20 \pm 0.1}{5 \pm 0.1} = 4\left(\frac{1 \pm (0.1/20)}{1 \pm (0.1/5)}\right) \approx 4\left(1 \pm \frac{0.1}{20}\right)\left(1 - \frac{\pm 0.1}{5}\right)$$

$$\Rightarrow \frac{I_{out}}{I_{REF}} = 4\left(1 \pm \frac{0.1}{20} - \frac{\pm 0.4}{20}\right) \approx 4\left(1 - (\pm 0.06)\right)$$

It is assumed that variations would have the same sign. In this case it is apparent that the ratio error is 1.5% of the desired current ratio

Current Mirror (contd.)

Mismatch in Aspect Ratio (contd.)

- **For large W, it's a good strategy to have W not much larger than L and to put equal transistors in parallel.**

- **A solution to this problem is to use appropriate layout technique. For example, use four duplicates of transistor M_1 to achieve one-to-four ratio. This way the tolerance on W_2 is multiplied by the nominal current gain.**
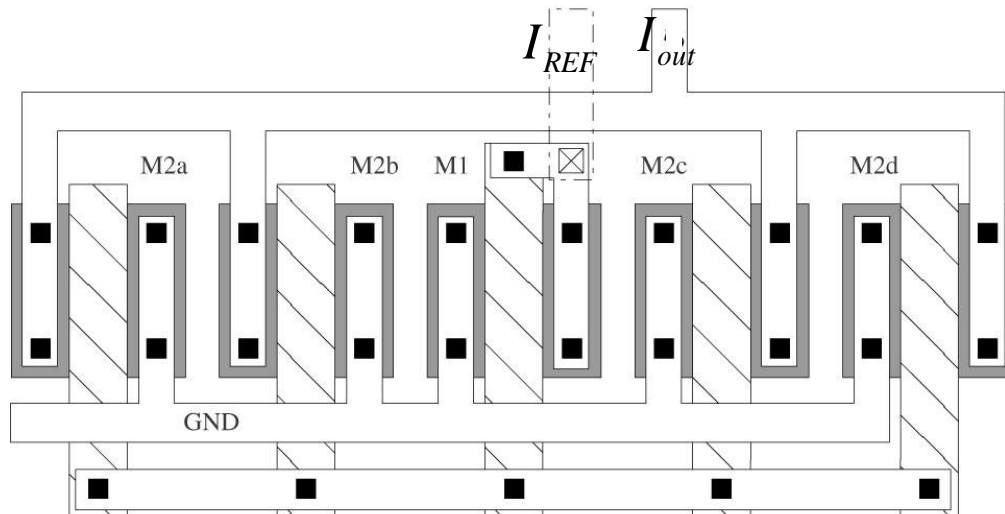

$$\frac{I_{out}}{I_{REF}} = \frac{W_2}{W_1} = \frac{4(5 \pm 0.1)}{5 \pm 0.1} = 4$$

Here its assumed that ΔW should be the same for all the transistors

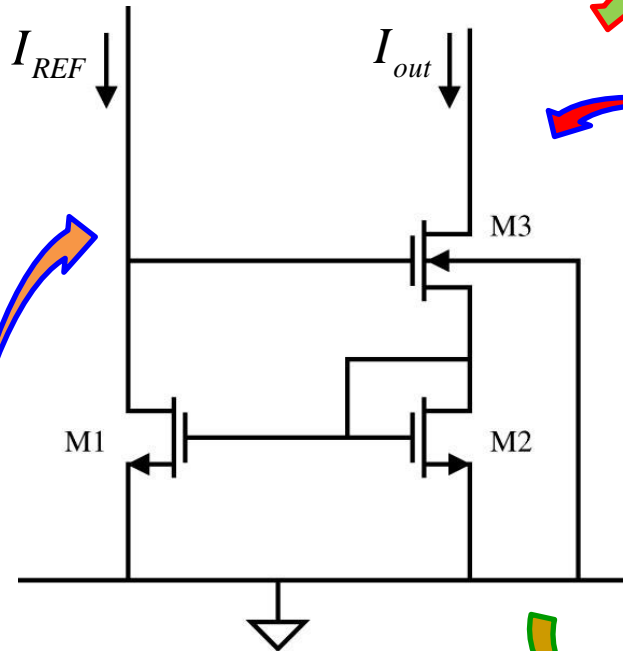## Current Mirror Configurations

- **It is a common practice to design current mirror circuits for high output impedance [for achieving near ideal current source!]**

- **No less important is the voltage headroom [specially for low voltage applications!!!]**

$$r_{out} = \frac{1}{g_m} \| r_o$$

$$V_{out.\min} = V_{DSsat}$$

$$\frac{I_{out}}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$
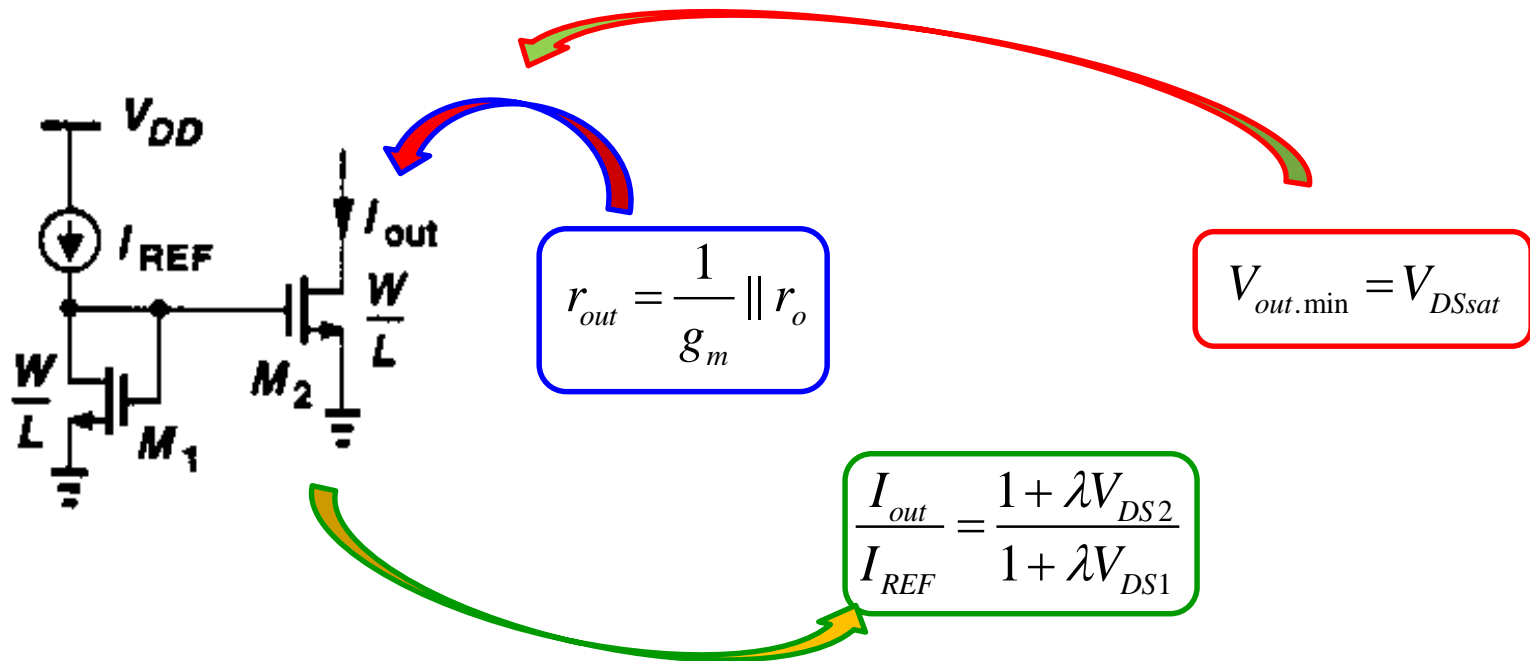
Current Mirror Configurations (contd.)

- **Wilson Current Mirror**

$$V_{out.\min} = V_{DSsat,3} + V_{GS2} > V_T + 2V_{Dsat}$$

Headroom is smaller

$$r_{out} \approx r_{o3} \frac{g_{m3}}{g_{m2}} g_{m1}(R_L \| r_{o1})$$

⇦ **High Value**

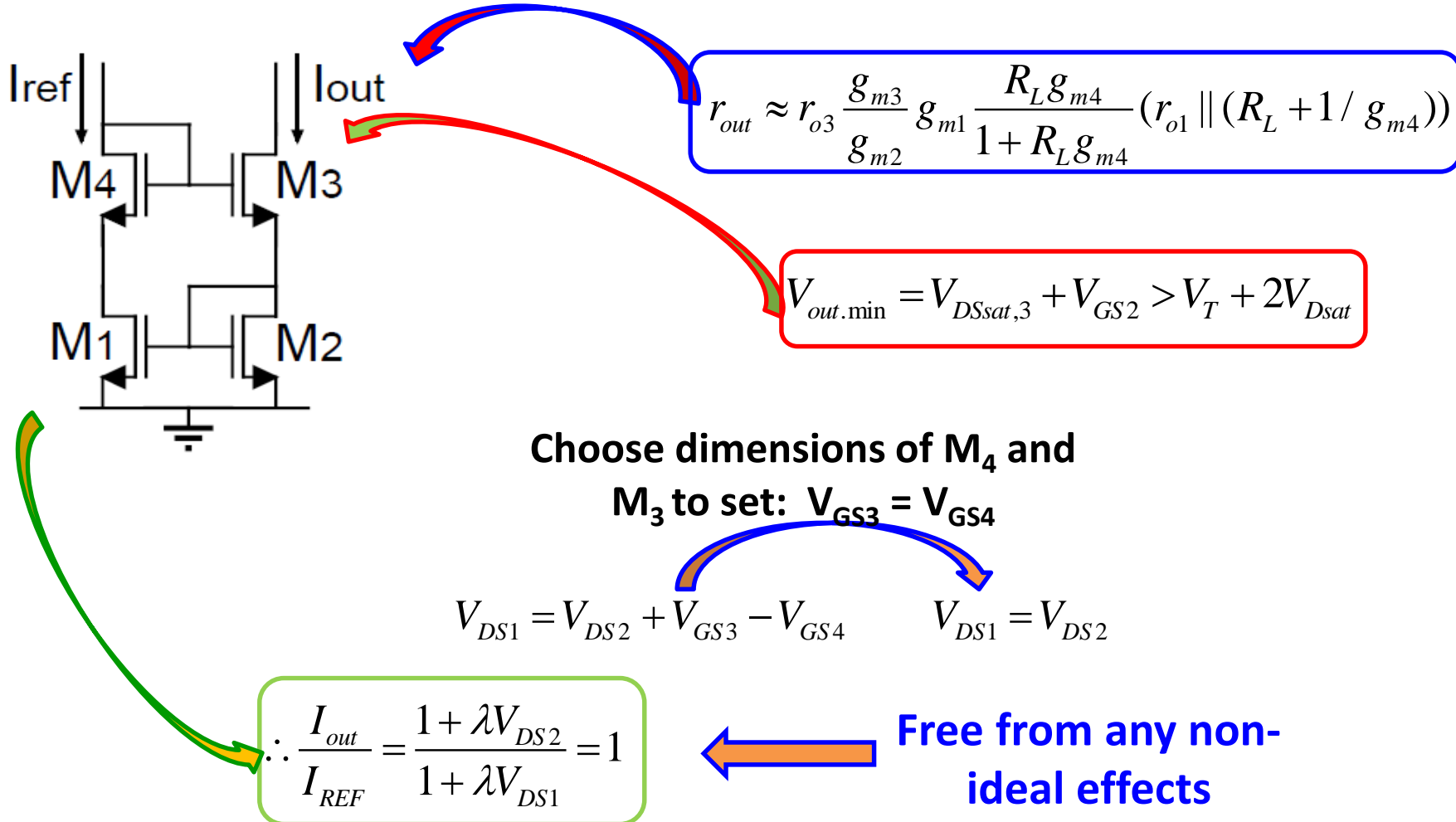$$\frac{I_{out}}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$ ⟹ $$\frac{I_{out}}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda(V_{DS2} + V_{GS3})}$$

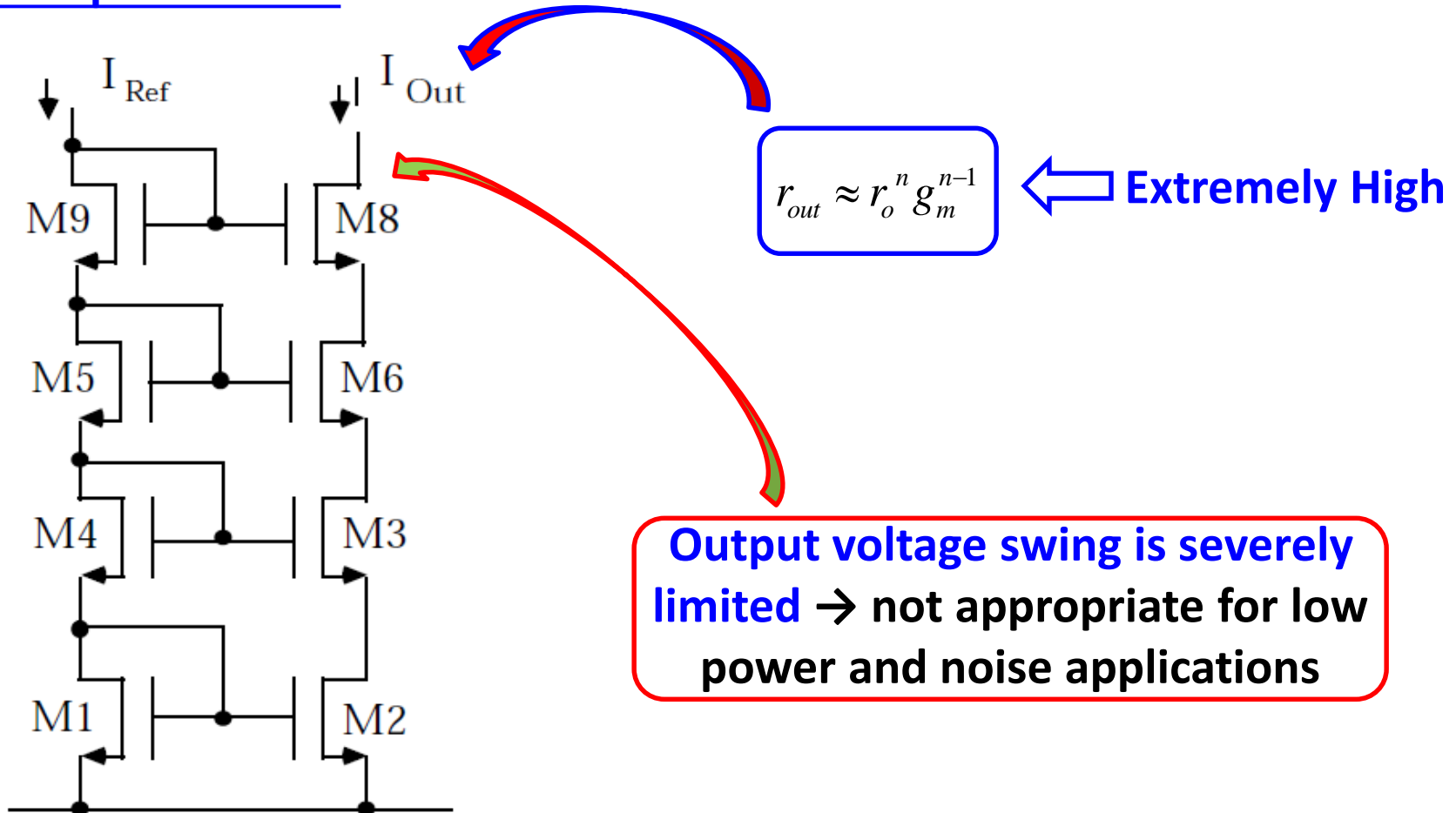**R_L is reference current generator impedance**

The dependence on V_{DS2}

Current Mirror Configurations (contd.)

- **Improved Wilson Current Mirror**

$$r_{out} \approx r_{o3} \frac{g_{m3}}{g_{m2}} g_{m1} \frac{R_L g_{m4}}{1 + R_L g_{m4}} (r_{o1} \| (R_L + 1/g_{m4}))$$

$$V_{out.\min} = V_{DSsat,3} + V_{GS2} > V_T + 2V_{Dsat}$$

Choose dimensions of M$_4$ and M$_3$ to set: V$_{GS3}$ = V$_{GS4}$

$$V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4} \qquad V_{DS1} = V_{DS2}$$

$$\therefore \frac{I_{out}}{I_{REF}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = 1$$

Free from any non-ideal effects

Current Mirror Configurations (contd.)

- **<u>Multiple Cascode</u>**

$$r_{out} \approx r_o^n g_m^{n-1}$$

Extremely High

Output voltage swing is severely limited → not appropriate for low power and noise applications

Current Mirror Configurations (contd.)

Configurations	Current Ratio	Output Swing	Output Impedance
Simple	$\dfrac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}$	V_{DSsat}	$\dfrac{1}{g_m} \parallel r_o$
Cascode	1	$2V_{DSsat} + V_T$	$r_o^2 \cdot g_m$
Triple Cascode	1	$3V_{DSsat} + 2V_T$	$r_o^3 \cdot g_m^2$
Wilson	$\dfrac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}$	$2V_{DSsat} + V_T$	$r_o^2 \cdot g_m$
Improved Wilson	1	$2V_{DSsat} + V_T$	$r_o^2 \cdot g_m$

Example-1

Following figure illustrates a source-degenerated current source. Calculate the output resistance at the given bias current by using the following model parameter: $\mu_n C_{ox}$ = 110 $\mu A/V^2$, λ = 0.04 (L=1 μm) or 0.01 (L= 2μm) /V, $2|\phi_F|$=0.7 , Υ=0.4 $V^{1/2}$
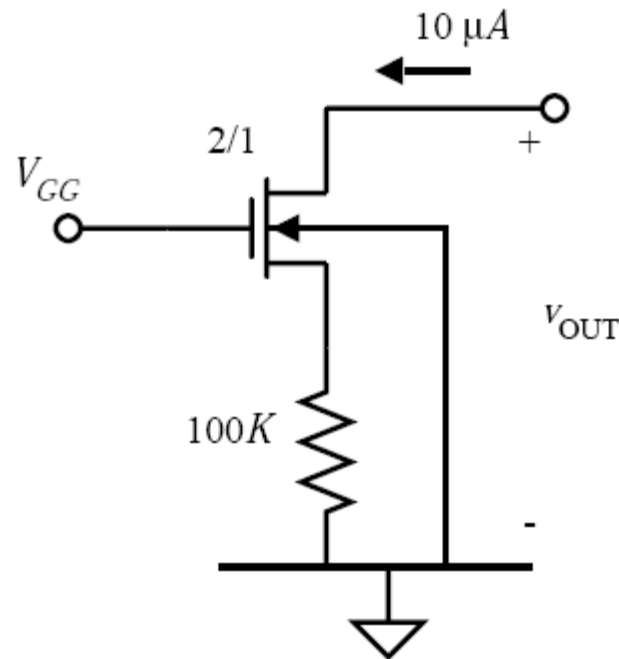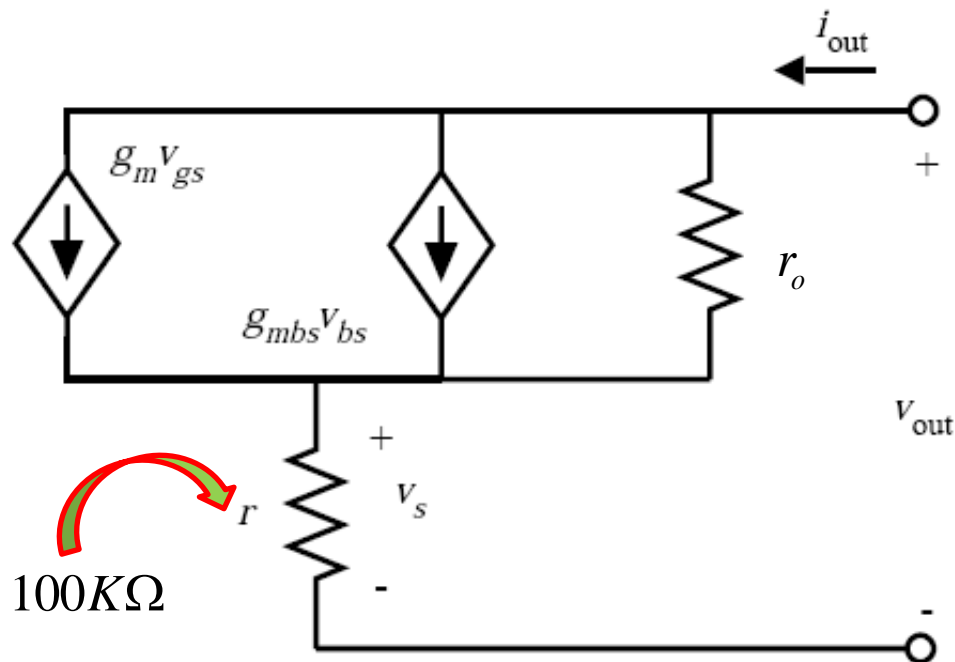
Example-1 (contd.)

The dc terminal conditions are:

$$I_D = 10\mu A \qquad V_S = I_D * R = 10 * 10^{-6} \times 100 * 10^3 = 1V \qquad V_{SB} = V_S$$

Now the small signal model of the circuit is:

Simplification gives:

$$r_{out} = \frac{v_{out}}{i_{out}} = r + r_{out} + \left[\left(g_m + g_{mbs} \right) r_o \right] r$$

Can be approximated to:

$$r_{out} = g_m r_o r$$

Example-1 (contd.)

The device parameters can be computed as:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \implies g_m = \sqrt{2 \times 110 * 10^{-6} \times \frac{2}{2} \times 10 * 10^{-6}} \implies \therefore g_m = 66.3 \times 10^{-6}$$

$$g_{mbs} = g\frac{\gamma}{2\left(2|\phi_F| + V_{SB}\right)^{1/2}} \implies g_{mbs} = 66.3 * 10^{-6} \frac{0.4}{2\left(0.7+1\right)^{1/2}} \implies \therefore g_{mbs} = 10.17 \times 10^{-6}$$

$$r_o = \frac{1}{\lambda I_D} \implies r_o = \frac{1}{0.04 \times 10 * 10^{-6}} \implies \therefore r_o = 2.5 \times 10^6 \Omega$$

Thus: $r_{out} = 100 * 10^3 + 2.5 * 10^6 + \left[\left(66.6 * 10^{-6} + 10.17 * 10^{-6}\right) 2.5 * 10^6\right] 100 * 10^3 = 21.7 * 10^6 \Omega$

The approximated: $r_{out} = 66.6 * 10^{-6} \times 2.5 * 10^6 \times 100 * 10^3 = 16.65 * 10^6 \Omega$

Example-2

Calculate the minimum output voltage required to keep device in saturation in example-1. The model parameters: $\mu_n C_{ox}$ = 110 µA/V², λ = 0.04 (L=1 µm) or 0.01 (L= 2µm) /V, 2|φ$_F$|=0.7 , ϒ=0.4 V$^{1/2}$
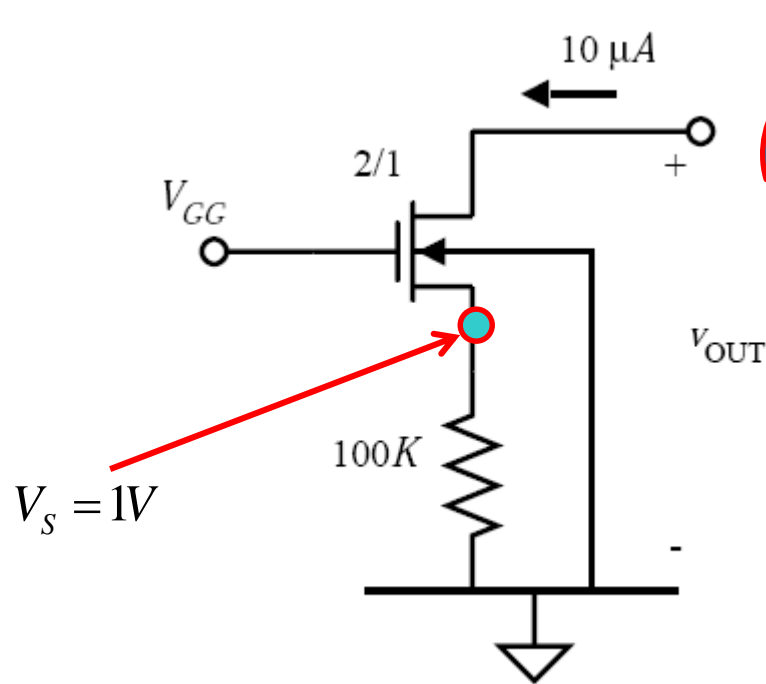
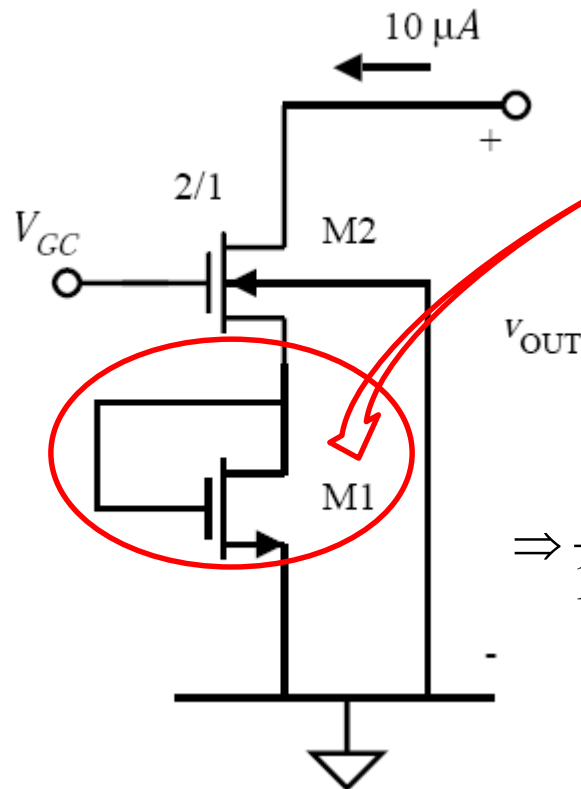$$I_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$\Rightarrow V_{GS} - V_T = \sqrt{\frac{2I_D}{(\mu_n C_{ox})\left(\frac{W}{L}\right)}}$$

$$\therefore V_{GS} - V_T = 0.302V$$

$$V_D(\min) = V_S + (V_{GS} - V_T)(\min) = 1 + 0.302 = 1.302V$$

Example-3

Using the Cascode circuit shown below, design the W/L of M1 to achieve the same output resistance as the circuit in example-1. Ignore body effect.

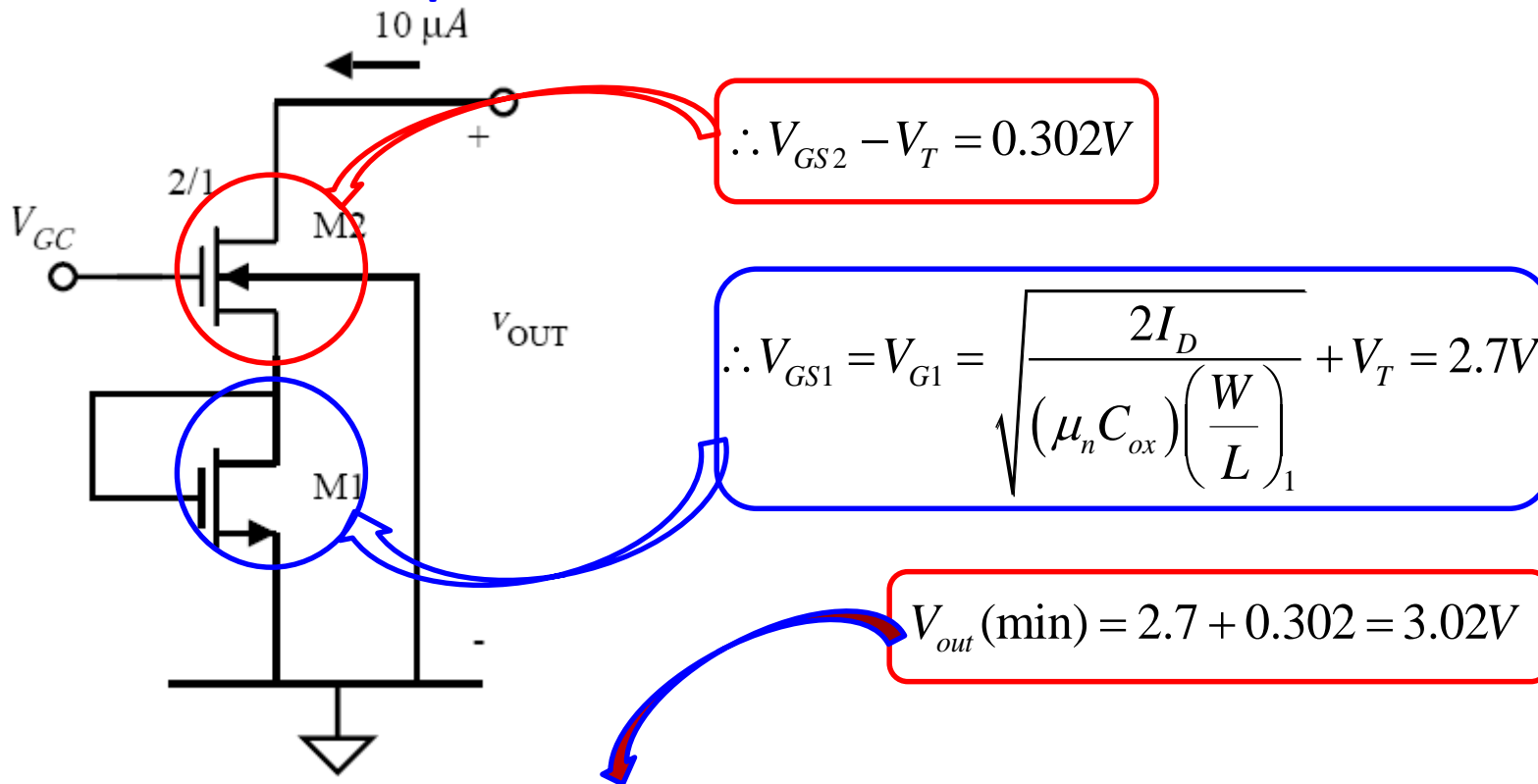This device should provide 100K impedance to maintain overall same output resistance

$$r_{o1} = 100 * 10^3 = \frac{1}{g_{m1}}$$

$$\Rightarrow \frac{1}{100 * 10^3} = g_{m1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_D}$$

$$\left(\frac{W}{L}\right)_1 = \frac{1}{22}$$

**Note that the terminal conditions of M2 must change to support the large gate voltage required for M1**

Example-4

Now calculate the minimum output voltage required to keep the devices in saturation in example-3.

$$\therefore V_{GS2} - V_T = 0.302V$$

$$\therefore V_{GS1} = V_{G1} = \sqrt{\frac{2I_D}{(\mu_n C_{ox})\left(\dfrac{W}{L}\right)_1}} + V_T = 2.7V$$

$$V_{out}(\min) = 2.7 + 0.302 = 3.02V$$

The minimum output voltage for circuit in example-1 is lower than the minimum output voltage for circuit in example-3, therefore is a better choice for low voltage applications

Example-5

Calculate the output resistance, while maintaining all the devices in saturation, for the circuit given below. Assume that I_{out} is actually 10μA. Ignore body effect.
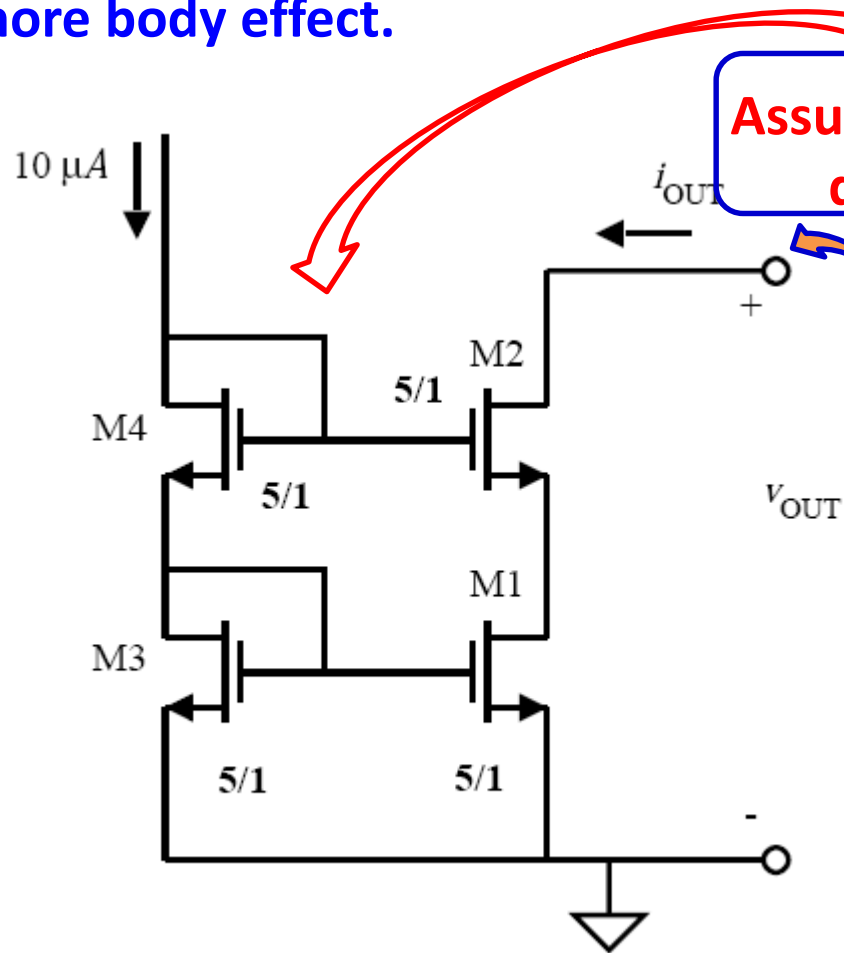
Assume a near perfect current mirror (all devices have 10μA drain current)

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{o1} + r_{o2} + \left[g_{m2} r_{o2} \right] r_{o1}$$

Example-5 (contd.)

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{o1} + r_{o2} + \left[g_{m2} r_{o2} \right] r_{o1}$$
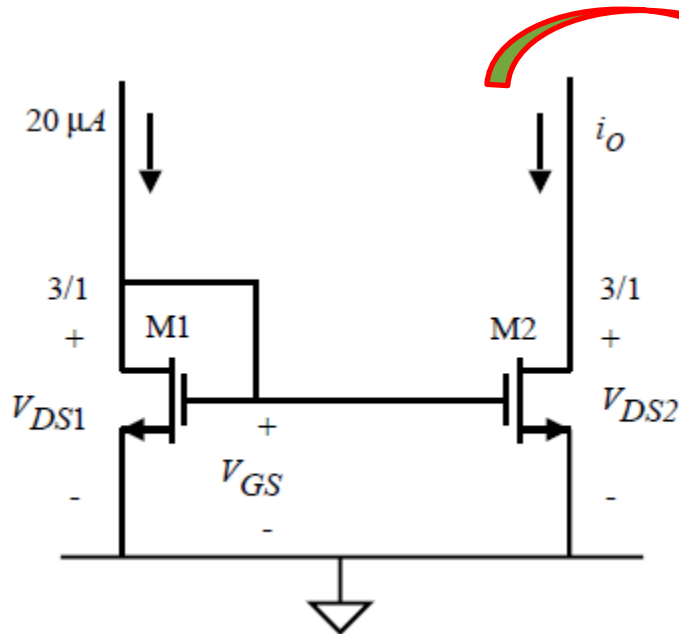
$$r_{o1} = r_{o2} = \frac{1}{\lambda I_D} = 2.5 * 10^6 \, \Omega$$

$$g_{m2} = \sqrt{2 \left(\mu_n C_{ox} \right) \left(\frac{W}{L} \right)_2 I_D} = 104.9 * 10^{-6}$$

$$\therefore r_{out} = 2.5 * 10^6 + 2.5 * 10^6 + \left[104.9 * 10^{-6} \times 2.5 * 10^6 \right] 2.5 * 10^6 \approx 661 * 10^6 \, \Omega$$

Example-6

Consider the simple current mirror given below.

Over process, the absolute variations of physical parameters are as:

Width Variation   +/- 5%
Length Variation +/- 5%
V_T variation   +/- 5%
$\mu_n C_{ox}$ Variation   +/- 5%

Assuming that the drain voltages are identical, what is the minimum and maximum output current measured over the process variations given above. The model parameters: $\mu_n C_{ox}$ = 110 µA/V², λ = 0.04 (L=1 µm) or 0.01 (L= 2µm) /V, $2|\phi_F|$=0.7 , ϒ=0.4 V$^{1/2}$

Example-6 (contd.)

We know:

K

$$I_D = \frac{1}{2} u_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$\Rightarrow V_{GS} = \sqrt{\frac{2I_D}{K\left(\frac{W}{L}\right)}} + V_T$$

- Assuming equal V_{GS} for both the transistors, we can express the output current as:

$$i_o = \frac{1}{2} K_2 \left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2 \times I_{\mathrm{Re}f}}{K_1\left(\frac{W}{L}\right)}} + V_{T1} - V_{T2}\right)^2$$

- We can deduce from this equation that the minimum and maximum of output current will happen under respective following conditions.

	K_1	K_2	$(W/L)_1$	$(W/L)_2$	V_{T1}	V_{T2}
i_o (min)	Max	Min	Max	Min	Min	Max
i_o (max)	Min	Max	Min	Max	Max	Min