Assignment 3
(Please highlight your answer in a box)

1) Find the a.c incremental current I_{out} flowing from node A to ground when $\lambda=0$ and $\lambda\neq0$.
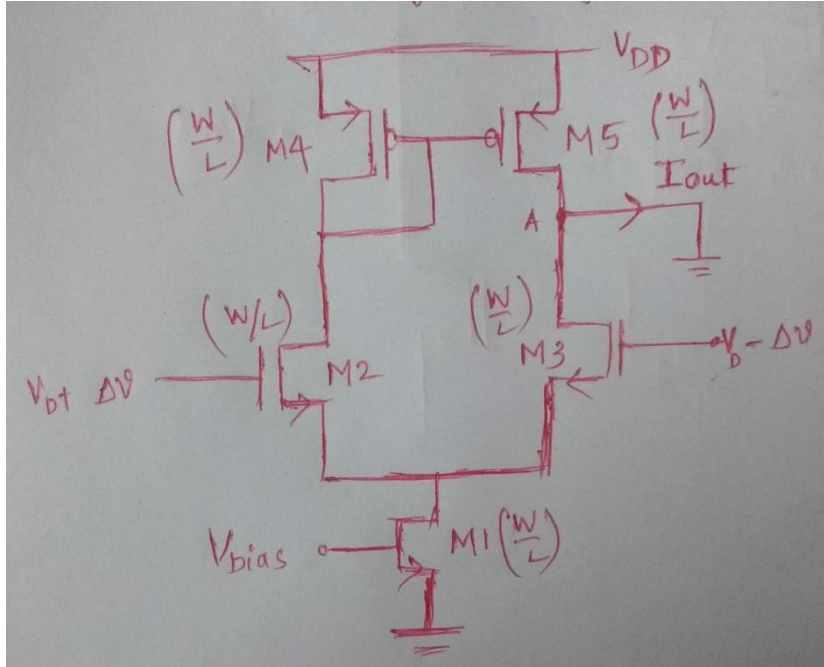**(Assuming all devices are equal in size and the tail current source is Ideal)**

Figure 1

2) $I_{bias}=25uA$, VDD = 1.8V, $(W/L)_{3,4}=50$ and $(W/L)_{1,2,5,6,10}=100$. Consider the other transistor size *(w/L)* which are not mentioned as 100.
a) Calculate the gain of this amplifier?
b) Slew rate of the amplifier when $C_L=5pF$
c) Simulate in ELDO and compare (Download 130nm PTM file for VDD Supply 2V and calculate all parameters required and proceed)
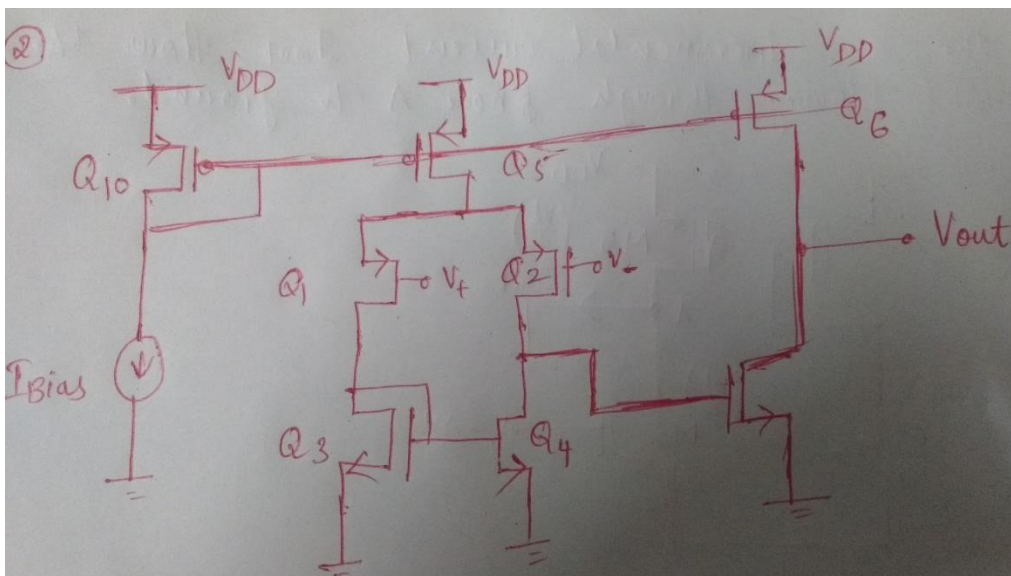

Figure 2

3) In Fig.3, $V_{DD} = 1.8$, $R_D = 2K$. Initially it was designed for a gain of 4 (Pick your own 130nm technology file and get gain of 4). Now bias the transistor which you have used to achieve gain 4 in order to achieve maximum gain without distortions.

Calculate the:

a) D.C level of Input
b) D.C level of output node
c) Power Dissipation
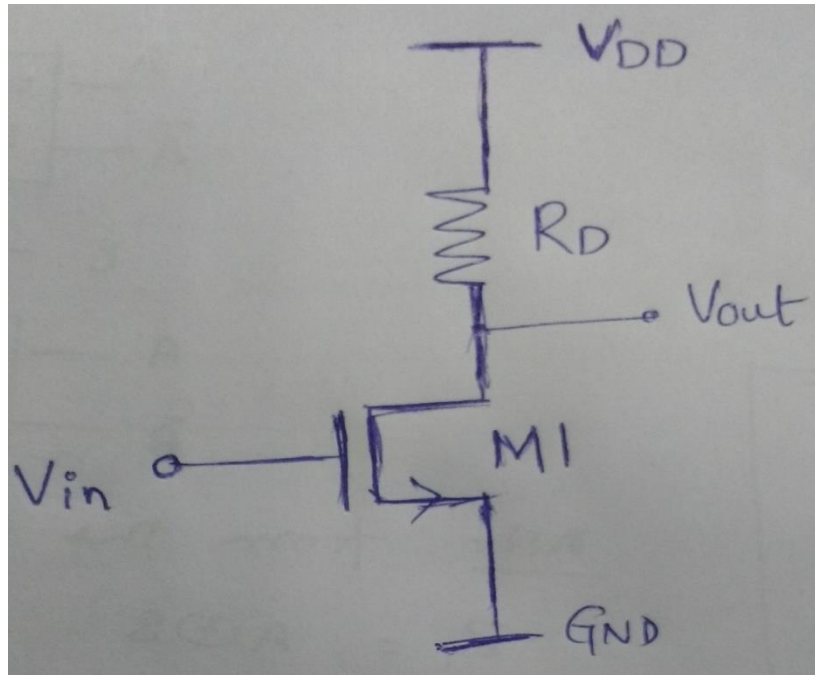d) Threshold voltage of M1
e) Value of parameter K

Figure 3