Home Assignment # 2

Scheme of Marking: Binary Marking
(Please highlight your answer in a box)
Data: $\mu_n C_{ox}$ = 100uA/V^2, W/L = 1, V_t = 1V.
All the Simulations must be carried out in ELDO

Total Marks: 10

Q1:
(a)Name the type of circuit in Fig. 1 (a).

Now, circuit shown in Fig. 1 (a) is required to have output impedance of **5Kohms**.
b) Determine the biasing **current I_o**.

c) Then Fig. 1(a) is actually implemented as Fig. 1 (b). The Quiescent voltage across the resistor R_0 is 5V. Determine the small signal gain for very high frequencies (Neglect all the device capacitances)

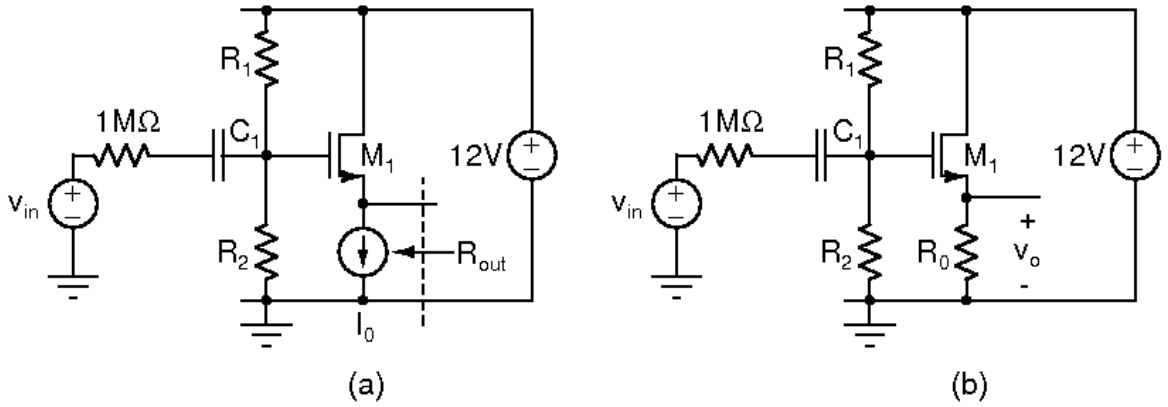

Figure 1

Q2: Transistor M_1 in the Fig. 2 is biased using M_{00}-M_0. Assuming C_1, R_1, and R_2 very large and $i_d/v_i = 20\mu S$ *where* i_d is small signal drain current.

(a) Determine bias current I_0 by assuming all the devices are in saturation.
(b) If M_0 is at the verge of saturation, determine R_1/R_2.
(c) Assume $v_o/v_i = -4$. Determine R_L assuming L_2, C_2 being very large.
Determine condition for L_2 at signal frequency of 1MHz

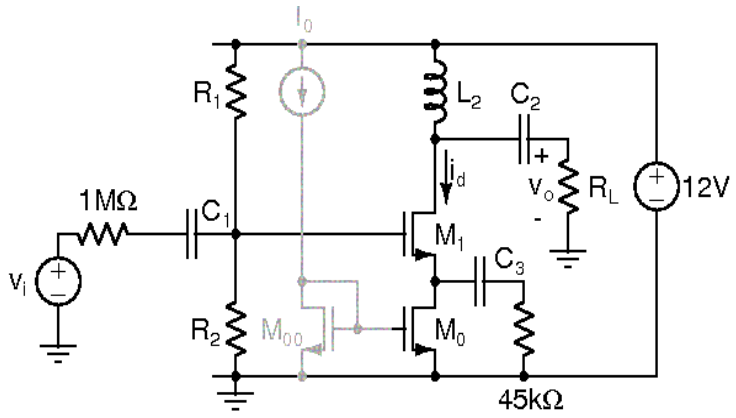

Figure 2

Q3: Find out the output impedance and input impedance for the circuit shown in Fig. 3

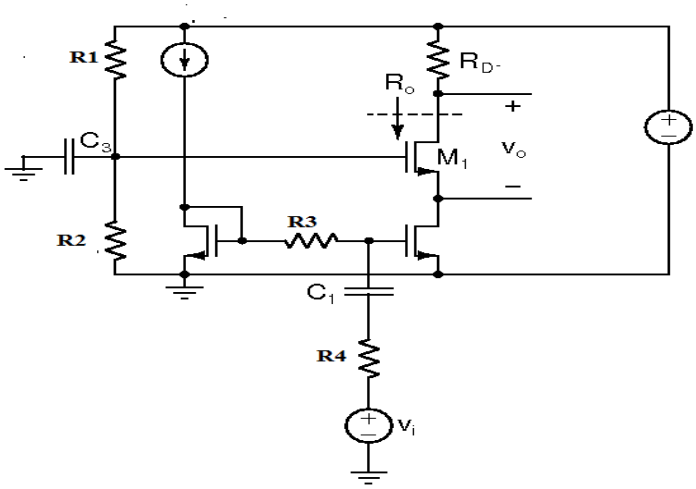

Figure 3

Q4: Fig.4 shows MOS transistors in various bias conditions. Identify the region of operations of devices (**Marks will be awarded only if all are correct).**

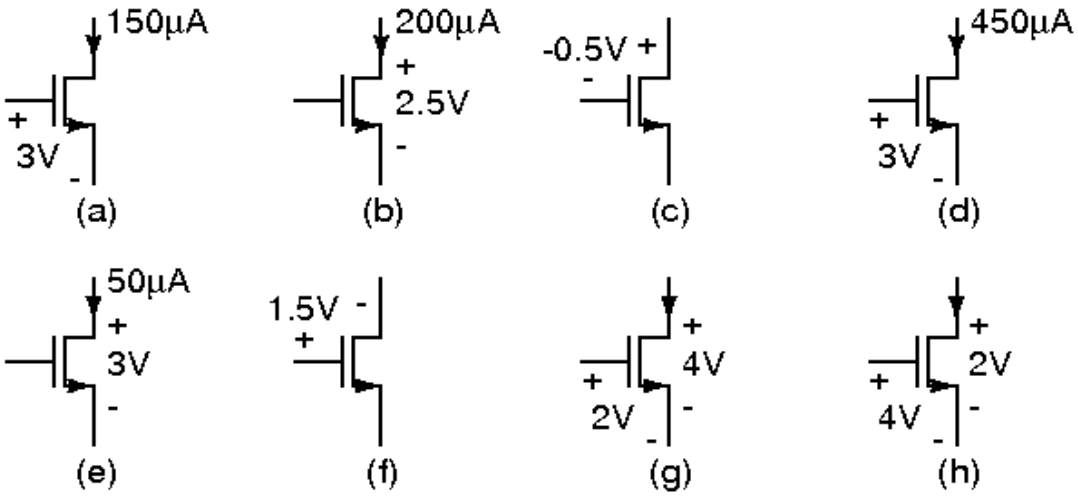

Figure 4

5) Refer Fig.5 and answer the following:

a) Perform DC Analysis (Operating point Analysis) and write down the values of V_{gs}, V_{ds}, V_{gd}
b) Discuss the effect of R_{gl} on biasing (Plot trends)
c) Disuss how the gain changes with variable R_D
d) Plot the trends of gain of the Amplifier with R_{gl} and discuss with appropriate explanation
e) Plot Gain with variable C_1 (1µf to 100µf at 10µf step) and variable R_L (1K to 100K at a step of 10K)

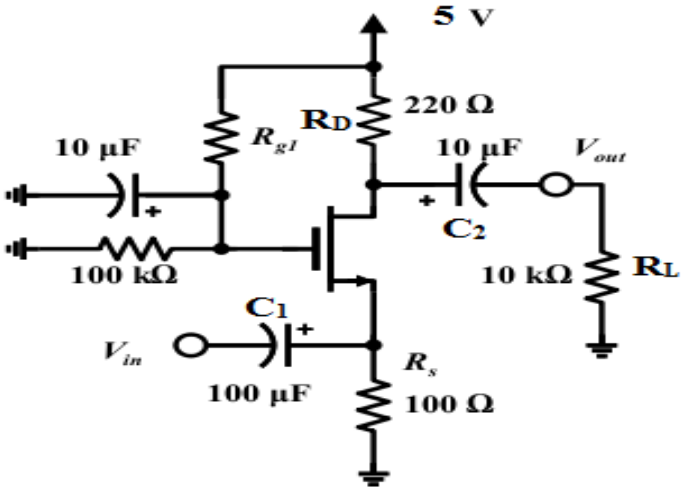

Figure 5