ASSIGNMENT # 1

Analog CMOS Circuit Design (ECE315 / ECE515)

Total Marks: 10 (each questions carry equal marks)

1. A three terminal Non linear device shown in Figure - 1 exhibits definite ***I_1 vs V_1, I_1 vs V_2, I_2 vs V_2*** and ***I_2 vs V_1*** characteristics.

Assume that the Non Linear Device shown in Figure (1) can be modelled as,

$I_1 = f(V_1, V_2)$

$I_2 = g(V_1, V_2)$

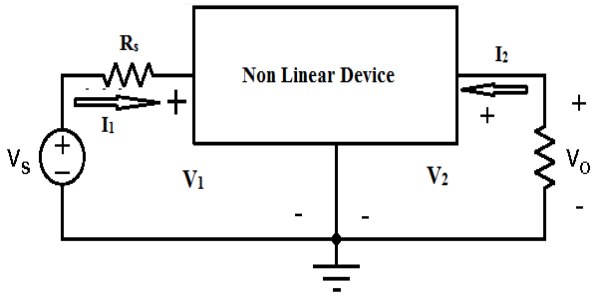

Figure 1

Now answer the following Questions (Your Answers must be Qualitative. An intuitive answer leads blunders)

a. Figure (2) shown below depicts ***I_1 vs V_1*** characteristics of two Non Linear devices (Device (i) and Device (ii)). Assume that the characteristics ***I_1 vs V_2, I_2 vs V_2*** and ***I_2 vs V_1*** are identical for both the amplifiers. Find out which of the Non Linear devices will yield maximum gain at the given operating point shown in the figure (**Green Circle**).

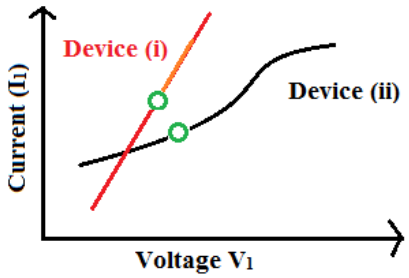

Figure 2

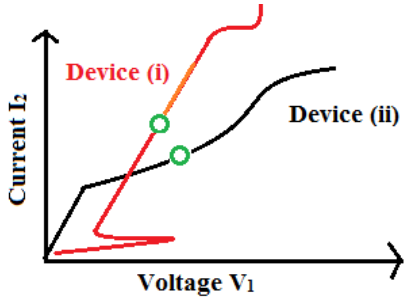

Figure 3

b. Figure (3) shown below depicts ***I_2 vs V_1*** characteristics of two Non Linear devices (Device (i) and Device (ii)). Assume that the characteristics ***I_1 vs V_2, I_2 vs V_2*** and ***I_1 vs V_1*** are identical for both the amplifiers. Find out which of the Non Linear devices will yield maximum gain at the given operating point shown in the figure (**Green Circle**).

2. Circuit shown in Figure 4 is designed for small signal gain of **– 4**. Consider R_1, R_2 >> 100K and R_D and R_L are same.The supply voltage V_{DD} must be chosen in such a way that at the operating point V_{DS} should be V_{GS} + 1.You have carried out the design assuming $\lambda = 0$. However, after analysis you realized that $\lambda = 0.0625V^{-1}$.

a. What is the actual small signal gain.

b. What is the value of R_D to be used to restore the small signal gain to – 4.

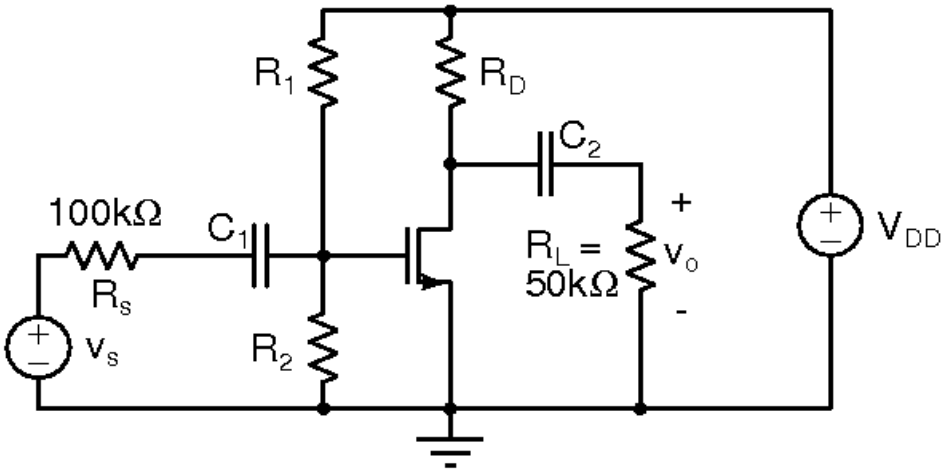

Figure 4

3. Assume that you have got two NMOSFET's with one at nominal threshold voltage (V_T) and other having a variation ΔV_T from its nominal value. How the transconductance ***(g_m)*** and Drain Current (I_{DS}) of the device varies with ΔV_T.

Repeat the same by assuming there is a variation in process parameter ***(K) = $\mu C_{ox}(W/L)$*** and **no variation** in threshold voltage.

4. For the circuit shown in **Figure 5:** ***(R_s = 50KΩ, R_g = 50MΩ, R_L = 100KΩ, I = 128 μA, V_T = 1V, $\mu C_{ox}(W/L)$ = 100μA/V^2)***

a. What kind of biasing scheme is incorporated and explain how DC biasing occurs in the circuit.

b. Determine the constraints on C_1 and C_2 such that the circuit behaves as an Amplifier.

c. For the same circuit an Input signal is applied with a frequency of 10KHz what are the values of C_1 and C_2 such that the AC coupling will not disturb in AC incremental analysis.

d. Implement the same using Cadence or SPICE and ELDO simulator for the values you got in ***Part.3*** and compare the gain of the amplifier with theortical gain.

e. Calculate the Input and output Impedence of the Amplifier for the same figure 2

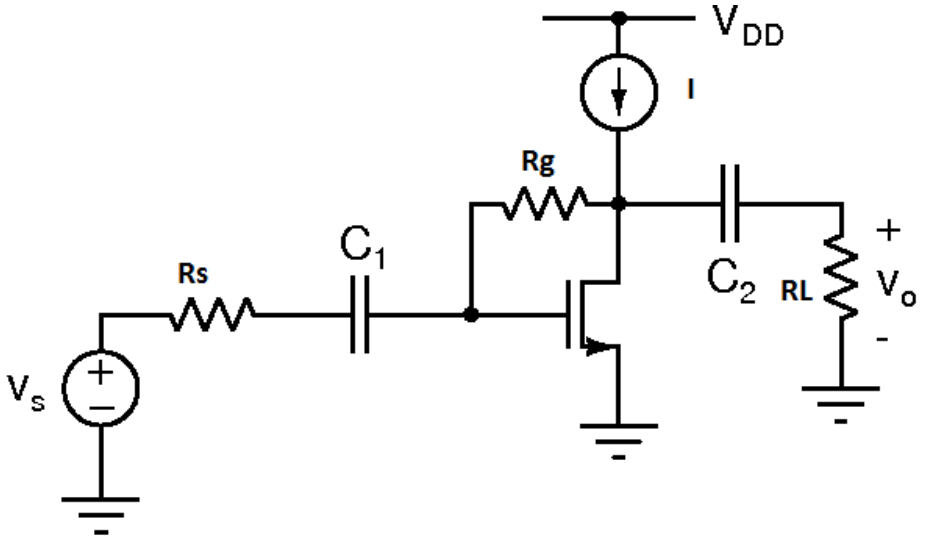

Figure 5